Dual 14-Bit 65-MSPS Digital-to-Analog Converter With Integrated Analog Quadrature Modulator

Check for Samples: AFE7071

FEATURES

- **Maximum Sample Rate: 65 MSPS**
- **Low Power: 334 mW**
- **Interleaved CMOS Input, 1.8–3.3 V IOVDD**
- **Input FIFO for Independent Data and DAC Clocks**
- **3- or 4-pin SPI Interface for Register Programming**
- **Quadrature Modulator Correction: Gain, Phase, Offset for Sideband and LO Suppression**
- **Analog Baseband Filter With Programmable Bandwidth: 20-MHz Maximum RF Bandwidth**
- **RF Frequency Range: 100 MHz to 2.7 GHz**
- **Package: 48-Pin QFN (7-mm × 7-mm)**

APPLICATIONS

- **Low-Power, Compact Software-Defined Radios**
- **Femto- and Pico-Cell BTS**

DESCRIPTION

The AFE7071 is a dual 14-bit 65-MSPS digital-to-analog converter (DAC) with integrated, programmable fourth-order baseband filter and analog quadrature modulator. The AFE7071 includes additional digital signal-processing features such as a quadrature modulator correction circuit, providing LO and sideband suppression capability. The AFE7071 has an interleaved 14-bit 1.8-V to 3.3-V CMOS input. The AFE7071 provides 20 MHz of RF signal bandwidth with an RF output frequency range of 100 MHz to 2.7 GHz.

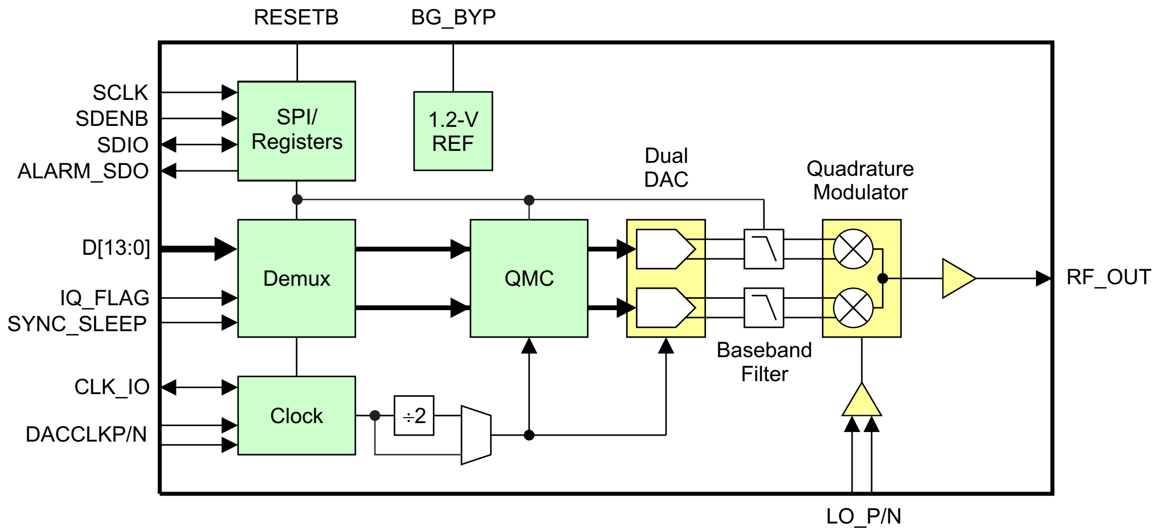
The AFE7071 package is a 7-mm × 7mm 48-pin QFN package. The AFE7071 is specified over the full industrial temperature range (–40°C to 85°C).

AVAILABLE OPTIONS

T_A	ORDER CODE	PACKAGE DRAWING/TYPE	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	AFE7071IRGZT	RGZ / 48QFN quad flatpack no-lead	Tape and reel	250
	AFE7071IRGZR			2500

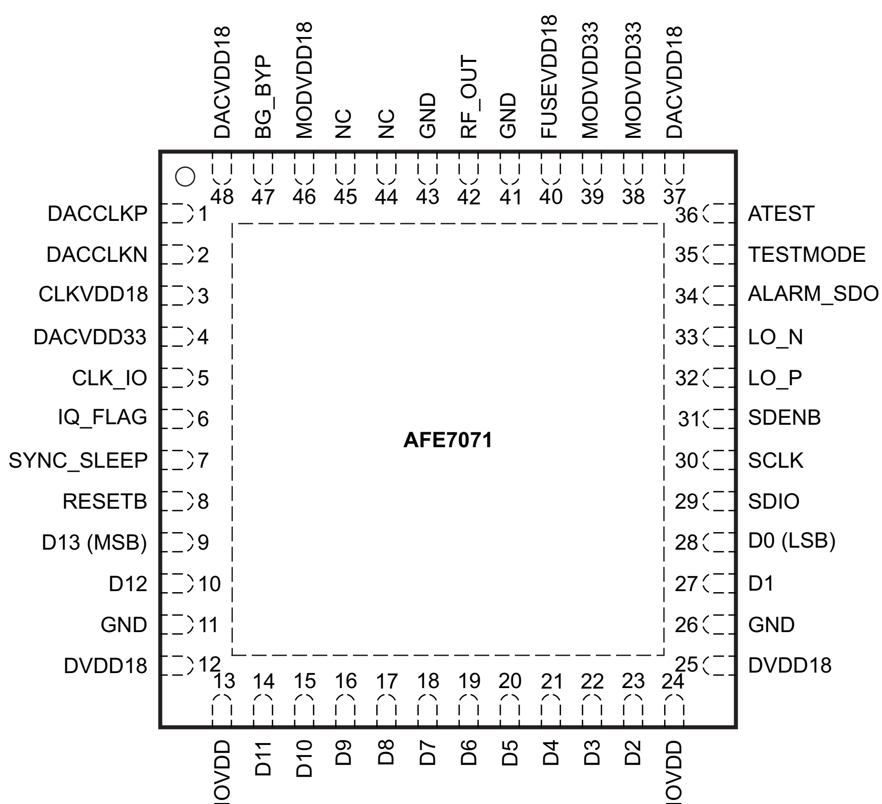
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM



PIN CONFIGURATION

RGZ Package
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
MISC/SERIAL			
ALARM_SDO	34	O	CMOS output for ALARM condition, active-low. The ALARM output functionality is defined through the CONFIG7 registers. Optionally, it can be used as the unidirectional data output in 4-pin serial interface mode (CONFIG3 sif_4pin = 1). 1.8-V to 3.3-V CMOS, set by IOVDD.
RESETB	8	I	Resets the chip when low. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pullup
SCLK	30	I	Serial interface clock. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pulldown
SDENB	31	I	Active-low serial data enable, always an input. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pullup
SDIO	29	I/O	Bidirectional serial data in 3-pin mode (default). In 4-pin interface mode (CONFIG3 sif_4pin), the SDIO pin is an input only. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pulldown
DATA/CLOCK INTERFACE			
CLK_IO	5	I/O	Single-ended input or output CMOS level clock for latching input data. 1.8-V to 3.3-V CMOS, set by IOVDD.
D[13:0]	9, 10, 14–23, 27, 28	I	Data bits 0 through 13. D13 is the MSB, D0 is the LSB. For complex data, channel I and channel Q are multiplexed. For NCO phase data, either 14 bits are transferred at the internal sample clock rate, or 8 MSBs and 8 LSBs are interleaved on D[13:6]. 1.8-V to 3.3-V CMOS, set by IOVDD. Internal pulldown
DACCLKP, DACCLKN	1, 2	I	Differential input clock for DACs.
IQ_FLAG	6	I	When register CONFIG1 iqswap is 0, IQ-FLAG high identifies the DACA sample in dual-input or dual-output clock modes. 1.8-V or 3.3-V CMOS, set by IOVDD. Internal pulldown
SYNC_SLEEP	7	I	Multi-function. Sync signal for signal processing blocks, TX ENABLE or SLEEP function. Selectable via SPI. 1.8-V to 3.3-V CMOS, set by IOVDD.
RF			
LO_P, LO_N	32, 33	I	Local oscillator input. Can be used differentially or single-ended by terminating the unused input through a capacitor and 50-Ω resistor to GND.
NC	44, 45	–	No internal connection
RF_OUT	42	O	Analog RF output
REFERENCE			
ATEST	36	O	Factory use only. Do not connect.
BG_BYP	47	I	Reference voltage decoupling – connect 0.1 µF to GND.
TESTMODE	35	I	Factory use only. Connect to GND.
POWER			
IOVDD	13, 24	I	1.8-V to 3.3-V supply for CMOS I/Os
CLKVDD18	3	I	1.8 V
DVDD18	12, 25	I	1.8 V
DACVDD18	37, 48	I	1.8 V
MODVDD18	46	I	1.8 V
DACVDD33	4	I	3.3 V
MODVDD33	38, 39	I	3.3 V
FUSEVDD18	40	I	Connect to 1.8 V to 3.3 V supply (1.8 V is preferred to lower power dissipation).
GND	11, 26, 41, 43	I	Ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE
Supply voltage range	DACVDD33, MODVDD33, FUSEVDD18, IOVDD(2)	–0.5 V to 4 V
	DVDD18, CLKVDD18, DACVDD18(2)	–0.5 V to 2.3 V
Supply voltage range(2)		–0.5 V to 4 V
	D[13..0], IQ FLAG, SYNC_SLEEP, SCLK, SDENB, SDIO, ALARM_SDO, RESETB , CLK_IO, TESTMODE	–0.5 V to IOVDD + 0.5 V
	DACCLKP, DACCLKN	–0.5 V to CLKVDD18 + 0.5 V
	BG_BYP, ATEST	–0.5 V to DACVDD33 + 0.5 V
	RFOUT, LO_P, LO_N	–0.5 V to MODVDD33 + 0.5 V
Operating free-air temperature range, T_A		–40°C to 85°C
Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND

DC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC SPECIFICATIONS						
	DAC resolution		14			Bits
REFERENCE OUTPUT						
	Reference voltage		1.14	1.2	1.26	V
POWER SUPPLY						
IOVDD	I/O supply voltage		1.71		3.6	V
DVDD18	Digital supply voltage		1.71	1.8	1.89	V
CLKVDD18	Clock supply voltage		1.71	1.8	1.89	V
DACVDD18	DAC 1.8-V analog supply voltage		1.71	1.8	1.89	V
FUSEVDD18	FUSE analog supply voltage	Connect to 1.8-V supply for lower power	1.71	1.8	3.6	V
DACVDD33	DAC 3.3-V analog supply voltage		3.15	3.3	3.45	V
MODVDD33	Modulator analog supply voltage		3.15	3.3	3.45	V
I_{IOVDD}	I/O supply current			2		mA
I_{DVDD18}	Digital supply current			18		mA
$I_{CLKVDD18}$	Clock supply current			2		mA
$I_{DACVDD18}$	DAC 1.8-V supply current			3		mA
$I_{MODVDD18}$	Modulator 1.8-V supply			0.2		mA
$I_{FUSEVDD18}$	FUSE supply current	Register 0x04 bit 7 = 1		1		mA
$I_{DACVDD33}$	DAC 3.3-V supply current			3		mA
$I_{MODVDD33}$	Modulator supply current			90		mA
	Power dissipation	Analog output: QMC active, f_{DAC} = 65 MHz, IOVDD = 2.5 V		335	380	mW
		Sleep mode with clock, internal reference on, IOVDD = 2.5 V		8	25	
		Sleep mode without clock, internal reference off, IOVDD = 2.5 V		5	25	
POWER SUPPLY versus MODE						
	3.3-V supplies (DACVDD33, MODVDD33, IOVDD)	1-MHz full-scale input, RF out on, QMC on, 65 MSPS		102		mA
	1.8-V supplies (DVDD18, CLKVDD18, DACVDD18, FUSEVD18, LVDSVDD18)			36		mA
	Power dissipation			334		mW
	3.3-V supplies (DACVDD33, MODVDD33, IOVDD)	1 MHz full-scale input, RF out on, QMC off, 32.5 MSPS		101		mA
	1.8-V supplies (DVDD18, CLKVDD18, DACVDD18, FUSEVD18, LVDSVDD18)			22		mA
	Power dissipation			325		mW

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (D[13:0], IQ_FLAG, SDI, SCLK, SDENB, RESETB, SYNC_SLEEP, ALARM_SDO, CLK_IO)						
V_{IH}	High-level input voltage	IOVDD = 3.3 V	2.3			V
		IOVDD = 2.5 V	1.75			
		IOVDD = 1.8 V	1.25			
V_{IL}	Low-level input voltage	IOVDD = 3.3 V			1	V
		IOVDD = 2.5 V			0.75	
		IOVDD = 1.8 V			0.54	
I_{IH}	High-level input current	IOVDD = 3.3 V	–80		80	µA
I_{IL}	Low-level input current	IOVDD = 3.3 V	–80		80	µA
C_i	Input capacitance			5		pF
f_{DAC}	DAC sample rate	Interleaved data, f_{DAC} = 1/2 × f_{INPUT}	0		65	MSPS
f_{INPUT}	Input data rate	Interleaved data, f_{INPUT} = 2 × f_{DAC}	0		130	MSPS
DIGITAL OUTPUTS (ALARM_SDO, SDIO, CLK_IO)						
V_{OH}	High-level output voltage	I_{LOAD} = –100 µA	IOVDD – 0.2			V
		I_{LOAD} = –2 mA	0.8 × IOVDD			V
V_{OL}	Low-level output voltage	I_{LOAD} = 100 µA			0.2	V
		I_{LOAD} = 2 mA			0.22 × IOVDD	V
CLOCK INPUT (DACCLKP/DACCLKN)						
	DACCLKP/N duty cycle		40%		60%	
	DACCLKP/N differential voltage		0.4		1	V
Timing Parallel Data Input (D[13:0], IQ_FLAG, SYNC_SLEEP) – Dual Input Clock Mode						
t_{SU}	Input setup time	Relative to CLK_IO rising edge	1	0.2		ns
t_H	Input hold time	Relative to CLK_IO rising edge	1	0.2		ns
t_{LPH}	Input clock pulse high time			3		ns
Timing Parallel Data Input (D[13:0], IQ_FLAG, SYNC_SLEEP) – Dual Output Clock Mode						
t_{SU}	Input setup time	Relative to CLK_IO rising edge	1	0.2		ns
t_H	Input hold time	Relative to CLK_IO rising edge	1	0.2		ns
Timing Parallel Data Input (D[13:0], IQ_FLAG, SYNC_SLEEP) – Single Differential DDR and SDR Clock Modes						
t_{SU}	Input setup time	Relative to DACCLKP/N rising edge	0	–0.8		ns
t_H	Input hold time	Relative to DACCLKP/N rising edge	2	1.2		ns
Timing – Serial Data Interface						
$t_{S(SDENB)}$	Setup time, SDENB to rising edge of SCLK			20		ns
$t_{S(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK			10		ns
$t_{H(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK			5		ns
t_{SCLK}	Period of SCLK			100		ns
t_{SCLKH}	High time of SCLK			40		ns
t_{SCLKL}	Low time of SCLK			40		ns
$t_{D(DATA)}$	Data output delay after falling edge of SCLK			10		ns
t_{RESET}	Minimum RESETB pulse duration			25		ns

AC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LO INPUT						
f_{LO}	LO frequency range		0.1		2.7	GHz
P_{LO_IN}	LO input power		–5		5	dBm
	LO port return loss			15		
INTEGRATED BASEBAND FILTER						
	Baseband attenuation at setting Filtertune = 8 relative to low-frequency signal	2.5 MHz		1		dB
		5 MHz		18		
		10 MHz		42		
		20 MHz		65		
	Baseband attenuation at setting Filtertune = 0 relative to low-frequency signal	10 MHz		1		dB
		20 MHz		18		
		40 MHz		42		
		55 MHz		58		
	Baseband filter phase linearity	RMS phase deviation from linear phase across minimum or maximum cutoff frequency		2		Degrees
	Baseband filter amplitude ripple	Frequency < 0.9 × nominal cutoff frequency		0.5		dB
RF Output Parameters – f_{LO} = 100 MHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power	Full-scale 50-kHz digital sine wave		–1		dBm
IP2	Output IP2	Maximum LPF BW setting, f_{BB} = 4.5, 5.5 MHz		63		dBm
IP3	Output IP3	Maximum LPF BW setting, f_{BB} = 4.5, 5.5 MHz		18		dBm
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		45		dBc
	Sideband suppression	Unadjusted, f_{BB} = 50 kHz, full scale		27		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		137		dBc/Hz
	Output return loss			8.5		dB
RF Output Parameters – f_{LO} = 450 MHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power	Full-scale 50-kHz digital sine wave		0.2		dBm
IP2	Output IP2	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		67		dBm
IP3	Output IP3	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		19		dBm
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		45		dBc
	Sideband Suppression	Unadjusted, f_{BB} = 50 kHz, full scale		38		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		143		dBc/Hz
	Output return loss			8.5		dB
RF Output Parameters – f_{LO} = 850 MHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power	Full-scale 50-kHz digital sine wave		0.3		dBm
IP2	Output IP2	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		64		dBm
IP3	Output IP3	Max LPF BW setting, f_{BB} = 4.5, 5.5 MHz		19		dBm
	Carrier feedthrough	Unadjusted, f_{BB} = 50 kHz, full scale		41		dBc
	Sideband suppression	Unadjusted, f_{BB} = 50 kHz, full scale		37		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		143		dBc/Hz
	Output return loss			8.5		dB
ACPR	Adjacent-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		65		dBc
		10-MHz LTE, PAR = 10 dB, P_{OUT} = –10 dBFS		61		dBc
ALT1	Alternate-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		66		dBc

AC ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sampling rate = 65 MSPS, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF Output Parameters – f_{LO} = 2.1 GHz, Analog Output						
P_{OUT_FS}	Fullscale RF output power			–1.5		dBm
IP2	Output IP2			50		dBm
IP3	Output IP3			19		dBm
	Carrier feedthrough			38		dBc
	Sideband suppression			42		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		141		dBc/Hz
	Output return loss			8.5		dB
ACPR	Adjacent-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		65		dBc
		20 MHz LTE, PAR = 10 dB, P_{OUT} = - 10 dBFS		61		dBc
ALT1	Alternate-channel power ratio	1 WCDMA TM1 signal, PAR = 10 dB, P_{OUT} = –10 dBFS		65		dBc
RF Output Parameters – f_{LO} = 2.7 GHz, Analog Output						
P_{OUT_FS}	Full-scale RF output power			–3.6		dBm
IP2	Output IP2			48		dBm
IP3	Output IP3			17		dBm
	Carrier feedthrough			36		dBc
	Sideband suppression			35		dBc
	Output noise floor	≥ 30 MHz offset, f_{BB} = 50 kHz, full scale		139		dBc/Hz
	Output return loss			8.5		dB

TYPICAL PERFORMANCE PLOTS

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

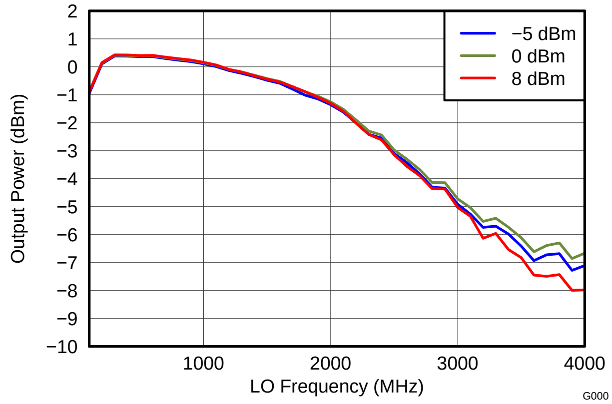


Figure 1. Output Power vs LO Frequency and LO Power

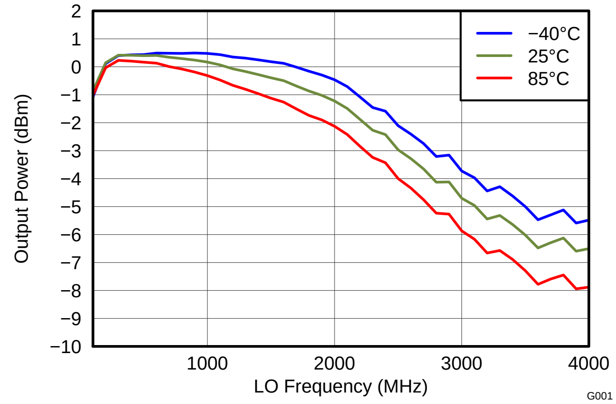


Figure 2. Output Power vs LO Frequency and Temperature

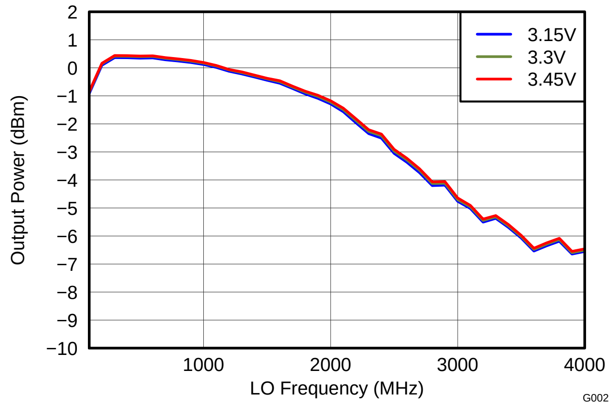


Figure 3. Output Power vs LO Frequency and Supply Voltage

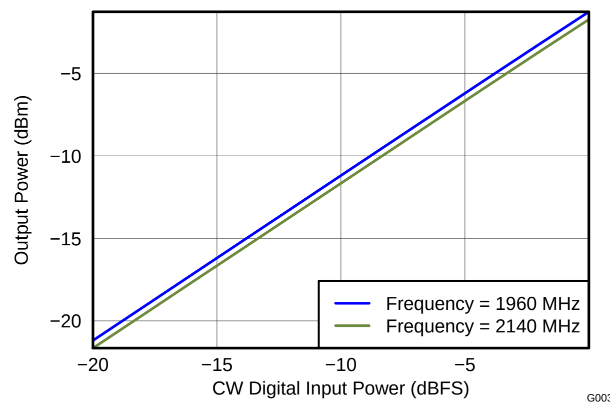


Figure 4. Output Power vs Input Power and LO Frequency

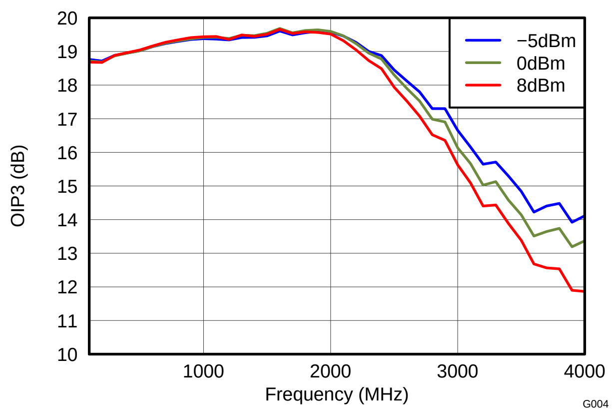


Figure 5. OIP3 vs LO Frequency and LO Power

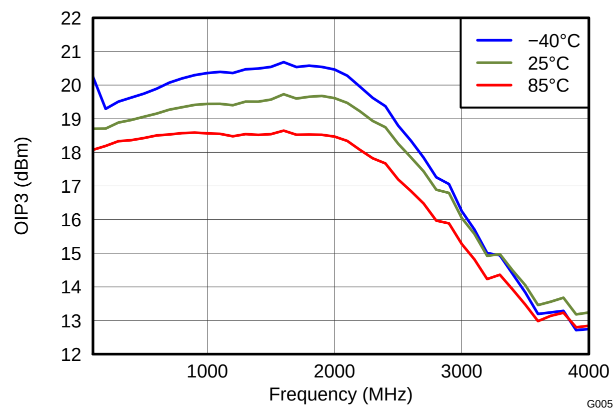


Figure 6. OIP3 vs LO Frequency and Temperature

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

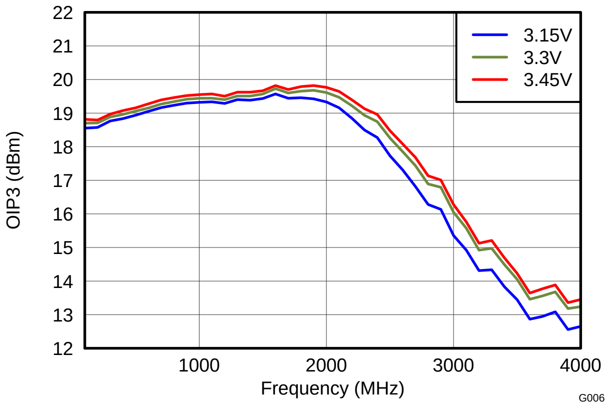


Figure 7. OIP3 vs LO Frequency and Supply Voltage

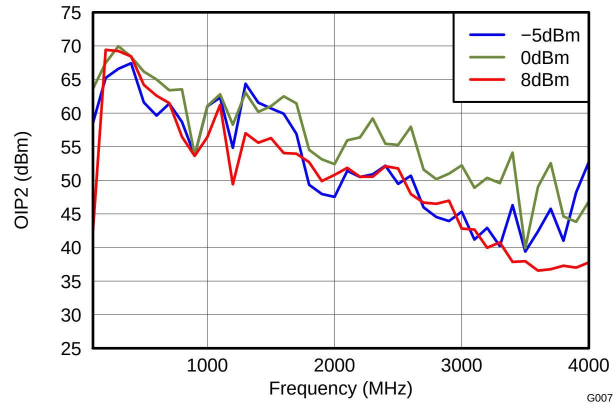


Figure 8. OIP2 vs LO Frequency and LO Power

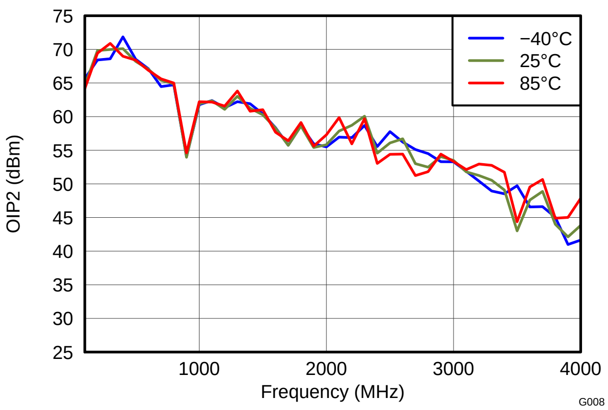


Figure 9. OIP2 vs LO Frequency and Temperature

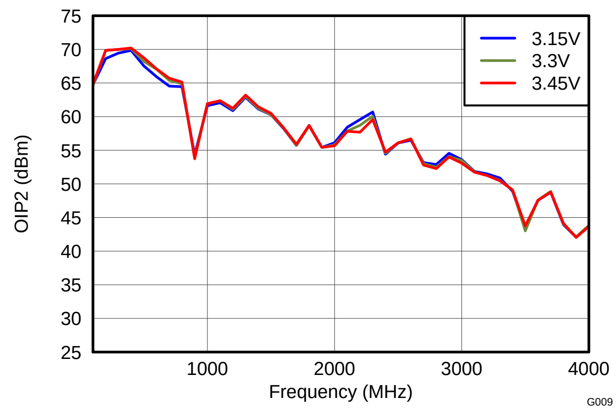


Figure 10. OIP2 vs LO Frequency and Supply Voltage

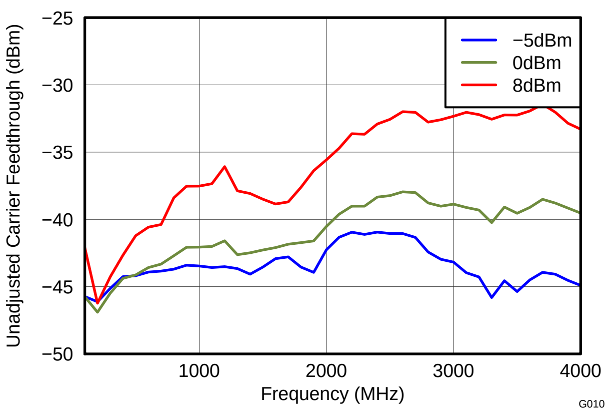


Figure 11. Unadjusted Carrier Feethrough vs LO Frequency and LO Power

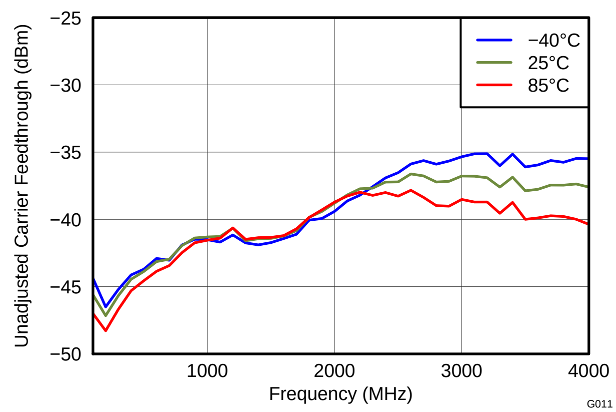


Figure 12. Unadjusted Carrier Feethrough vs LO Frequency and Temperature

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

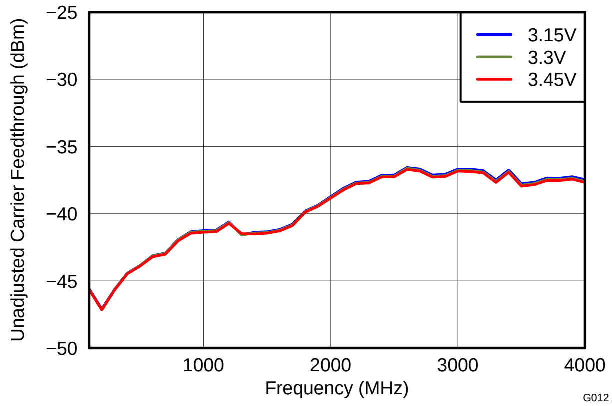


Figure 13. Unadjusted Carrier Feethrough vs LO Frequency and Supply Voltage

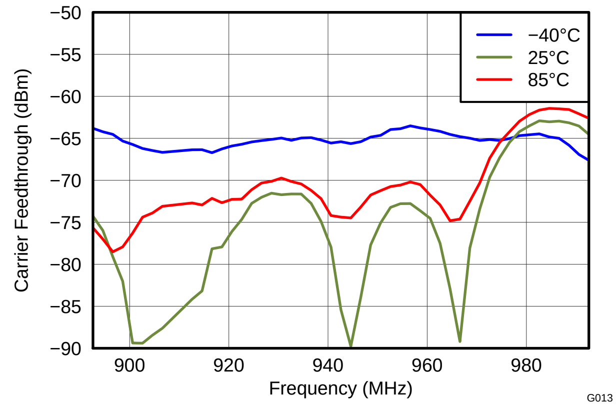


Figure 14. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 940 MHz

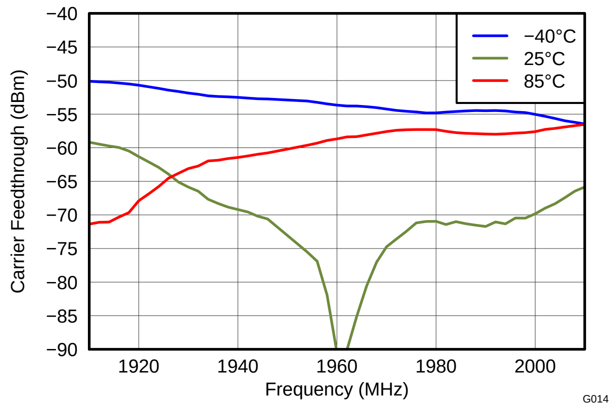


Figure 15. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 1960 MHz

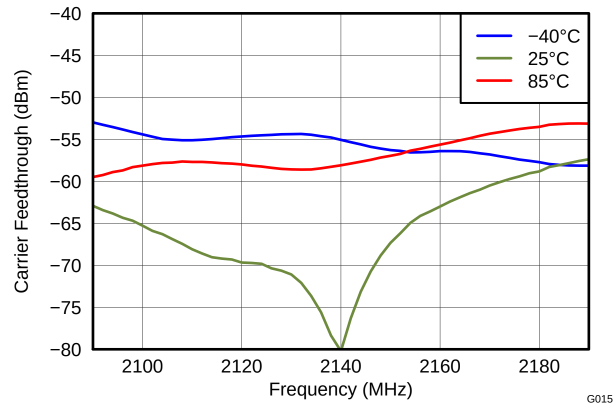


Figure 16. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 2140 MHz

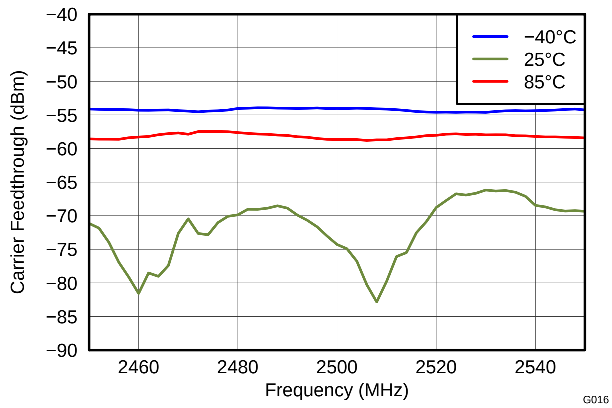


Figure 17. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 2500 MHz

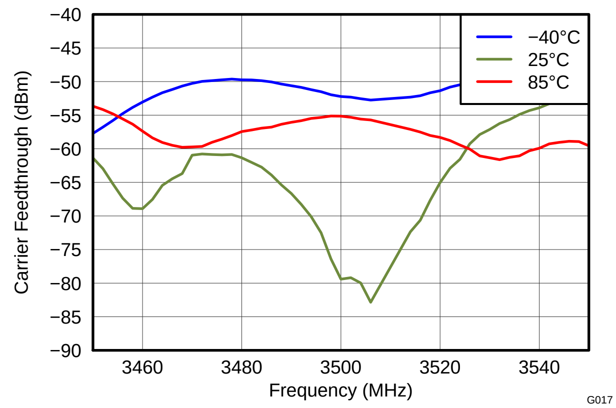


Figure 18. Adjusted Carrier Feethrough vs LO Frequency and Temperature at 3500 MHz

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

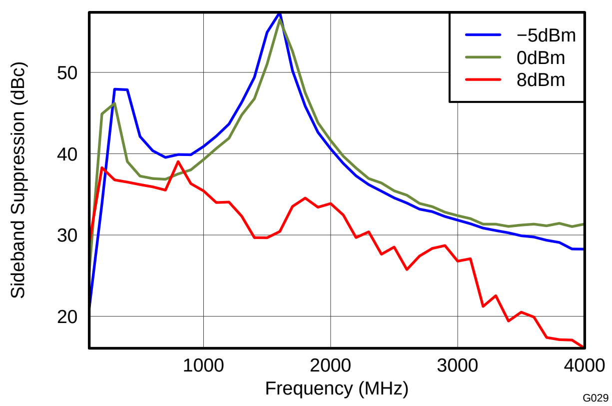


Figure 19. Unadjusted Sideband Suppression vs LO Frequency and LO Power

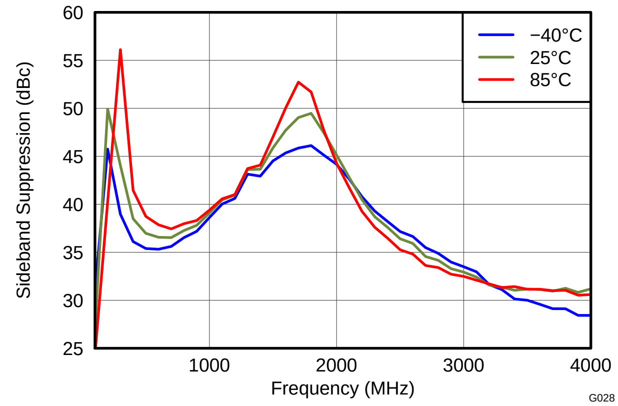


Figure 20. Unadjusted Sideband Suppression vs LO Frequency and Temperature

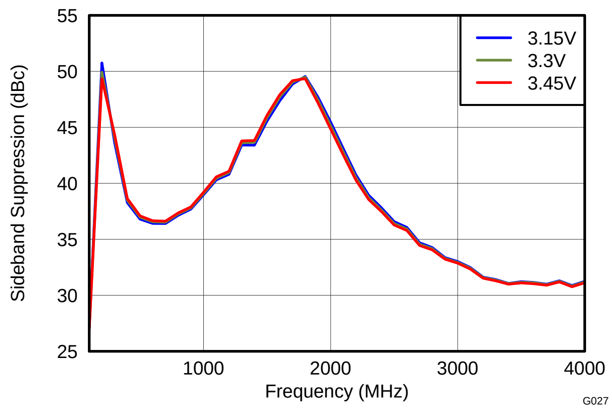


Figure 21. Unadjusted Sideband Suppression vs LO Frequency and Supply Voltage

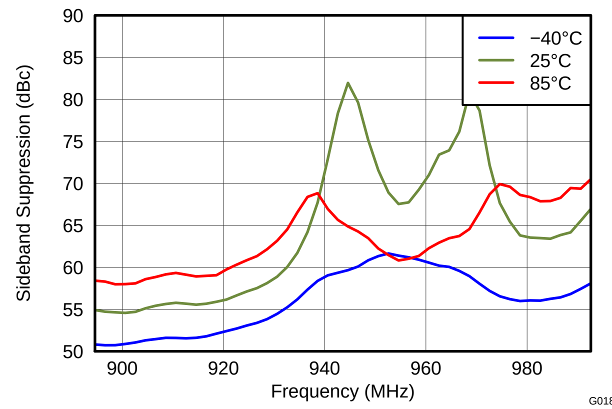


Figure 22. Adjusted Sideband Suppression vs LO Frequency and Temperature at 940 MHz

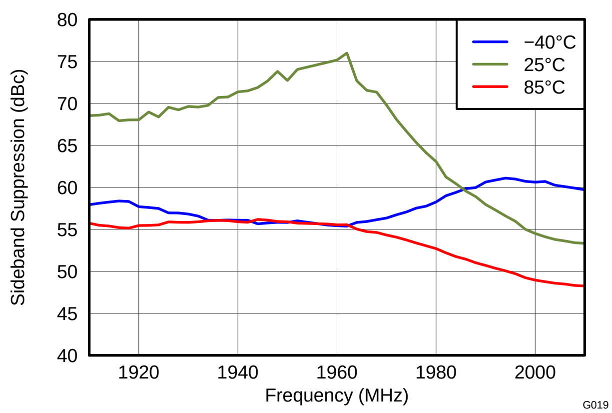


Figure 23. Adjusted Sideband Suppression vs LO Frequency and Temperature at 1960 MHz

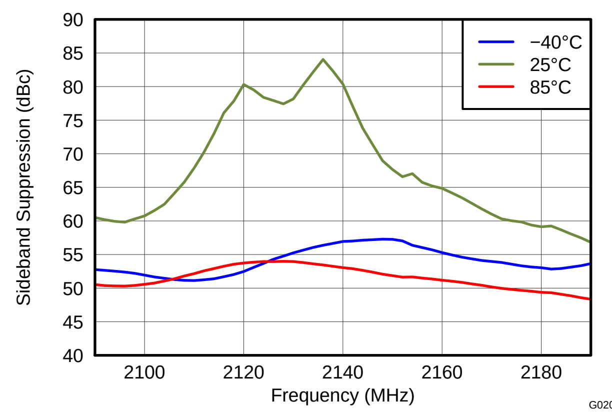


Figure 24. Adjusted Sideband Suppression vs LO Frequency and Temperature at 2140 MHz

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

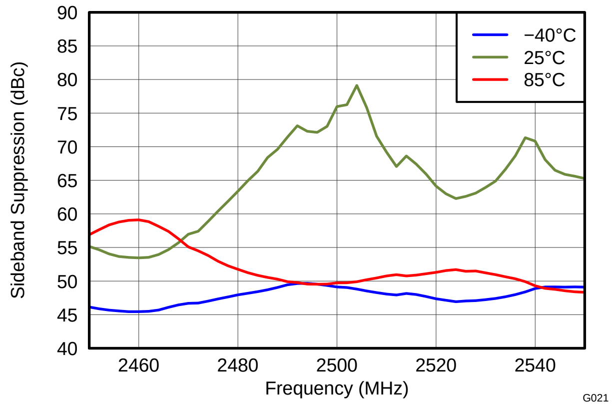


Figure 25. Adjusted Sideband Suppression vs LO Frequency and Temperature at 2500 MHz

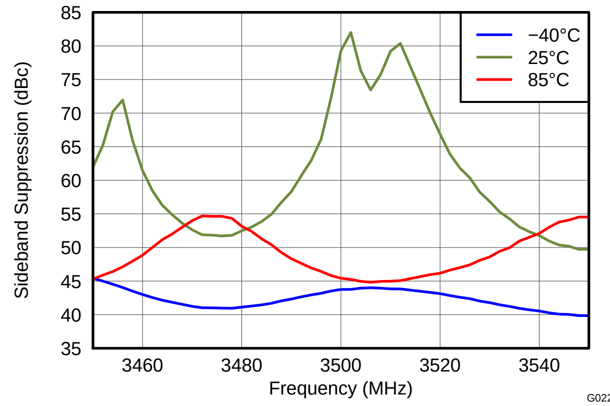


Figure 26. Adjusted Sideband Suppression vs LO Frequency and Temperature at 3500 MHz

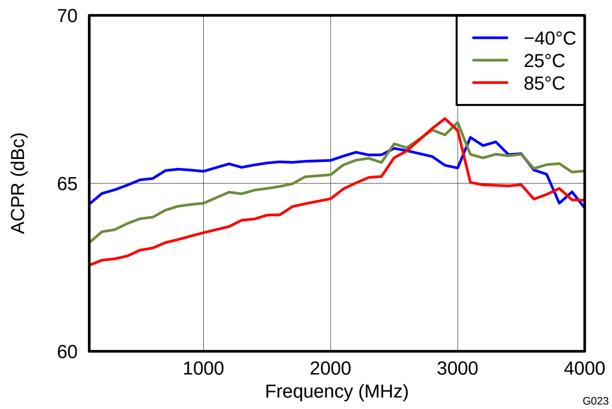


Figure 27. WCDMA Adjacent-Channel Power Ratio (ACPR) vs Temperature

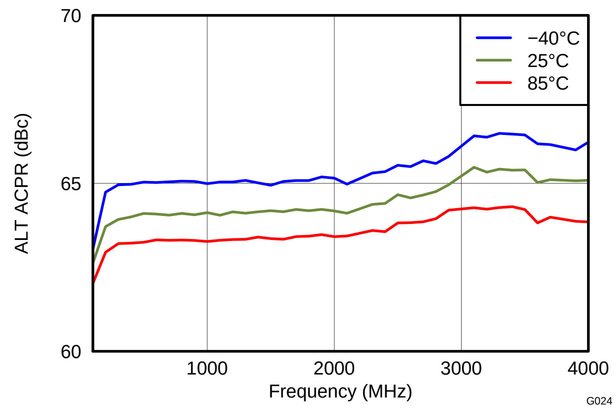


Figure 28. WCDMA Adjacent-Channel Power Ratio (Alt-ACPR) vs Temperature

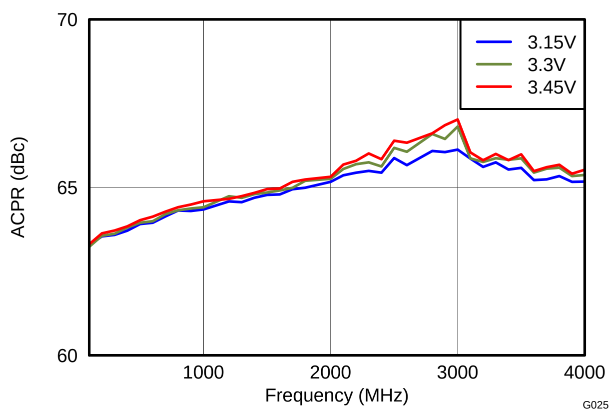


Figure 29. WCDMA Adjacent-Channel Power Ratio (ACPR) vs Supply Voltage

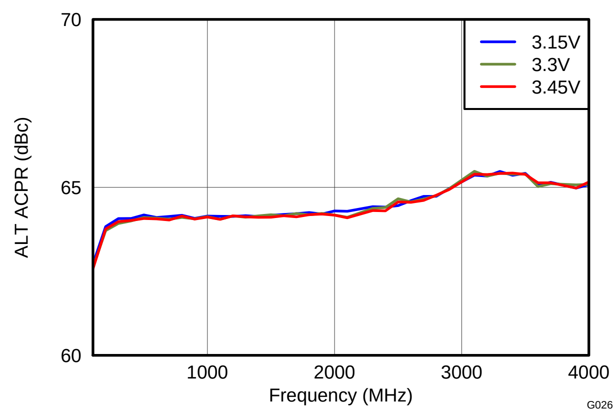


Figure 30. WCDMA Adjacent-Channel Power Ratio (Alt-ACPR) vs Supply Voltage

TYPICAL PERFORMANCE PLOTS (continued)

T_A = 25°C, DAC sampling rate = 65 MSPS, single-tone IF = 1.1 MHz, two-tone IF = 1 MHz and 2 MHz, DVDD18 = 1.8 V, CLKVDD18 = 1.8 V, DACVDD18 = 1.8 V, FUSEVDD18 = 1.8 V, IOVDD = 3.3 V, DACVDD33 = 3.3 V, MODVDD33 = 3.3 V, analog output, unless otherwise noted

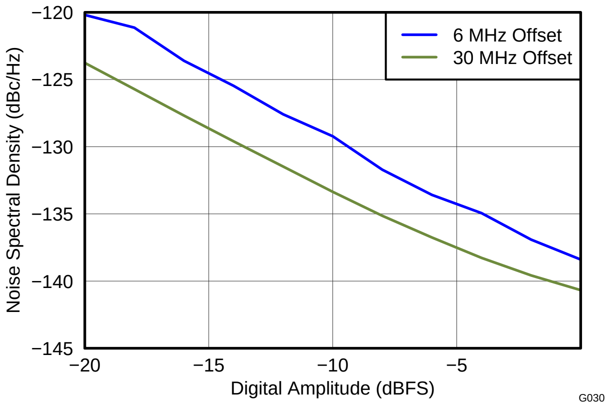


Figure 31. Noise Spectral Density (NSD) vs Input Power and LO Frequency

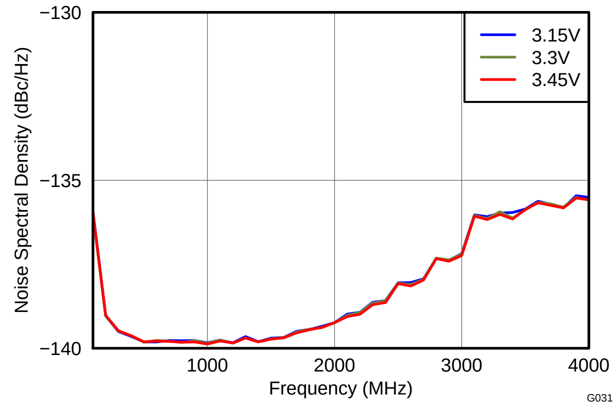


Figure 32. Noise Spectral Density (NSD) at 6-MHz Offset vs LO Frequency and Supply Voltage

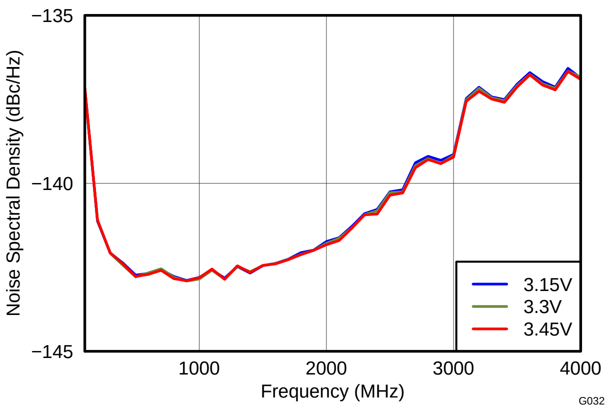


Figure 33. Noise Spectral Density (NSD) at 30-MHz Offset vs LO Frequency and Supply Voltage

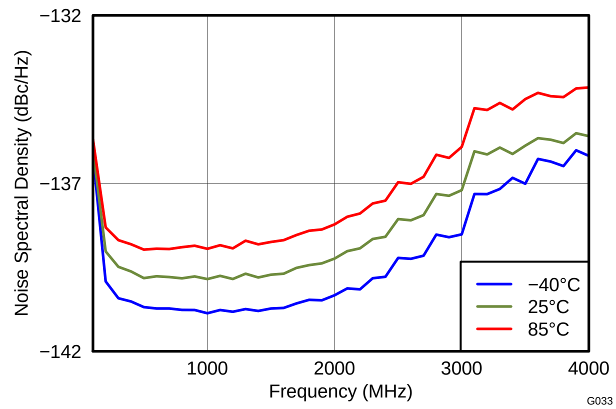


Figure 34. Noise Spectral Density (NSD) at 6-MHz Offset vs LO Frequency and Temperature

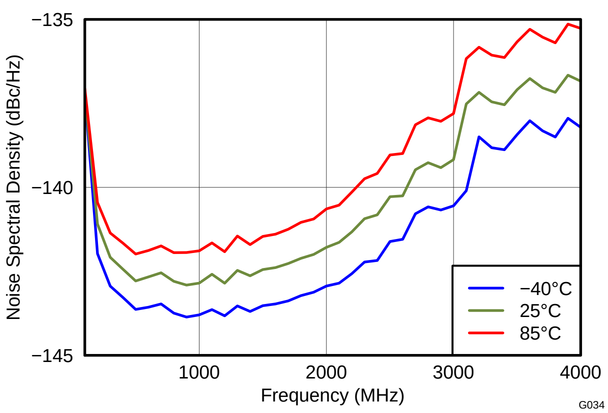


Figure 35. Noise Spectral Density (NSD) at 30-MHz Offset vs. LO Frequency and Temperature

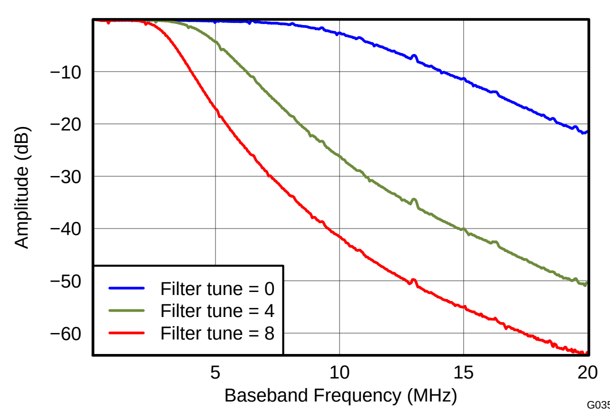


Figure 36. Baseband Filter Response

SERIAL INTERFACE

The serial port of the AFE7071 is a flexible serial interface which communicates with industry-standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of the AFE7071. The serial port is compatible with most synchronous transfer formats and can be configured as a 3- or 4-pin interface by **sif_4pin** in **CONFIG3 (bit6)**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For the 3-pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For the 4-pin configuration, **SDIO** is data-in only and **ALARM_SDO** is data-out only. Data is input into the device with the rising edge of **SCLK**. Data is output from the device on the falling edge of **SCLK.**

Each read/write operation is framed by signal **SDENB** (serial data-enable bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle, which identifies the following data transfer cycle as read or write, how many bytes to transfer, and the address to which to transfer the data. Table 1 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 through 5 comprise the data transfer cycle.

Table 1. Instruction Byte of the Serial Interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W — Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from the AFE7071, and a low indicates a write operation to the AFE7071.

[N1 : N0] — Identifies the number of data bytes to be transferred, as listed in Table 2. Data is transferred MSB first.

Table 2. Number of Transferred Bytes Within One Communication Frame

N1	N0	DESCRIPTION
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

[A4 : A0] — Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the AFE7071 MSB first and counts down for each byte.

Figure 37 shows the serial interface timing diagram for an AFE7071 write operation. **SCLK** is the serial interface clock input to AFE7071. Serial data enable **SDENB** is an active-low input to the AFE7071. **SDIO** is serial data in. Input data to the AFE7071 is clocked on the rising edges of **SCLK**.

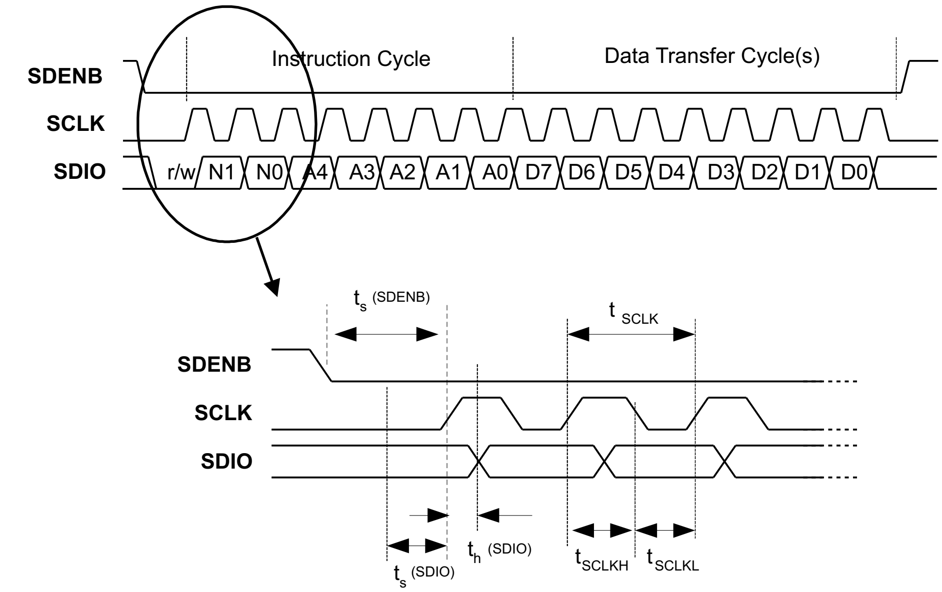


Figure 37. Serial Interface Write Timing Diagram

Figure 38 shows the serial interface timing diagram for an AFE7071 read operation. **SCLK** is the serial interface clock input to AFE7071. Serial data enable **SDENB** is an active-low input to the AFE7071. **SDIO** is serial data-in during the instruction cycle. In the 3-pin configuration, **SDIO** is data-out from the AFE7071 during the data transfer cycle(s), while **ALARM_SDO** is in a high-impedance state. In the 4-pin configuration, **ALARM_SDO** is data-out from the AFE7071 during the data transfer cycle(s). At the end of the data transfer, **ALARM_SDO** outputs low on the final falling edge of **SCLK** until the rising edge of **SDENB**, when it enters the high-impedance state.

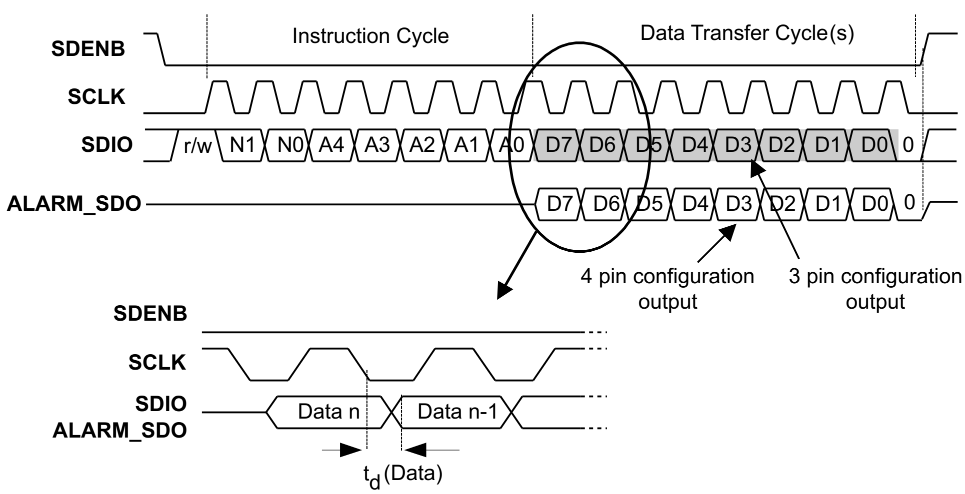


Figure 38. Serial Interface Read Timing Diagram

REGISTER DESCRIPTIONS

In the SIF interface there are three types of registers, *NORMAL, READ_ONLY*, and *WRITE_TO_CLEAR*. The *NORMAL* register type allows data to be written and read from the register. All 8 bits of the data are registered at the same time, but there is no synchronizing with an internal clock. All register writes are asynchronous with respect to internal clocks. *READ_ONLY* registers only allow reading of the registers—writing to them has no effect. *WRITE_TO_CLEAR* registers are just like *NORMAL* registers in that they can be written and read; however, when the internal signals set a bit high in these registers, that bit stays high until it is written to 0. This way, interrupts are captured and constant until dealt with and cleared.

Register Map

Name	Address	Default	(MSB) bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	(LSB) bit 0
CONFIG0	0x00	0x10	div2_dacclk_ena	div2_sync_ena	clkio_sel	clkio_out_ena_n	data_clk_sel	Reserved	fifo_ena	sync_IorQ
CONFIG1	0x01	0x10	twos	iqswap	Reserved		daca_ complement	dacb_ complement	Reserved	
CONFIG2	0x02	0xXX	Unused	Unused	Unused	Unused	Unused	Unused	Alarm_fifo_ 2away	Alarm_fifo_1away
CONFIG3	0x03	0x10	alarm_or_sdo_ ena	sif_4pin	SLEEP	TXENABLE	SYNC	sync_sleep_txenable_sel		msb_out
CONFIG4	0x04	0x0F	fuse_pd	Reserved	pd_clkrcvr	pd_clkrcvr_ mask	coarse_dac(3:0)			
CONFIG5	0x05	0x00	offset_ena	qmc_corr_ena	Reserved	filter_tune(4:0)				
CONFIG6	0x06	0x00	Reserved	pd_rf_out	pd_dac	pd_analogout	Reserved	pd_tf_out_ mask	pd_dac_mask	pd_analogout_ mask
CONFIG7	0x07	0x13	mask_2away	mask_1away	fifo_sync_mask	fifo_offset	alarm2away_ ena			alarm_1away_ ena
CONFIG8	0x08	0x00	qmc_offseta (7:0)							
CONFIG9	0x09	0x7A	qmc_offsetb (7:0)							
CONFIG10	0x0A	0xB6	qmc_offseta(12:8)					Unused	Unused	Unused
CONFIG11	0x0B	0xEA	qmc_offsetb(12:8)					Unused	Unused	Unused
CONFIG12	0x0C	0x45	qmc_gaina (7:0)							
CONFIG13	0x0D	0x1A	qmc_gainb (7:0)							
CONFIG14	0x0E	0x16	qmc_phase (7:0)							
CONFIG15	0x0F	0xAA	qmc_phase(9:8)		qmc_gaini(10:8)			qmc_gainq(10:8)		
CONFIG16	0x10	0xC6	Reserved							
CONFIG17	0x11	0x24	Reserved							
CONFIG18	0x12	0x02	Reserved							
CONFIG19	0x13	0x00	Reserved							
CONFIG20	0x14	0x00	Reserved							
CONFIG21	0x15	0x00	Reserved							
CONFIG22	0x16	0x00	Reserved							
CONFIG23	0x17	0xXX	Reserved							
CONFIG24	0x18	0xXX	Reserved							
CONFIG25	0x19	0xXX	Reserved							
CONFIG26	0x1A	0xXX	Reserved							
CONFIG27	0x1B	0xXX	Reserved							
CONFIG28	0x1C	0xXX	Reserved							
CONFIG29	0x1D	0xXX	Reserved							
CONFIG30	0x1E	0xXX	Reserved							
CONFIG31	0x1F	0x82	titest_voh	titest_vol	Version(5:0)					

Register name: CONFIG0; Address: 0x00

BIT 7							BIT 0
div2_dacclk_ena	div2_sync_ena	clkio_sel	clkio_out_ena_n	data_clk_sel	Reserved	fifo_ena	sync_IorQ
0	0	0	1	0	0	0	0

Table 3. Clock Mode Memory Programming

Mode	div2_dacclk_ena	div2_sync_ena	clkio_sel	clkio_out_ena_n	data_clk_sel
Dual input clock(00)	1	0	1	1	0
Dual output clock (01)	1	1	0	0	0
Single differential DDR clock (10)	0	0	0	1	1
Single differential SDR clock (11)	0	0	1	1	1

div2_dacclk_ena: When set to 1, this enables the divide-by-2 in the DAC clock path. This must be set to 1 when in dual-input clock mode or dual-output clock mode.

div2_sync_ena: When set to 1, the divide-by-2 is synchronized with the iq_flag. It is only useful in the dual-clock modes when the divide-by-2 is enabled. Care must be take to ensure the input data and DAC clocks are correctly aligned.

clkio_sel: This bit is used to determine which clock is used to latch the input data. This should be set according to Table 3.

clkio_out_ena_n: When set to 0, the clock CLK_IO is an output. Depending on the mode, is should be set according to Table 3.

data_clk_sel: This bit is used to determine which clock is used to latch the input data. This should be set according to Table 3.

fifo_ena: When asserted, the FIFO is enabled. Used in dual-input clock mode only. In all other modes, the FIFO is bypassed.

sync_IorQ: When set to 0, sync is latched on the I phase of the input clock. When set to 1, sync is detected on the Q phase of the clock and is sent to the rest of the chip when the next I data is presented.

Register name: CONFIG1; Address: 0x01

BIT 7							BIT 0
twos	iqswap	Reserved		daca_complement	dacb_complement	Reserved	
0	0	0	1	0	0	X	X

twos:	When asserted, the input to the chip is 2s complement, otherwise offset binary.
iqswap:	When asserted, the DACA data is driven onto DACB and reverse.
daca_complement:	When asserted, the output to DACA is complemented. This allows the user of the chip effectively to change the + and – designations of the PADs.
dacb_complement:	When asserted, the output to DACB is complemented. This allows the user of the chip effectively to change the + and – designations of the PADs.

Register name: CONFIG2; Address: 0x02
Write-to-clear register bits remain asserted once set. Each bit must be written to 0 before another 1 can be captured.

BIT 7							BIT 0
Unused	Unused	Unused	Unused	Unused	Unused	Alarm_fifo_2away	Alarm_fifo_1away
0	0	0	0	0	0	1	1

Alarm_fifo_2away: When asserted, the FIFO pointers are 2 away from collision. **(WRITE_TO_CLEAR)**

Alarm_fifo_1away: When asserted, the FIFO pointers are 1 away from collision. **(WRITE_TO_CLEAR)**

Register name: CONFIG3; Address: 0x03 (INTERFACE SELECTION)

BIT 7							BIT 0
alarm_or_sdo_ena	sif_4pin	SLEEP	TXenable	SYNC	sync_sleep_txenable_sel		msb_out
0	0	0	1	0	0	0	0

alarm_or_sdo_ena: When asserted, the output of the ALARM_SDO pin is enabled.

sif_4pin: When asserted, the part is in 4-pin SPI mode. The data-out is output on the ALARM_SDO pin. If this bit is not enabled, the alarm signal is output on the ALARM_SDO pin.

sleep: When asserted, all blocks programmed to go to sleep in CONFIG4 and CONFIG6 registers labeled pd_***_mask are powered down.

TXenable: When 0, the data path is zeroed. When 1, the device transmits.

sync: When written with a 1, the part is synced. To be resynced using the sif register, it must be reset to 0 by writing a 0 then write a 1 to the sif to sync.

sync_sleep_txenable_sel: This is used to define the function of the SYNC_SLEEP pin. This pin can be used for multiple functions, but only one at a time. When it is set to control any one of the functions, all other functions are controlled by writing their respective sif register bits.

sync_sleep_txenable_sel	Pin controls
00	All controlled by sif bit
01	TXENABLE
10	SYNC
11	SLEEP

msb_out: When set, and alarm_sdo_out_ena is also set, the ALARM_SDO pin outputs the value of daca bit 13.

Register name: CONFIG4; Address: 0x04

BIT 7							BIT 0
fuse_pd	Reserved	pd_clkrcvr	pd_clkrcvr_mask	coarse_dac(3:0)			
0	0	0	0	1	1	1	1

fuse_pd: When set to 1, the fuses are powered down. This saves approximately 50 µA at 1.8 V for every intact fuse. The default value is 0.

pd_clkrcvr: When asserted, the clock receiver is powered down.

pd_clkrcvr_mask: When asserted, allows the clock receiver to be powered down with the SYNC_SLEEP pin or sleep register bit.

coarse_dac: DAC full-scale current control

Register name: CONFIG5; Address: 0x05

BIT 7							BIT 0
offset_ena	qmc_corr_ena	Reserved	filter_tune(4:0)				
0	0	0	0	0	0	0	0

offset_ena: When asserted, the qmc offset blk is enabled.

qmc_corr_ena: When asserted, the qmc correction is enabled.

filter_tune(4:0): Bits used to change the bandwidth of the analog filters

Register name: CONFIG6; Address: 0x06

BIT 7							BIT 0
pd_lvds	pd_rf_out	pd_dac	pd_analogout	Reserved	pd_tf_out_mask	pd_dac_mask	pd_analogout_ mask
0	0	0	1	1	1	0	0

pd_lvds: Powers down the LVDS output circuit (not connected on AFE7071). Assert to save 12 mA on the MODVDD18 supply

pd_rf_out: When asserted, the RF output is powered down.

pd_dac: When asserted, DACs are powered down.

pd_analog_out: When asserted, the RF analog output is powered down.

The following are used to determine what blocks are powered down when the SYNC_SLEEP pin is used or the sleep register bit is set.

pd_rf_out_mask: When asserted, allows the RF output to be powered down

pd_dac_mask: When asserted, allows the DACs to be powered down

Register name: CONFIG7; Address: 0x07

BIT 7							BIT 0
mask_2away	mask_1away	fifo_sync_mask	fifo_offset			alarm_2away_ena	alarm_1away_ena
0	0	0	1	0	0	1	1

mask_2away: When set to 1, the ALARM_SDO pin is not asserted when the FIFO pointers are 2 away from collision. The alarm still shows up in the CONFIG7 bits.

mask_1away: When set to 1, the ALARM_SDO pin is not asserted when the FIFO pointers are 1 away from collision. The alarm still shows up in the CONFIG7 bits.

fifo_sync_mask: When set to 1, the sync to the FIFO is masked off. Sync does not then reset the pointers. If the value is 0, when the sync is toggled the FIFO pointers are reset to the offset values.

fifo_offset: Used to set the offset pointers in the FIFO. Programs the starting location of the output side of the FIFO, allows the output pointer to be shifted from –4 to +3 (2s complement) positions with respect to its default position when synced. The default position for the output side pointer is 2. The input side pointer defaults to 0.

alarm_2away_ena: When asserted, alarms from the FIFO that represent the pointers being 2 away from collision are enabled.

alarm_1away_ena: When asserted, alarms from the FIFO that represent the pointers being 1 away from collision are enabled.

Register name: CONFIG8; Address: 0x08

BIT 7							BIT 0
qmc_offseta (7:0)							
0	0	0	0	0	0	0	0

qmc_offseta(7:0): Bits 7:0 of qmc_offseta. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG9; Address: 0x09

BIT 7							BIT 0
qmc_offsetb (7:0)							
0	1	1	1	1	0	1	0

qmc_offsetb(7:0): Bits 7:0 of qmc_offsetb. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG10; Address: 0x0A

BIT 7							BIT 0
qmc_offseta(12:8)					Unused	Unused	Unused
1	0	1	1	0	1	1	0

qmc_offsetb(12:8): Bits 12:8 of qmc_offseta. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG11; Address: 0x0B

BIT 7							BIT 0
qmc_offsetb(12:8)					Unused	Unused	Unused
1	1	1	0	1	0	1	0

qmc_offsetb(12:8): Bits 12:8 of qmc_offsetb. The complete registers qmc_offseta[12:0] and qmc_offsetb[12:0] are updated when CONFIG8 is written, so CONFIG9, CONFIG10, and CONFIG11 should be written before CONFIG8.

Register name: CONFIG12; Address: 0x0C

BIT 7							BIT 0
qmc_gaina (7:0)							
0	1	0	0	0	1	0	1

qmc_gaina(7:0): Bits 7:0 of qmc_gaina. The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG13; Address: 0x0D

BIT 7							BIT 0
qmc_gainb (7:0)							
0	0	0	1	1	0	0	0

qmc_gainb(7:0): Bits 7:0 of qmc_gainb. The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG14; Address: 0x0E

BIT 7							BIT 0
qmc_phase (7:0)							
0	0	0	1	0	1	1	0

qmc_phase(7:0) Bits 7:0 of qmc_phase. The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG15; Address: 0x0F

BIT 7							BIT 0
qmc_phase(9:8)		qmc_gaina(10:8)			qmc_gainb(10:8)		
1	0	1	0	1	0	1	0

qmc_phase(9:8): Bits 9:8 of qmc_phase value

qmc_gaina(10:8): Bits 9:8 of qmc_gaina value

qmc_gainb(10:8): Bits 9:8 of qmc_gainb value

The complete registers qmc_gaina[10:0], qmc_gainb[10:0] and qmc_phase[9:0] are updated when CONFIG12 is written, so CONFIG13, CONFIG14, and CONFIG15 should be written before CONFIG12.

Register name: CONFIG16; Address: 0x10

BIT 7							BIT 0
Reserved							
1	1	0	0	0	1	1	0

Register name: CONFIG17; Address: 0x11

BIT 7							BIT 0
Reserved							
0	0	1	0	0	1	0	0

Register name: CONFIG18; Address: 0x12

BIT 7							BIT 0
Reserved							
0	0	0	0	0	0	1	0

Register name: CONFIG19; Address: 0x13

BIT 7							BIT 0
Reserved							
0	0	0	0	0	0	0	0

Register name: CONFIG20; Address: 0x14

BIT 7							BIT 0
Reserved							
0	0	0	0	0	0	0	0

Register name: CONFIG21; Address: 0x15

BIT 7							BIT 0
Reserved							
0	0	0	0	0	0	0	0

Register name: CONFIG22; Address: 0x16

BIT 7							BIT 0
Reserved							
0	0	0	0	0	0	0	0

Register name: CONFIG23; Address: 0x17

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG24; Address: 0x18

BIT 7							BIT 0
reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG25; Address: 0x19

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG26; Address: 0x1A

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG27; Address: 0x1B

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG28; Address: 0x1C

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG29; Address: 0x1D

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG30; Address: 0x1E

BIT 7							BIT 0
Reserved – Varies from device to device							
X	X	X	X	X	X	X	X

Register name: CONFIG31; Address: 0x1F

BIT 7							BIT 0
titest_voh	titest_vol	Version(5:0)					
1	0	0	0	0	0	1	0

titest_voh:	Bit held high for sif test purposes
titest_voh:	Bit held low for sif test purposes
version:	Version of the chip

PARALLEL DATA INPUT

The AFE7071 input is either complex I and Q data interleaved on D[13:0] at a data rate 2× the internal output sample clock frequency.

CLOCK MODES

The AFE7071 has three clock modes for providing the DAC sample clock and data latching clocks.

Clock Mode	CLK_IO	FIFO	DataLatch	DACCLKFreqRatio	DataFormat	Progamming Bits
Dual-input clock	Input	Enabled	CLK_IO	1× or 2× internal sample clock	IQ or phase (MSB/LSB)	See Table 3 in CONFIG0 decription.
Dual-output clock	Output	Disabled	CLK_IO	2× internal sample clock	IQ or phase (MSB/LSB)	
Single differential DDR clock	Disabled	Disabled	DACCLK	1× internal sample clock	IQ or phase (MSB/LSB)	

DUAL-INPUT CLOCK MODE

In dual-input clock mode, the user provides both a differential DAC clock at pins DACCLKP/N at 2× the internal sample clock frequency and a second single-ended CMOS-level clock at CLK_IO for latching input data. The DACCLK is divided by 2 internally to provide the internal output sample clock, with the phase determined by the IQ_FLAG input. The IQ_FLAG signal can either be a repetitive high/low signal or a single event that is used to reset the clock divider phase and identify the I sample.

CLK_IO is an SDR clock at the input data rate, or 2× the internal sample-clock frequency. The DAC clock and data clock must be frequency locked, and a FIFO is used internally to absorb the phase difference between the two clock domains. The phase relationship of CLK_IO and DACCLK can be any phase at the initial sync of the FIFO, and thereafter can move up to ±4 clock cycles before the FIFO input and output pointers overrun and cause data errors. In dual-input clock mode, the latency from input data to output samples is not controlled because the FIFO can introduce a one-clock cycle variation in latency, depending on the exact phase relationship between DACCLK and CLK_IO.

An external sync must be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks. Because the internal processing blocks process I and Q in parallel, the user can provide the sync signal during either the I or Q input times (or both). Note that the internal sync signal must propagate through the input FIFO, and therefore the latency of the sync updates of the signal processing blocks is not controlled.

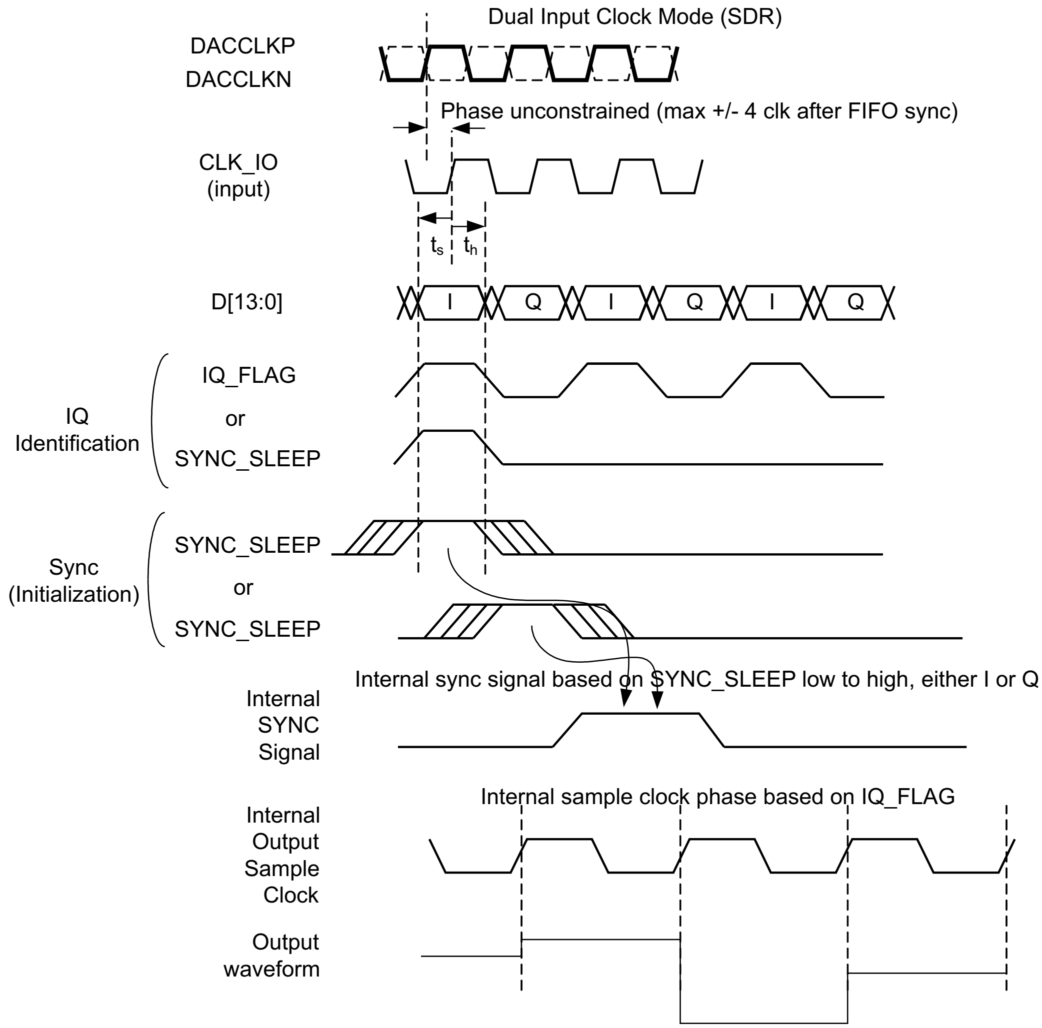


Figure 39. Dual-Input Clock Mode

DUAL-OUTPUT CLOCK MODE

In dual-output clock mode, the user provides a differential DAC clock at pins DACCLKP/N at 2× the internal sample clock frequency. The DACCLK is divided by 2 internally to provide the internal output sample clock, with the phase determined by the IQ_FLAG input. The IQ_FLAG signal can either be a repetitive high/low signal or a single event that is used to reset the clock divider phase and identify the I sample.

The AFE7071 outputs a single-ended CMOS-level clock at CLK_IO for latching input data. CLK_IO is an SDR clock at the input data rate, or 2× the internal sample clock frequency. The CLK_IO clock can be used to drive the input data source (such as digital upconverter) that sends the data to the DAC. Note that the CLK_IO delay relative to the input DACCLK rising edge (t_d) in Figure 40) increases with increasing loads.

An external sync can be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks. Because the internal processing blocks process I and Q in parallel, the user can provide the sync signal during either the I or Q input times (or both).

In the dual-output clock mode, the FIFO is bypassed, so the latency from the data input to the DAC output and the time from sync input to update of the signal processing block are deterministic.

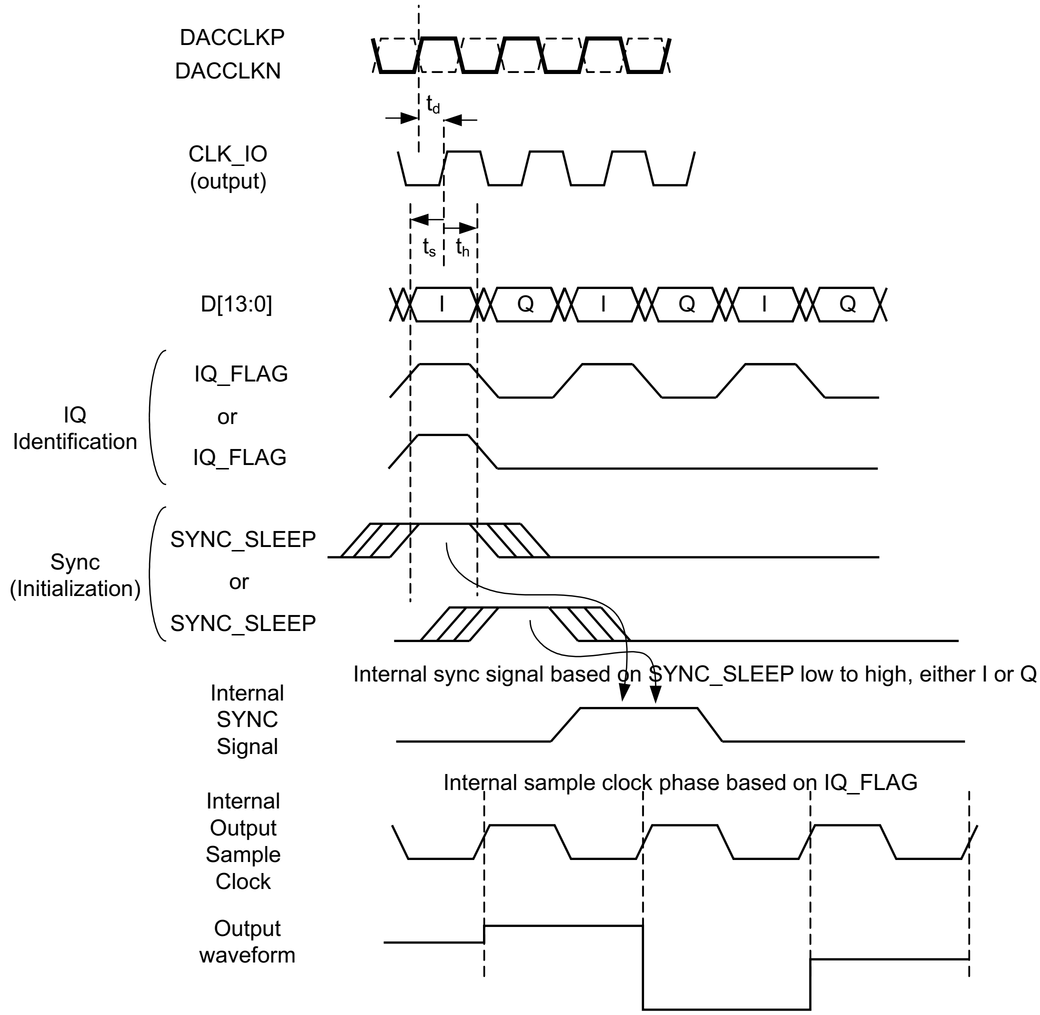


Figure 40. Dual-Output Clock Mode Timing Diagram

SINGLE DIFFERENTIAL DDR CLOCK

In single differential DDR clock mode, the user provides a differential clock to DACCLKP/N at the internal output sample clock frequency. The rising and falling edges of DACCLK are used to latch I and Q data, respectively. The internal output sample clock is derived from DACCLKP/N.

An external sync can be given on the SYNC_SLEEP pin to reset/initialize internal signal processing blocks. Because the internal processing blocks process I and Q in parallel, the user can provide the sync signal during either the I or Q input times (or both).

In the single differential DDR clock mode, the FIFO is bypassed, so the latency from the data input to the DAC output and the time from sync input to update of the signal processing block are deterministic.

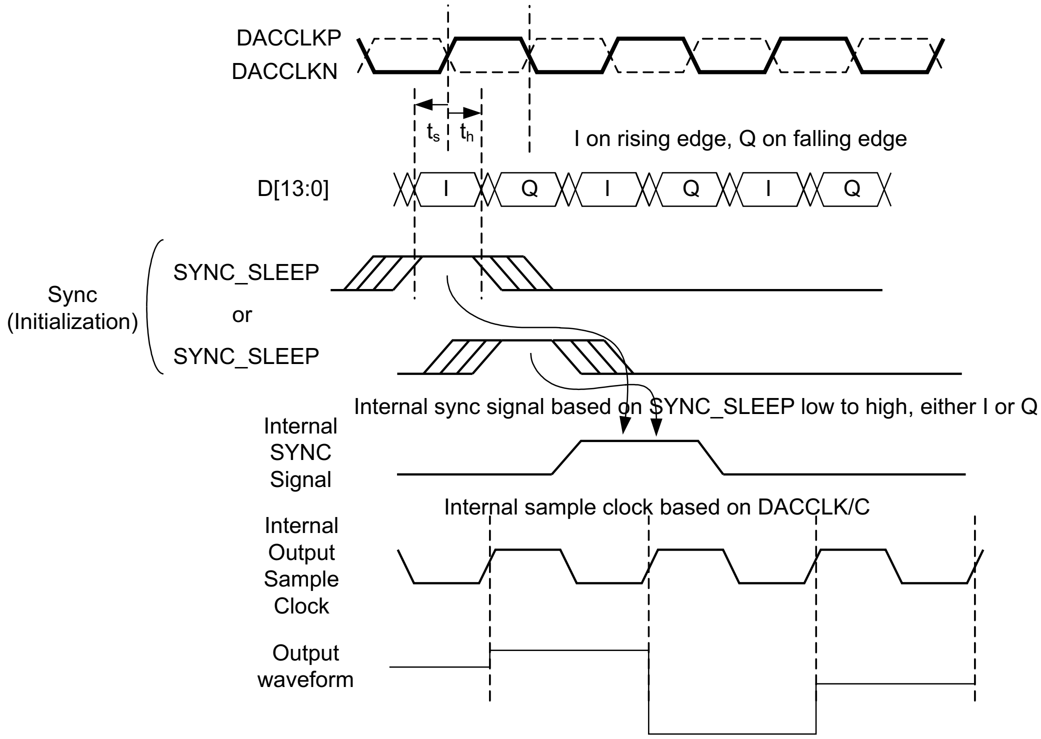


Figure 41. Single-Clock-Mode Timing Diagram

FIFO ALARMS

The FIFO only operates when the write and read pointers are positioned properly. If either pointer over- or under-runs the other, samples are duplicated or skipped. To prevent this, register CONFIG2 can be used to track two FIFO-related alarms:

- alarm_fifo_2away: Occurs when the pointers are within two addresses of each other
- alarm_fifo_1away: Occurs when the pointers are within one address of each other

These two alarm events are generated asynchronously with respect to the clocks and can be accessed through the ALARM_SDO pin by writing a 1 in register alarm_or_sdo_ena (CONFIG3[7]) and 0 in register sif_4pin (CONFIG3[6]).

QUADRATURE MODULATOR CORRECTION (QMC) BLOCK

The quadrature modulator correction (QMC) block provides a means for changing the phase balance of the complex signal to compensate for I and Q imbalance present in an analog quadrature modulator. The block diagram for the QMC block is shown in Figure 42. The QMC block contains three programmable parameters. Registers **qmc_gaina(10:0)** and **qmc_gainb(10:0)** control the I and Q path gains and are 11-bit values with a range of 0 to approximately 2.0. Register **qmc_phase(9:0)** controls the phase imbalance between I and Q and is a 10-bit value with a range of –1/8 to approximately +1/8. LO feedthrough can be minimized by adjusting the DAC offset feature described below.

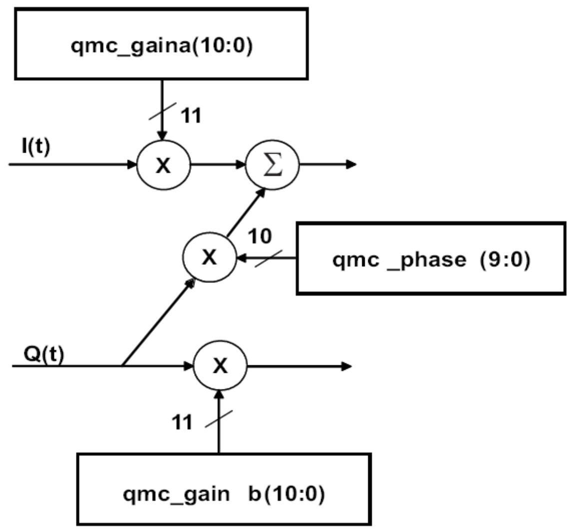


Figure 42. QMC Gain/Phase Block Diagram

The LO feedthrough can be minimized by adjusting the DAC offset. Registers **qmc_offseta(12:0)** and **qmc_offsetb(12:0)** control the I and Q path offsets and are 13-bit values with a range of –4096 to 4095. The DAC offset value adds a digital offset to the digital data before digital-to-analog conversion. The **qmc_gaina** and **qmc_gainb** registers can be used to back off the signal before the offset to prevent saturation when the offset value is added to the digital signal.

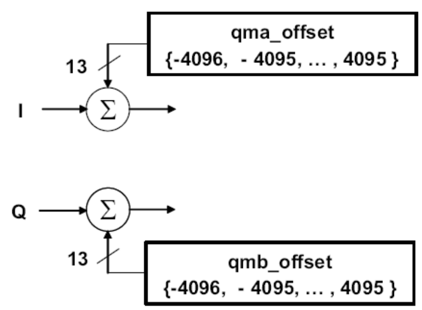


Figure 43. QMC Offset Block Diagram

REVISION HISTORY

Changes from Original (May 2012) to Revision A	Page
• Revised the Product Preview data sheet	1

Changes from Revision A (October 2012) to Revision B	Page
• Changed the device From: Product Preview To: Production data	1

Changes from Revision B (December 2012) to Revision C	Page
• Changed the TYP value of f_{LO} = 450 MHz, Analog Output noise floor From: 156 To: 143	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7071IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AFE7071I	Samples
AFE7071IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AFE7071I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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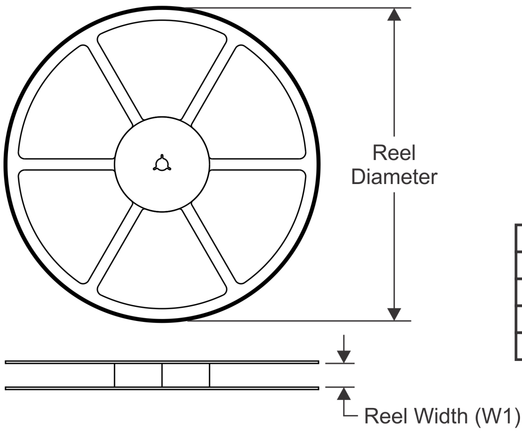
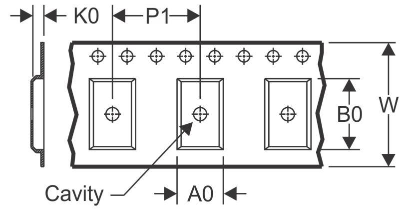
TAPE AND REEL INFORMATION

REEL DIMENSIONS

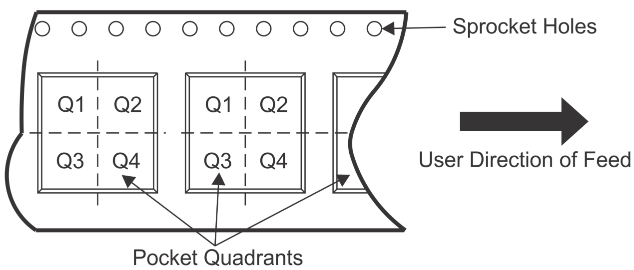


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

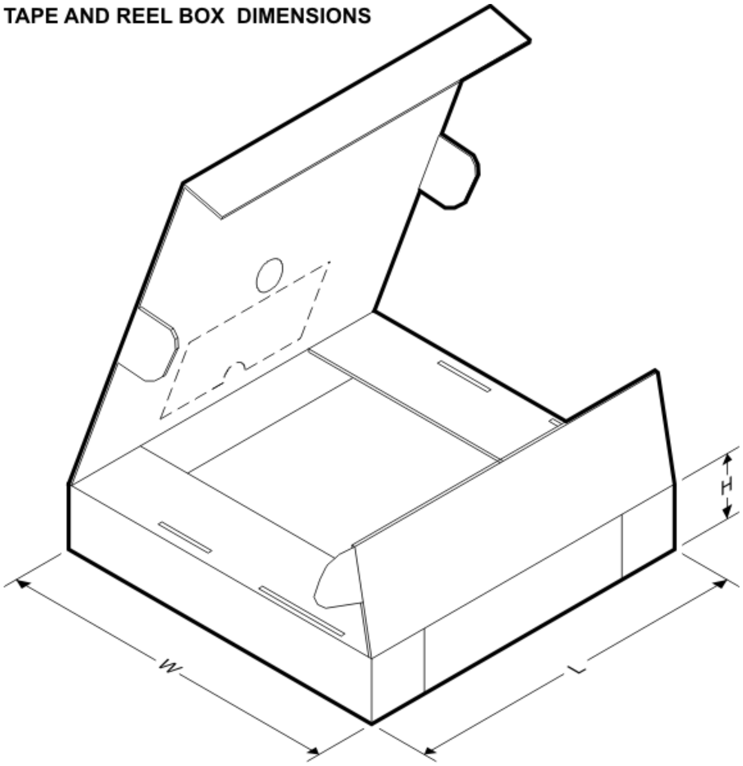
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE7071IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
AFE7071IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

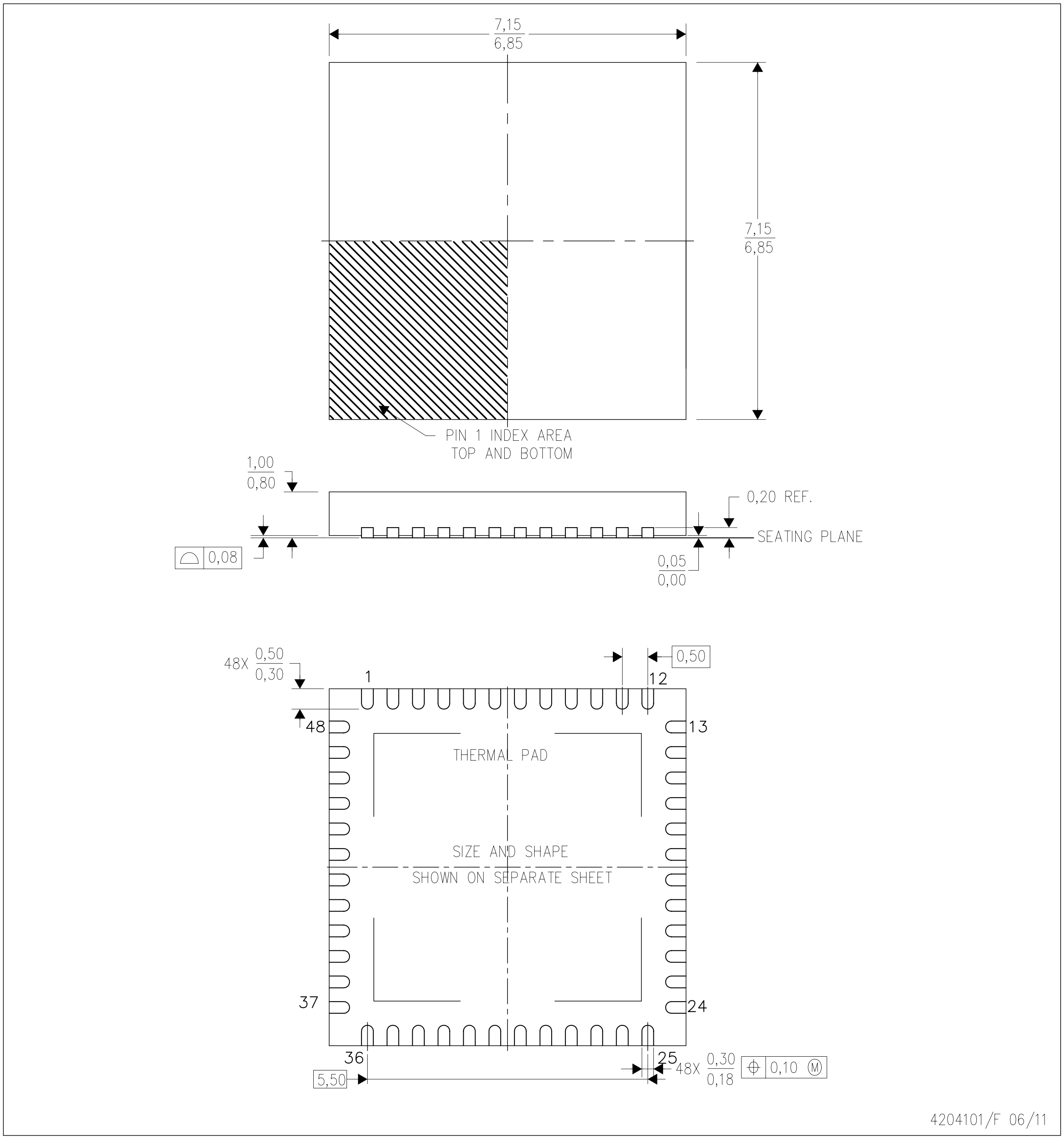
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE7071IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
AFE7071IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

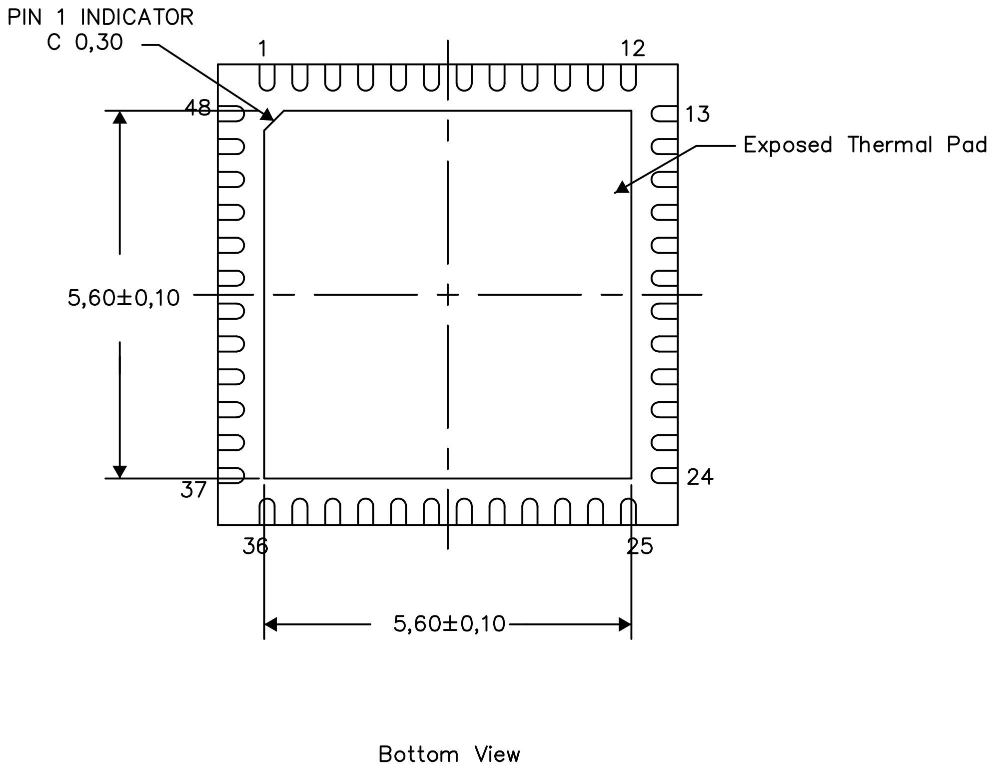
RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

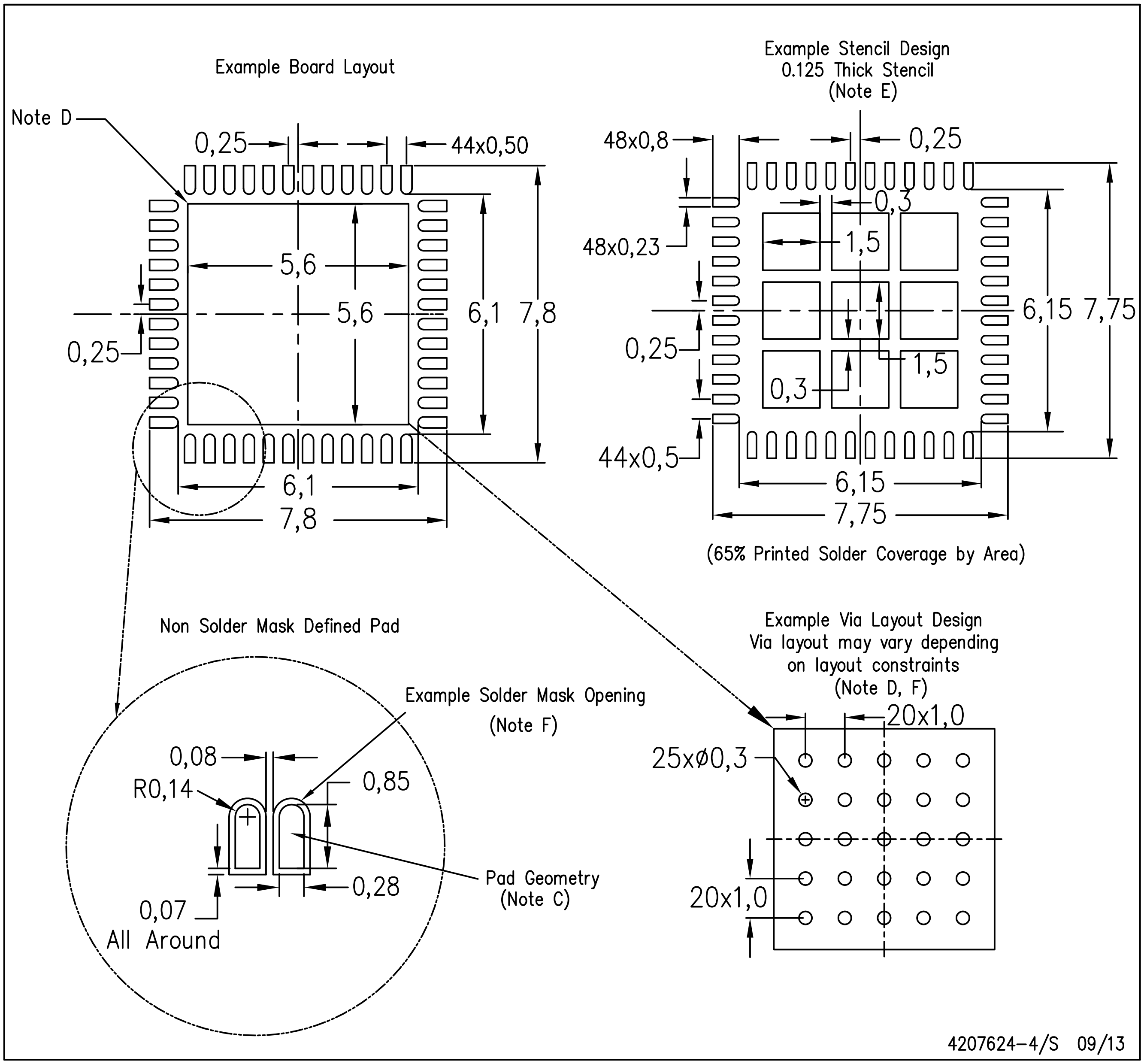


Exposed Thermal Pad Dimensions

4206354-5/W 09/13

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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