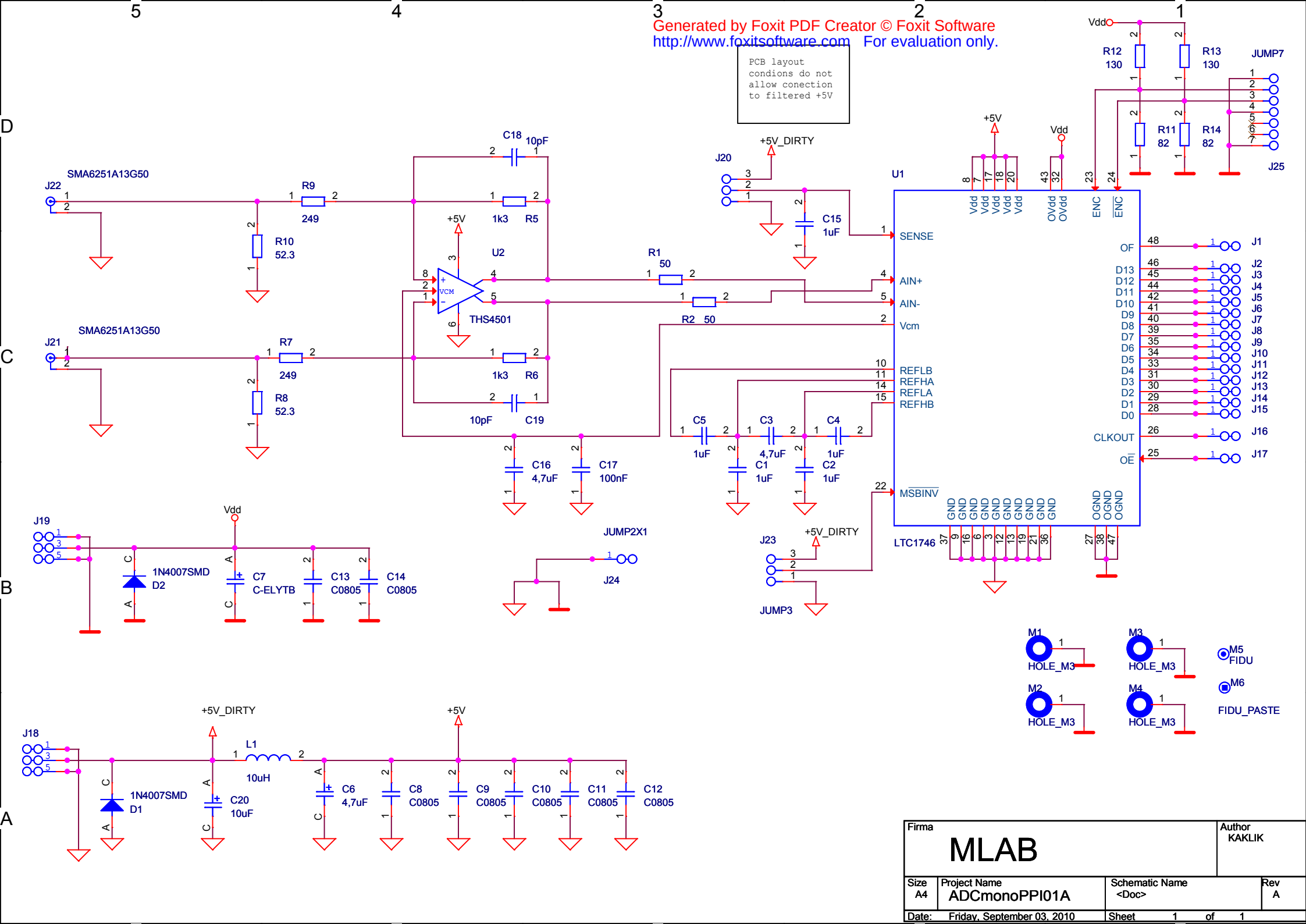
PCB layout condions do not allow conection to filtered +5V



Firma: MLAB			Author: KAKLIK
Size: A4	Project Name: ADCmonoPPI01A	Schematic Name: <Doc>	Rev: A
Date: Friday, September 03, 2010	Sheet 1 of 1		