

S3AN01A

XILINX Spartan 3AN
FPGA School Board

- 1.00 New Design
- 1.01 Typo Corrections and Errata
Verified in hardware

**Superseded by a new version
S3AN01B which is backwards
compatible and contains all
changes required by Errata.**

Errata

Pins 33 and 35 are Input Only and can not be used for LED output.

Cut wires PS2_CLK1 and PS2_DATA1 near to serial R (bellow Q10 and Q11)

Connect U1.12 with U1.35 - LED Display

Connect U1.13 with U1.33 - LED Display

Connect U1.130 with Q10.S - New connection for PS2_DATA1

Connect U1.127 with Q11.S - New connection for PS2_CLK1

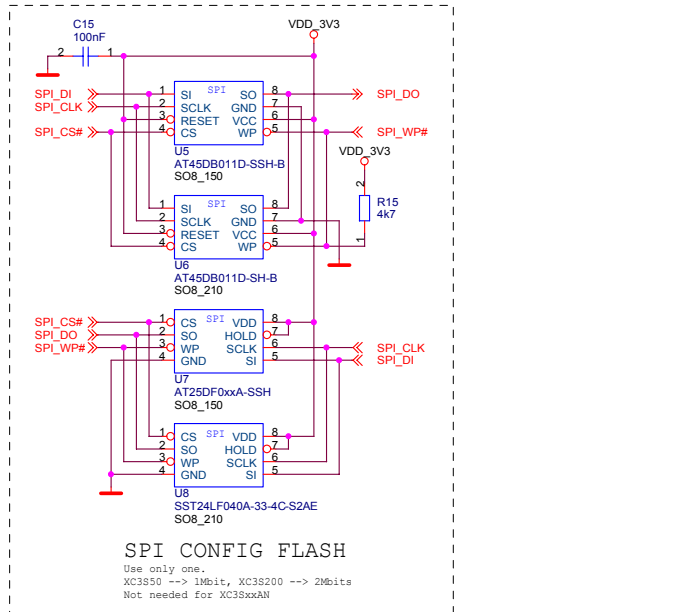
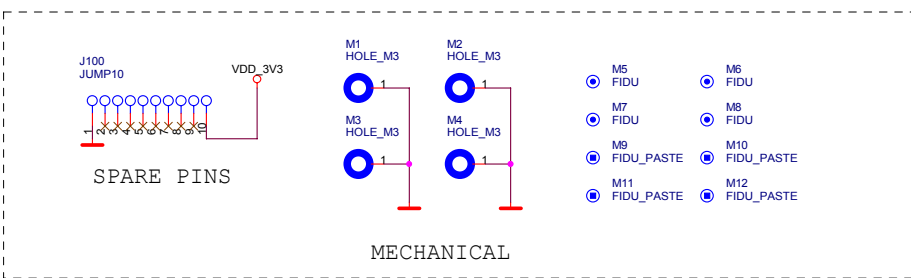
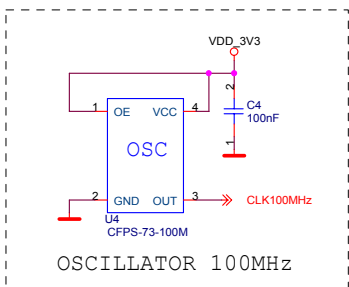
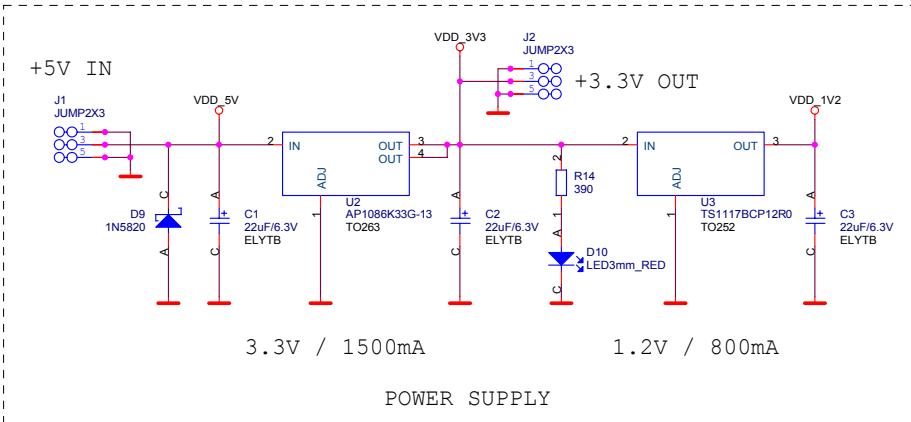
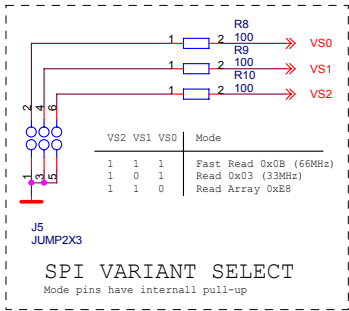
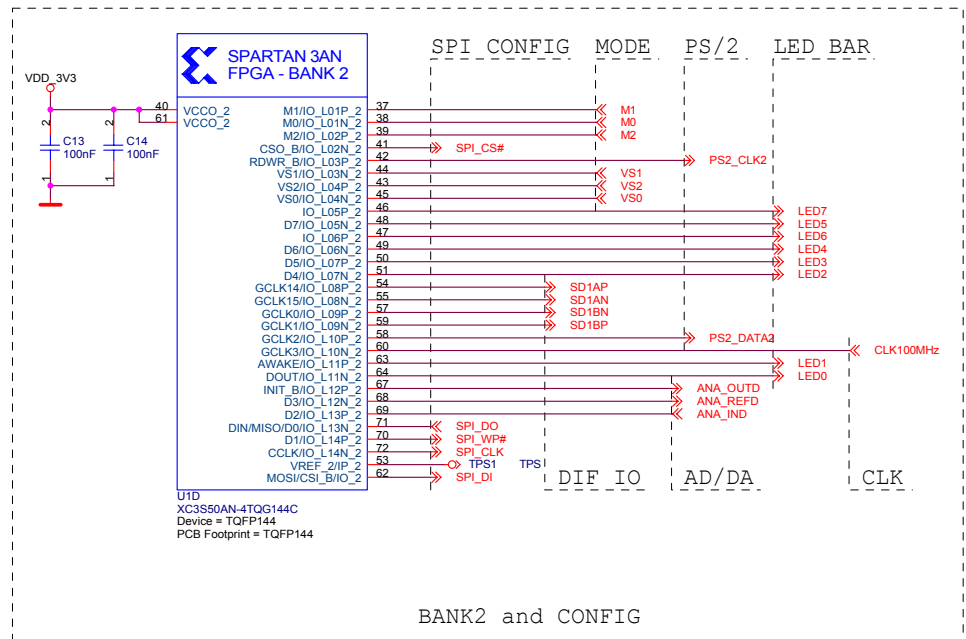
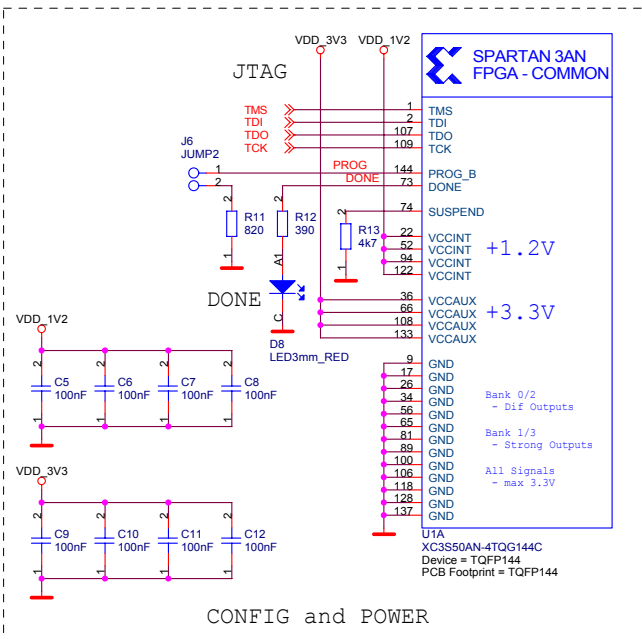
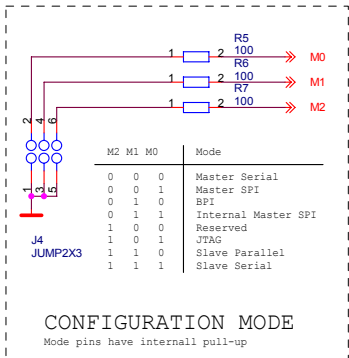
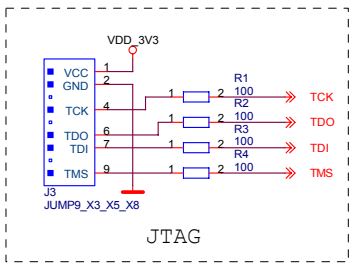
There are missing serial resistors for LED display.

Enable LED display segments for a short time only

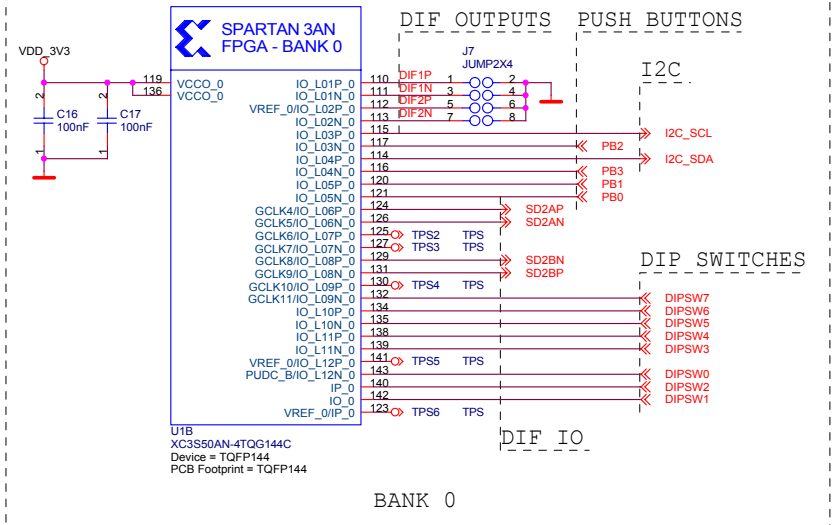
Identifiers B1_nn (port of bank 1) ends in '_' what is not valid
identifier in VHDL.

Use name "P" in VHDL and UCF.

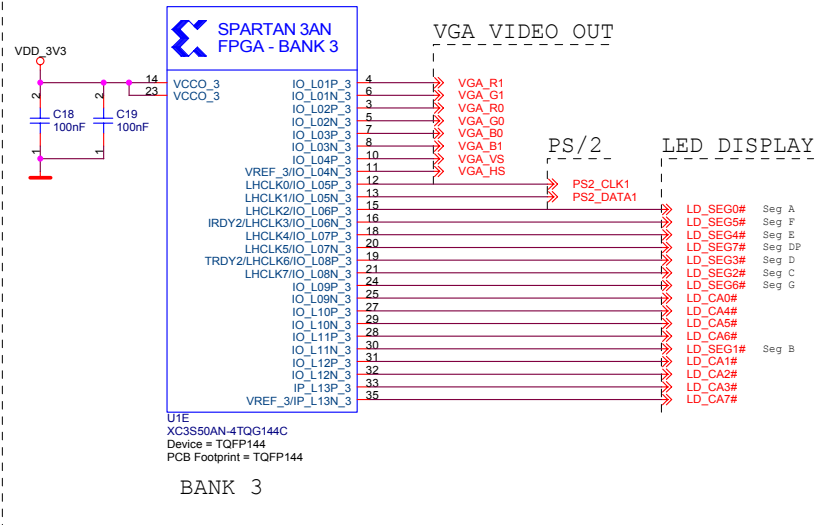
Firma		Author	
MLAB		MIHO	
Size	Project Name	Schematic Name	Rev
A3	MLAB	S3AN01A	1.01
Date:	Monday, March 21, 2011	Sheet	1 of 5



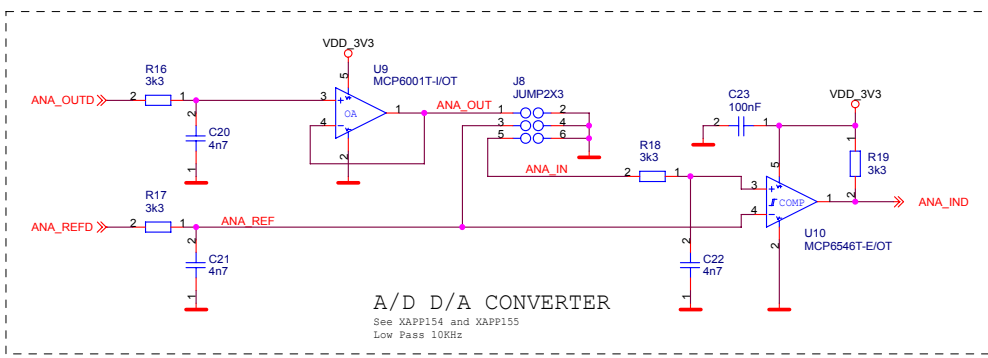
Firma MLAB		Author MIHO	
Size A3	Project Name MLAB	Schematic Name S3AN01A	Rev 1.01
Date: Monday, March 21, 2011	Sheet 2 of 5		



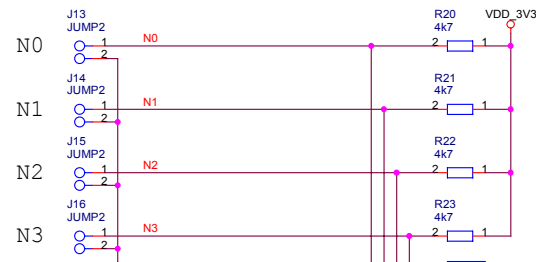
BANK 0



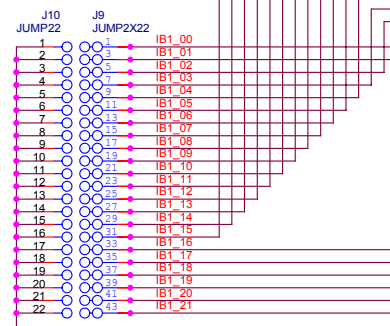
BANK 3



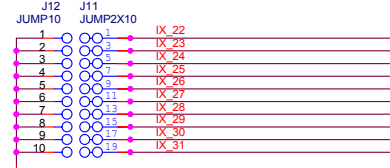
Firma		MLAB		Author	MIHO
Size	A3	Project Name	MLAB	Schematic Name	S3AN01A
Date:	Monday, March 21, 2011	Sheet	3	of	5
				Rev	1.01



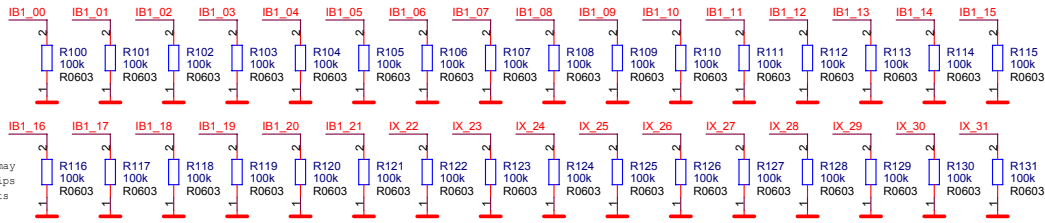
NIBBLE
ENABLE



5V TOLERANT INPUTS (BANK 1)

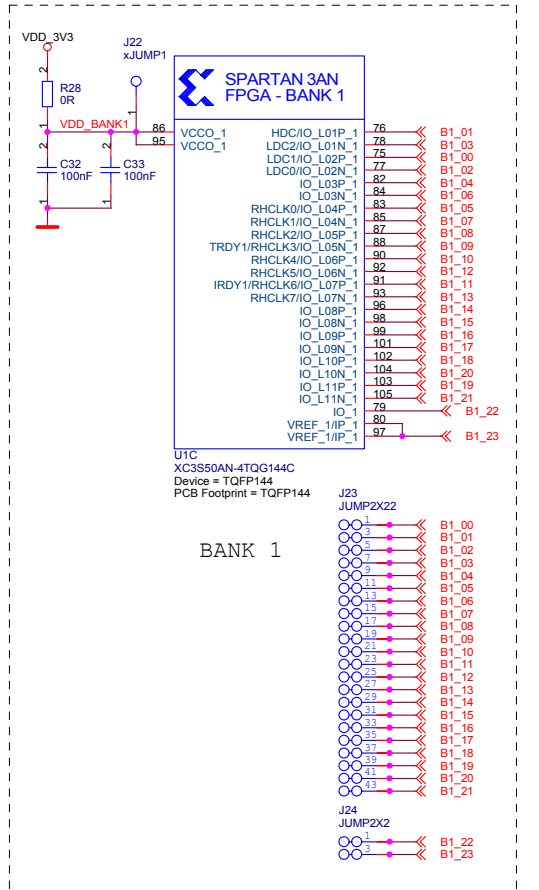
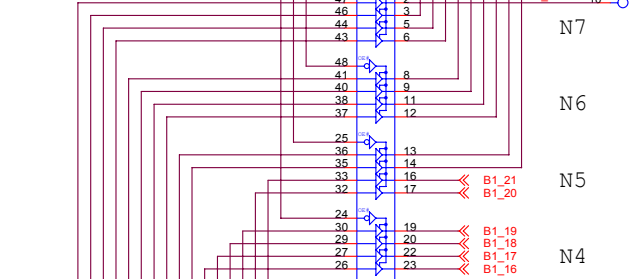
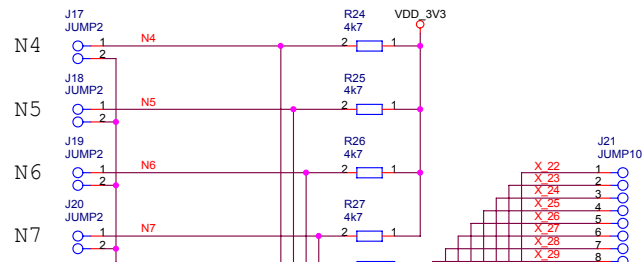


5V TOLERANT INPUTS

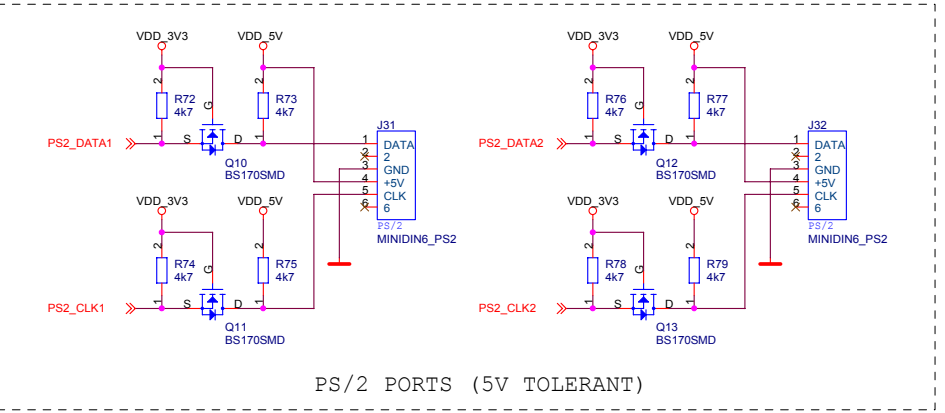
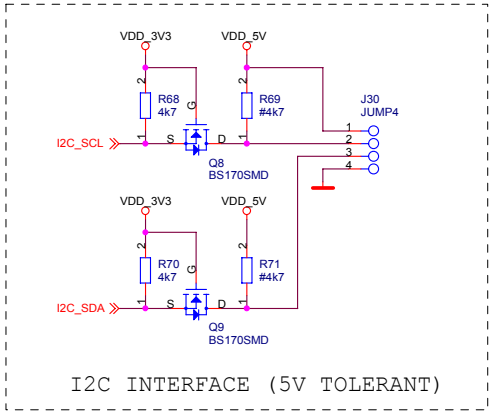
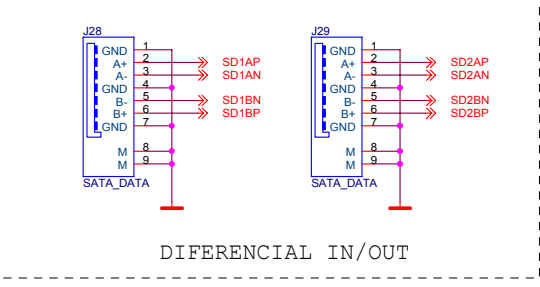
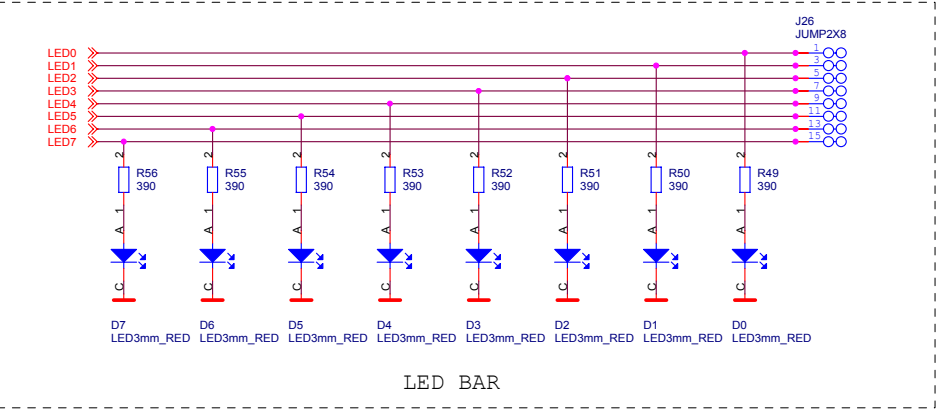
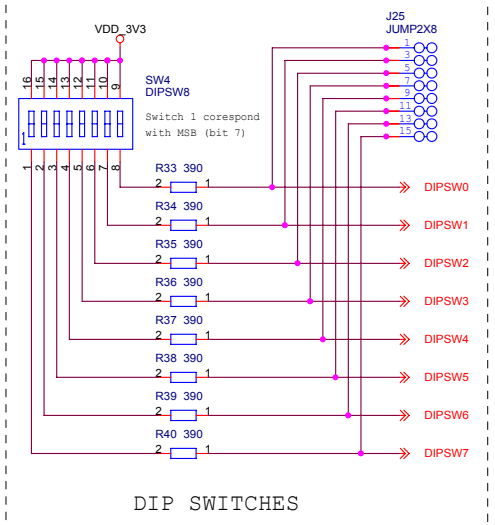
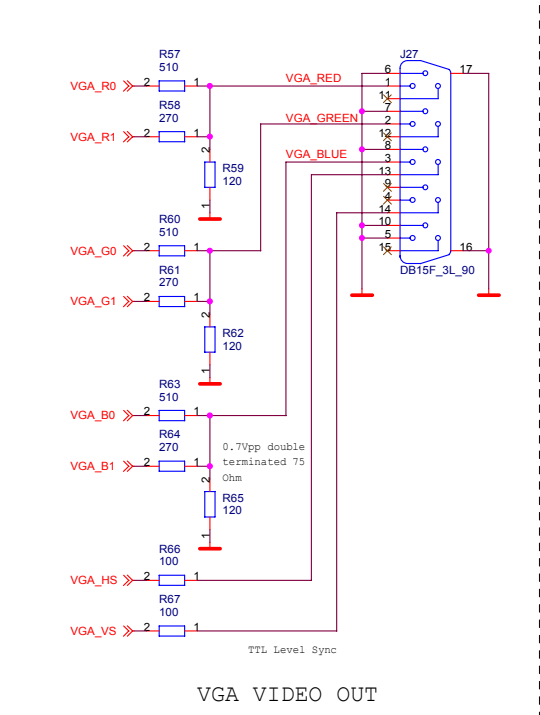
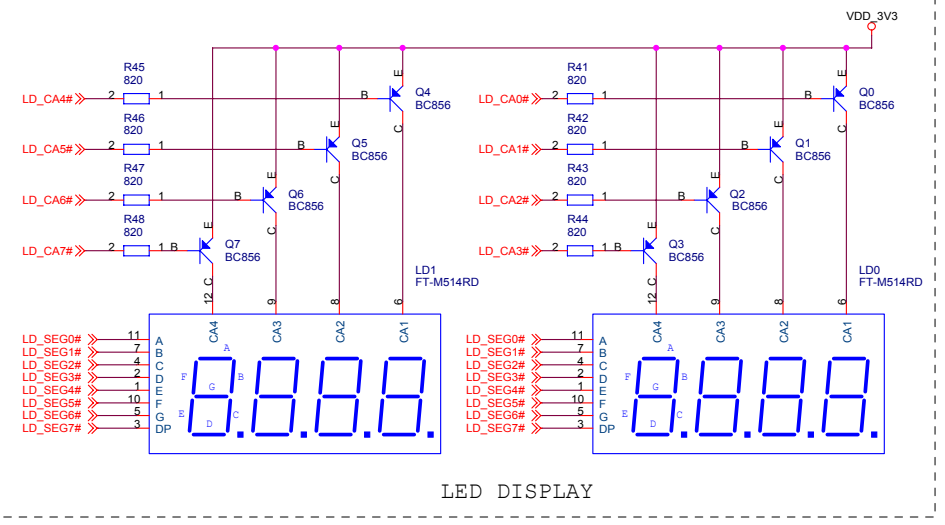
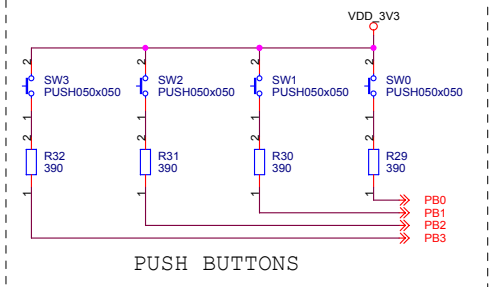


5V TOLERANT INPUTS for BANK 1

Pull Down Resistors may be omitted if used chips with Bus Keeper inputs



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A3	MLAB	S3AN01A	1.01
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