

S3AN01A

XILINX Spartan 3AN  
FPGA School Board

- 1.00 New Design
- 1.01 Typo Corrections and Errata  
Verified in hardware

Errata

Pins 33 and 35 are Input Only and can not be used for LED output.

Cut wires PS2\_CLK1 and PS2\_DATA1 near to serial R

Connect U1.12 with U1.35

Connect U1.13 with U1.33

Do not use PS2 (1)

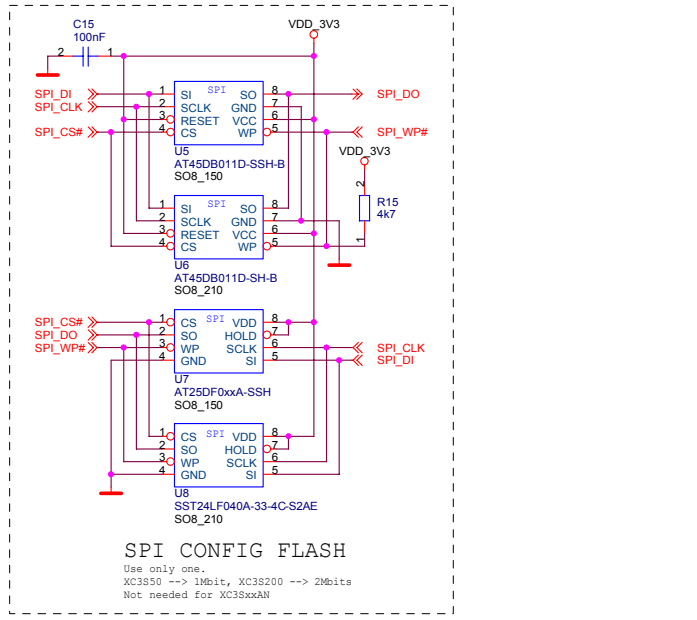
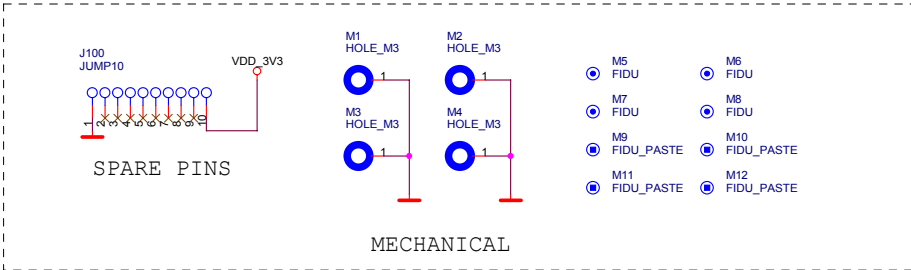
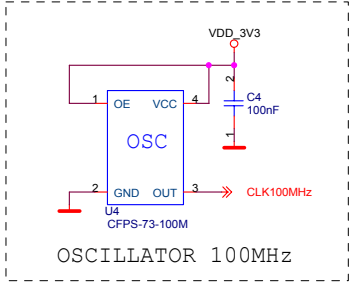
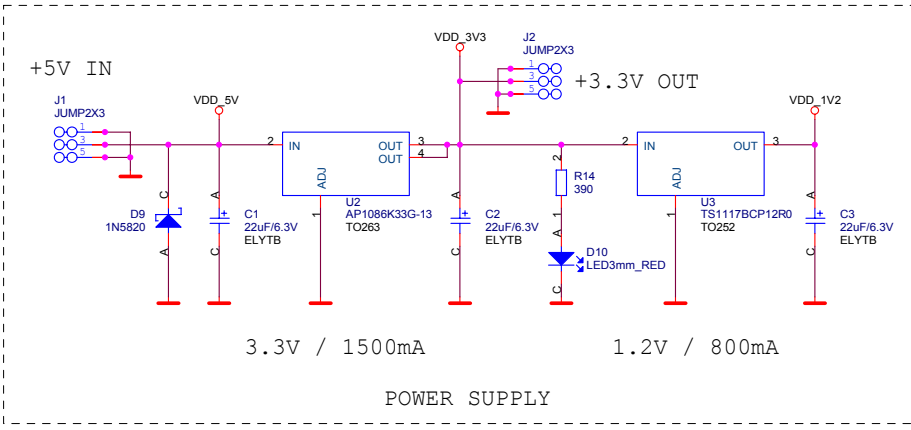
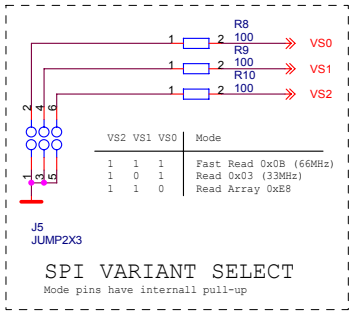
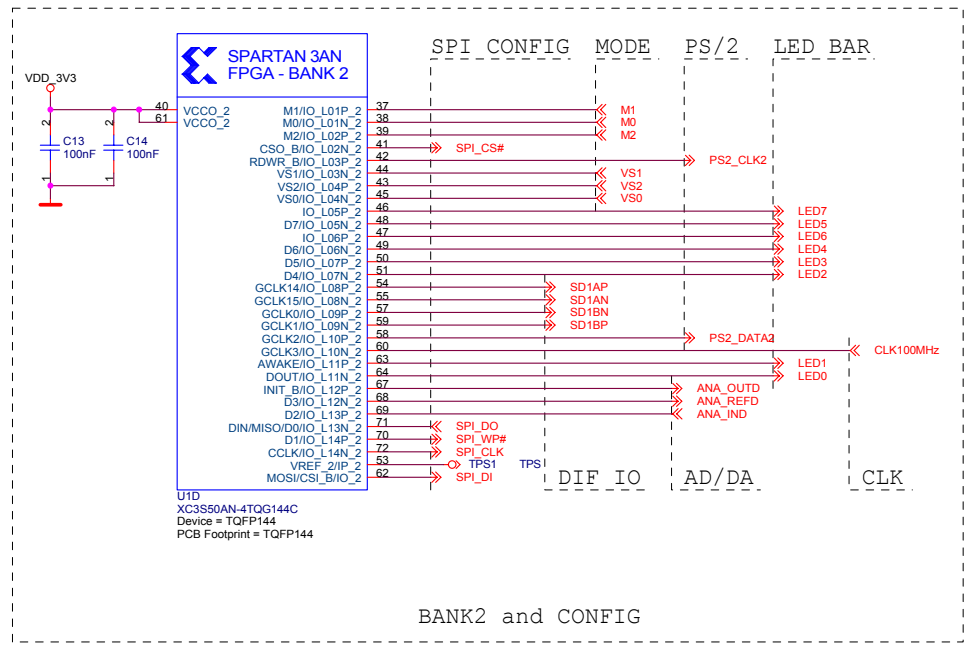
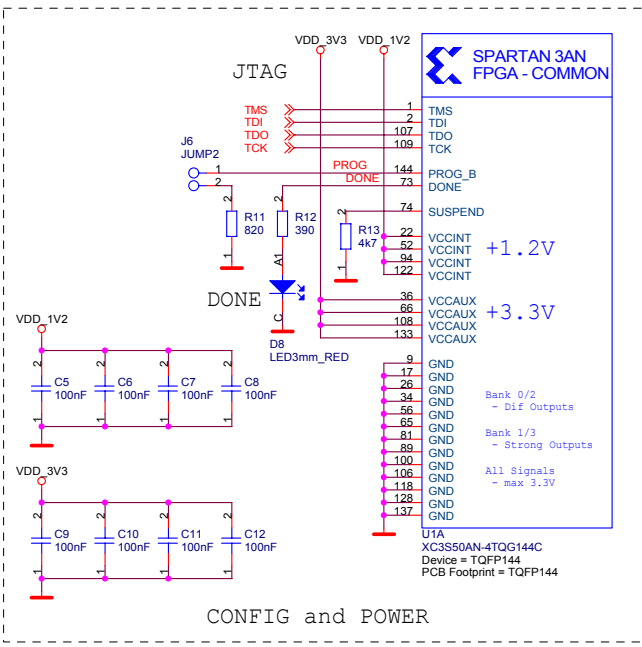
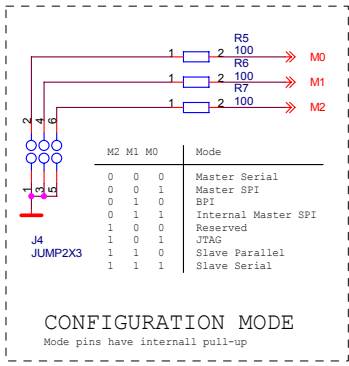
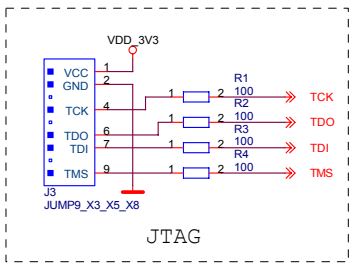
There are missing serial resistors for LED display.

Enable LED display segments for a short time only

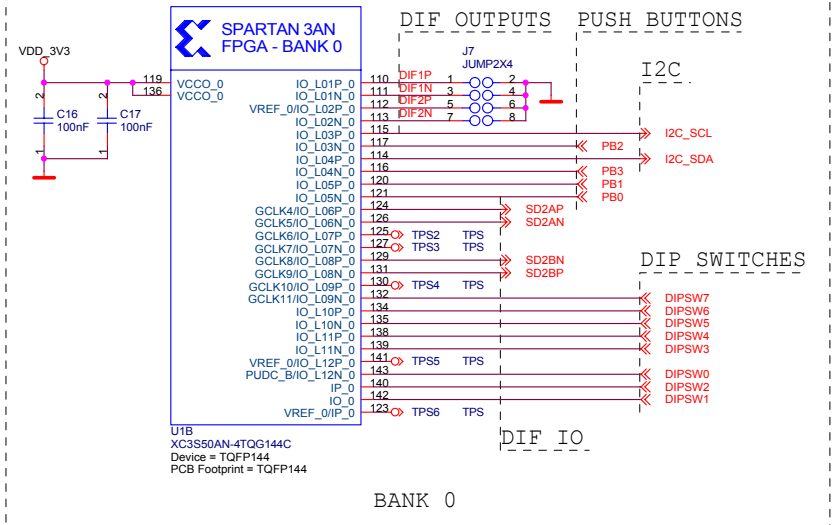
Identifiers B1\_nn of bank 1 pins ends in '\_' what is not valid  
identifier in VHDL.

Use different name in VHDL and UCF

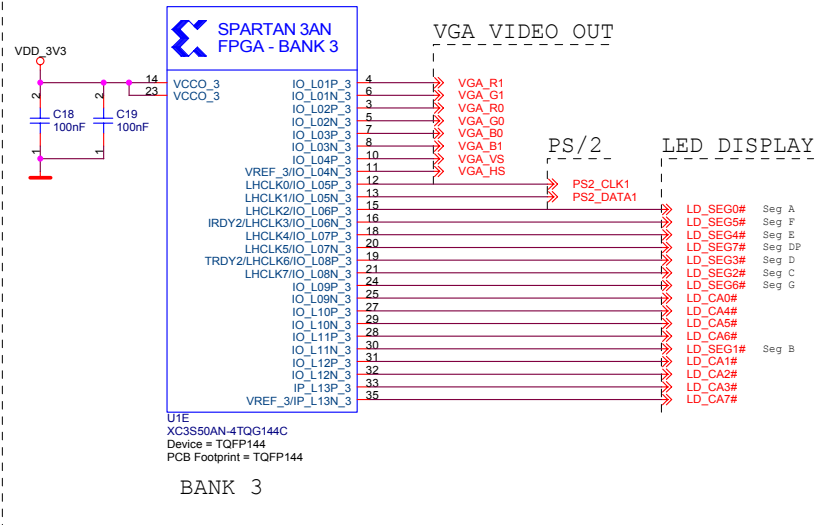
Firma		Author	
MLAB		MIHO	
Size	Project Name	Schematic Name	Rev
A3	MLAB	S3AN01A	1.01
Date:	Thursday, March 17, 2011	Sheet	1 of 5



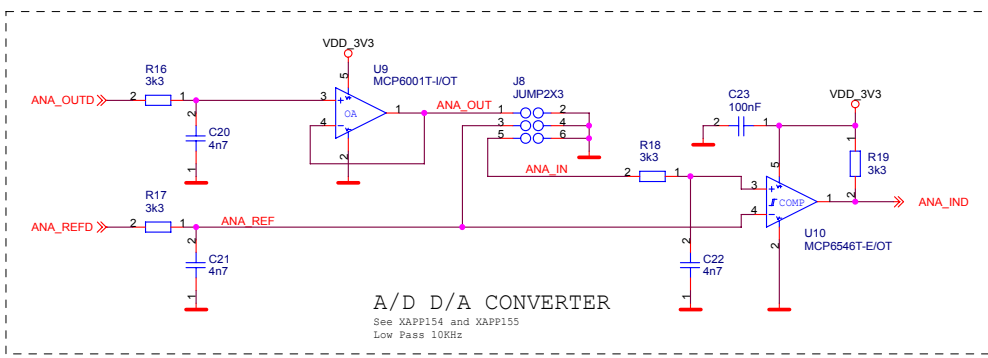
Firma		Author MIHO	
<b>MLAB</b>			
Size A3	Project Name MLAB	Schematic Name S3AN01A	Rev 1.01
Date: Thursday, March 17, 2011	Sheet 2 of 5		



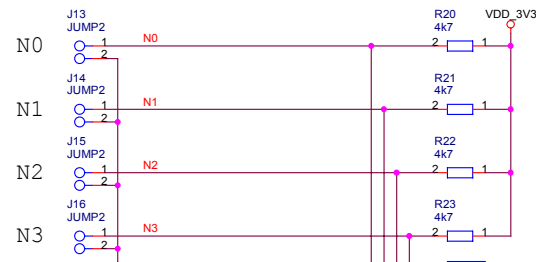
BANK 0



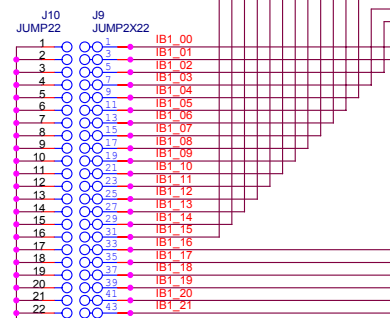
BANK 3



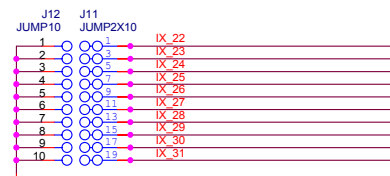
Firma		<b>MLAB</b>		Author	MIHO
Size	A3	Project Name	MLAB	Schematic Name	S3AN01A
Date:	Thursday, March 17, 2011	Sheet	3	of	5
				Rev	1.01



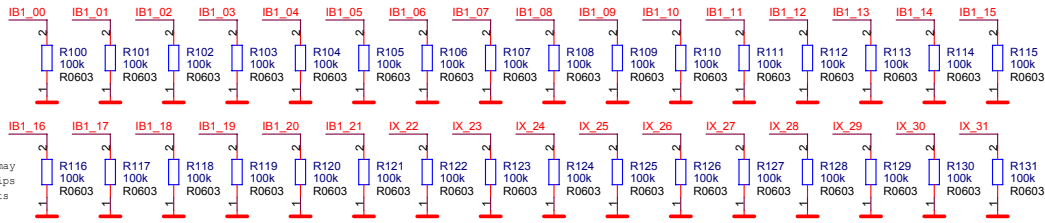
NIBBLE  
ENABLE



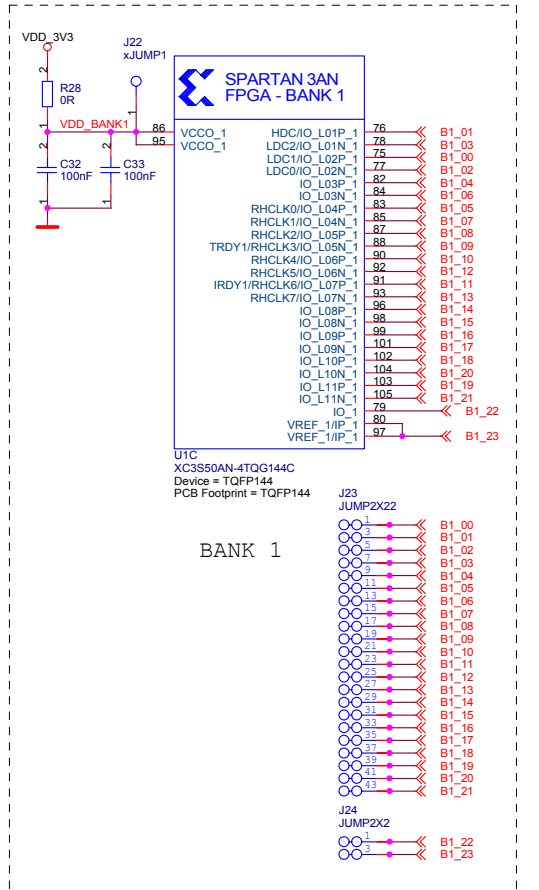
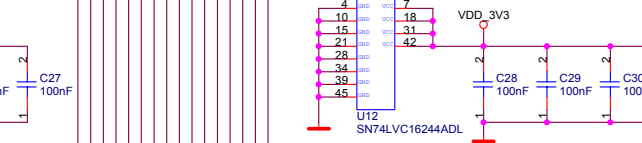
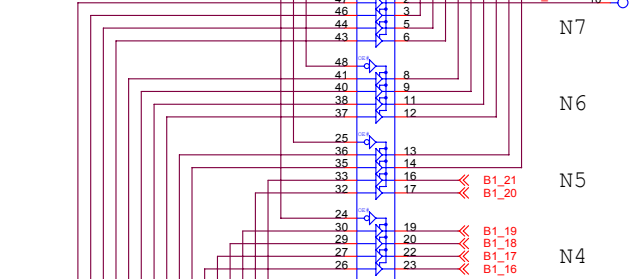
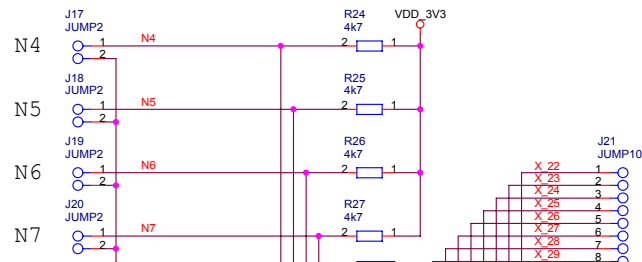
5V TOLERANT INPUTS (BANK 1)



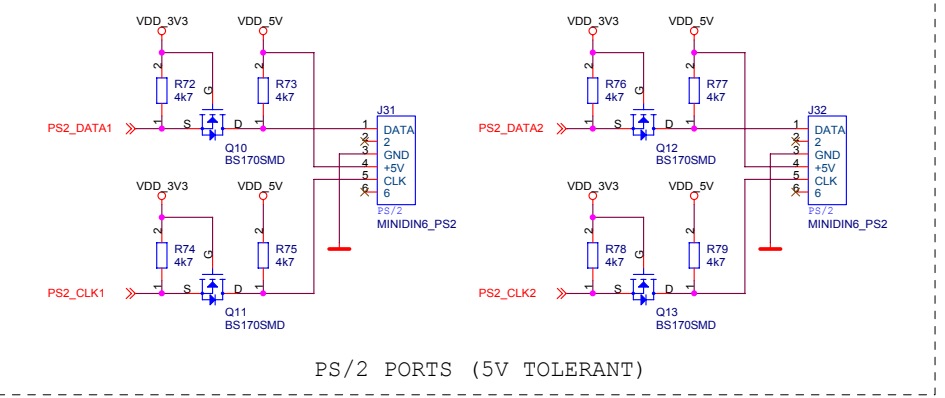
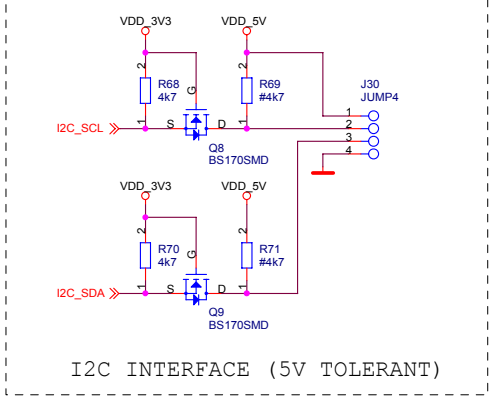
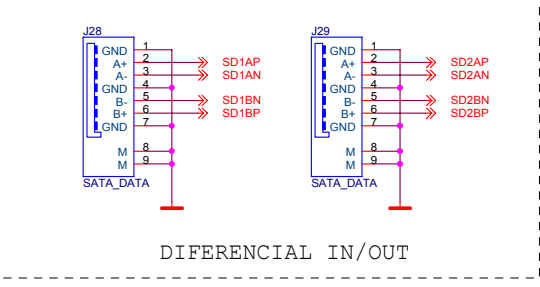
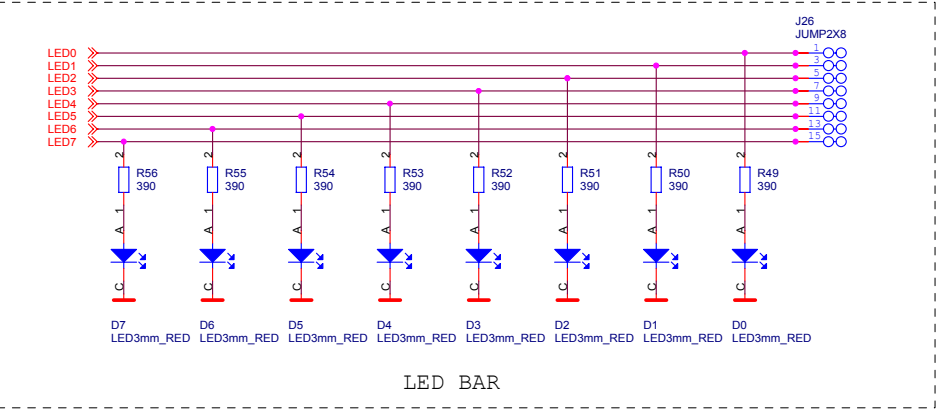
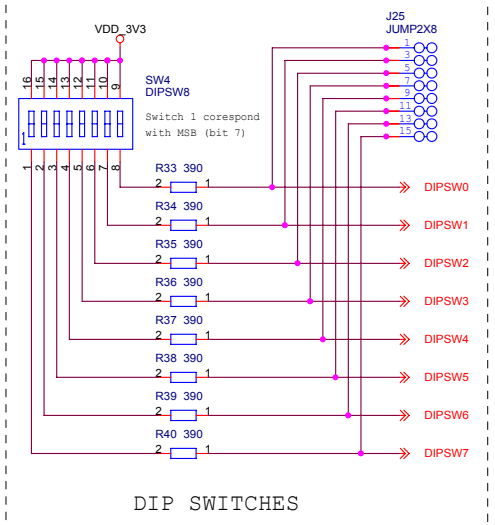
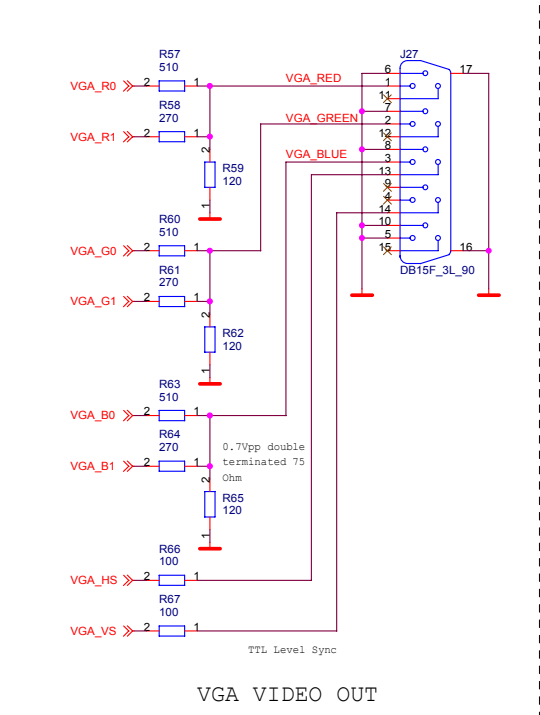
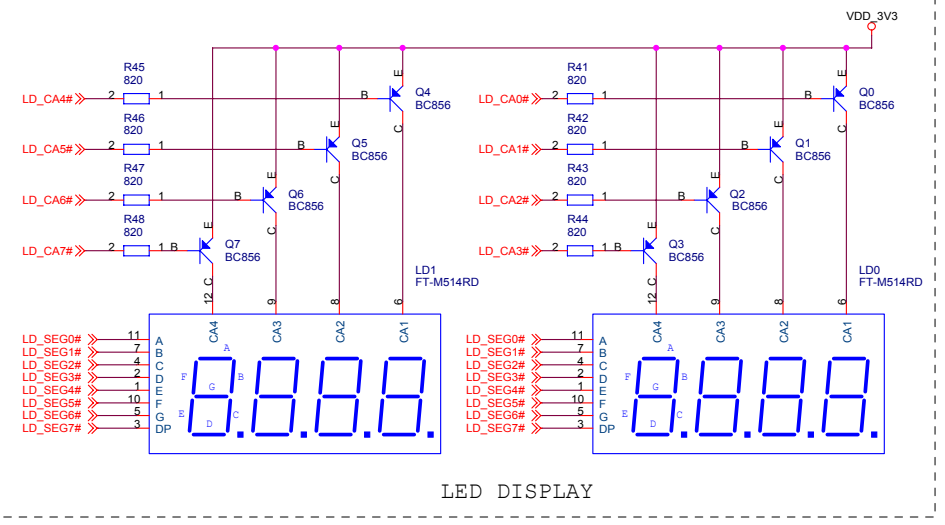
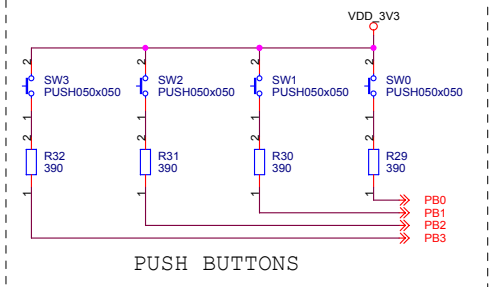
5V TOLERANT INPUTS



5V TOLERANT INPUTS for BANK 1



Firma		Author	
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A3	MLAB	S3AN01A	1.01
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<b>MLAB</b>		MIHO	
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