ISM BAND FSK TRANSMITTER MODULE

RFM02

（the purpose of this spec covers mainly for the physical characteristic of the module, for register configure and its related command info please refer to RF02 data sheets）

RFM02

General Introduction

RFM02 is a low costing ISM band transmitter module implemented with unique PLL approach. It works with FSK modulated signal ranges from 433/868/915MHZ bands, comply with FCC, ETSI regulation. The SPI interface is used to communicate with microcontroller for parameter setting. RFM02 works with RFM01 receiver module. At 433MHZ band, the pair of module can work up to 300m in the free open air.

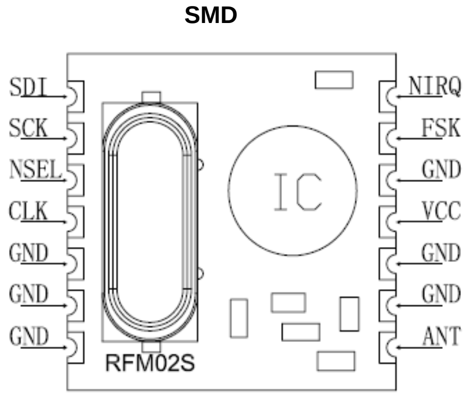
Features:

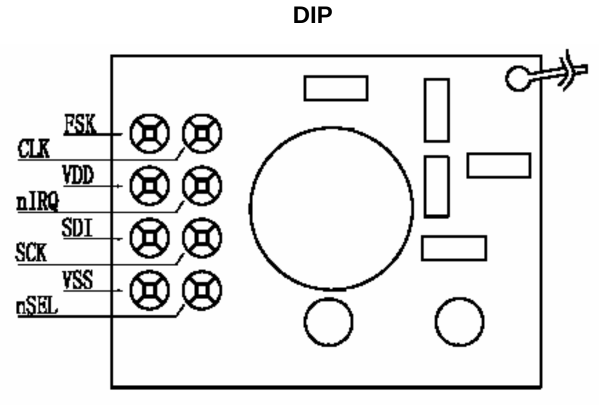
- Low costing, high performance and price ratio
- Tuning free during production
- FSK transmission
- PLL employed
- Fast PLL lock time
- High resolution PLL with 2.5 KHz step
- Programmable frequency deviation (from 30 kHz to 210 kHz, step 30 kHz)
- Programmable output power
- High data rate (up to 115.2 kbps with FSK modulation)
- Differential antenna output
- Automatic antenna tuning
- SPI interface
- Clock and reset signal output for external MCU use
- 10MHz crystal for PLL reference
- Programmable crystal load capacitor bank
- Wakeup timer
- low battery detection
- 2.2V - 5.4V power supply
- Low power consumption
- stand by current less than 0.3μA

Typical Application:

- Remote control
- Remote sensor
- Wireless data collection
- Home security system
- Toys
- Tire pressure monitoring system

Pin Definition:





Definition	TYPE	function
FSK	DI	FSK data input
CLK	DO	clock out for MCU (1 MHz-10 MHz)
VDD	S	Positive power supply
nIRQ	DO	Interrupts request output（active low）
SDI	DI	SPI data input
SCK	DI	SPI clock input
VSS	S	negative power supply, GND
nSEL	DI	Chip select (active low)

Electrical Specification:

Maximum（not at working mode）

symbol	parameter	min	max	unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	V_{dd}+0.5	V
I_{in}	Input current except power	-25	25	mA
ESD	Human body model		1000	V
T_{st}	Storage temperature	-55	125	℃
T_{ld}	Soldering temperature(10s)		260	℃

Recommended working range

symbol	parameter	min	max	unit
V_{dd}	Positive power supply	2.2	5.4	V
T_{op}	operation temperature	-40	85	℃

DC Characteristics:

symbol	parameter		conditions/note	min	typ	max	unit
$I_{dd\_TX\_0}$	current consumption	433 MHz band	0 dBm power output		12		mA
		868 MHz band			14		
		915 MHz band			15		
$I_{dd\_TX\_PMAX}$	current consumption	433 MHz band	max power output		23		mA
		868 MHz band			25		
		915 MHz band			26		
I_{pd}	sleep mode current		all blocks off		0.3		μA
I_{wt}	waek-up timer current consumption				1.5		μA
I_{lb}	low battery detector current consumption				0.5		μA
I_x	idle mode current		only crystal work		1.5		mA
V_{lba}	low battery detection accuracy				75		mV
V_{lb}	low battery detection range		0.1V step	2.2		5.3	V
V_{il}	Low level input					0.3*V_{dd}	V
V_{ih}	High level input			0.7*V_{dd}			V
I_{il}	Leakage current		Vil = 0 V	-1		1	μA
I_{ih}	Leakage current		$V_{ih} = V_{dd}$, V_{dd} = 5.4V	-1		1	μA
V_{ol}	Low level output		I_{ol} = 2 mA			0.4	V
V_{oh}	High level output		I_{oh} = -2 mA	V_{dd}-0.4			V

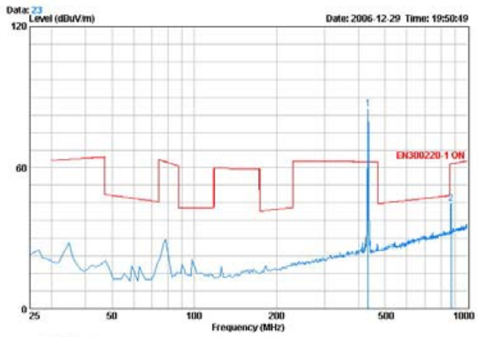
DC Characteristics:

symbol	parameter	conditions/notes	min	typ	max	unit
f_{ref}	PLL reference frequency	Parallel fundamental	9	10	11	MHz
f_o	Output frequency (f_{ref}=10MHZ)	433MHz band,2.5kHz step 868MHz band,5.0kHz step 915MHz band,7.5kHz step	430.24 860.48 900.72		439.75 879.51 929.27	MHz
f_o	Output frequency (f_{ref}=9MHZ)	433MHz band,2.5kHz step 868MHz band,5.0kHz step 915MHz band,7.5kHz step	387.22 774.43 810.65		395.76 791.56 836.34	MHz
f_o	Output frequency (f_{ref}=11MHZ)	433MHz band,2.5kHz step 868MHz band,5.0kHz step 915MHz band,7.5kHz step	473.26 946.53 990.79		483.73 967.46 1022.2	MHz
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		20		μs
t_{sp}	PLL start time	After crystal stabilized			250	μs
P_{maxL}	available ouput power(315and433MHz band)			8		dBm
P_{maxH}	available ouput power(868and915MHz band)			5		dBm
C_o	output capacitance(set by antenna tuning circuit)	low bands high bands	1.5 1.6	2.3 2.2	3.1 2.8	pF
Q_o	Q factor of output capacitance		16	18	22	
BR_{FSK}	FSK data rate				115.2	kbps
df_{fsk}	FSK deviation	30KHz step	30KHz		210	kHz
C_{xl}	crystal load capacitance	0.5pF step,tolerance +/-10%	8.5		16	pF
t_{PBt}	period of wake-up timer clock	calibrated evry 30 seconds	0.95		1.05	ms
$t_{wake\text{-}up}$	wake-up time(programable)		1		2*10E9	ms
t_{POR}	internal POR time	after power reached 90% VDD			100	ms
t_{sx}	Crystal start time	ESR < 100 ohms			5	ms

Field testing range

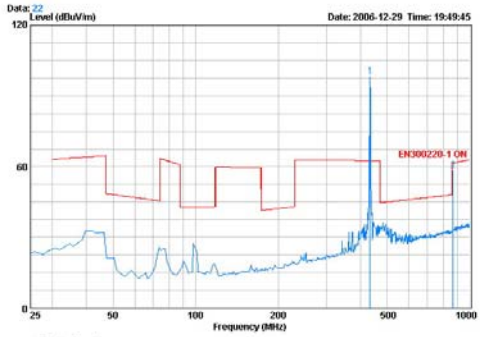
operation band	condition	range
433MHz band	Bandwidth=134KHz, data rate=1.2kbps Frequency deviation=60KHZ（matches with RFM01） in free open area	>300m
868MHz band	Bandwidth=134KHz, data rate=1.2kbps Frequency deviation=60KHZ（matches with RFM01） in free open area	>200m
915MHz band	Bandwidth=134KHz, data rate=1.2kbps Frequency deviation=60KHZ（matches with RFM01） in free open area	>200m

SGS Reports



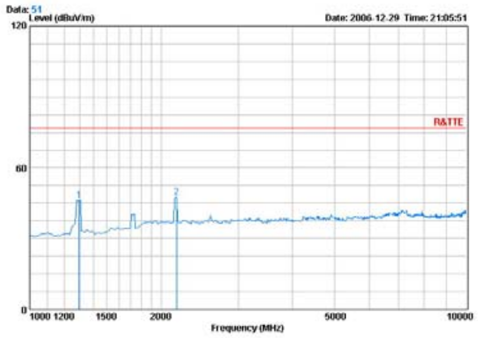
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	432.550	2.34	16.56	27.52	93.56	84.94	62.55	22.39
2	872.275	3.50	22.93	26.57	44.93	44.80	61.61	-16.82



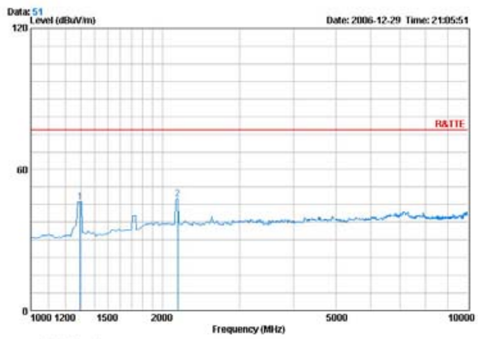
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	432.550	2.34	16.56	27.52	106.57	97.95	62.55	35.41
2	868.375	3.48	22.85	26.58	58.53	58.28	61.57	-3.29



Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 @	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65



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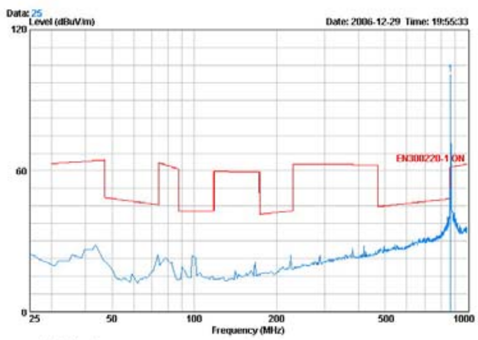
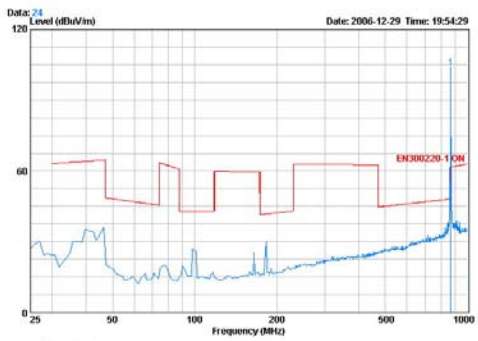
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 @	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65



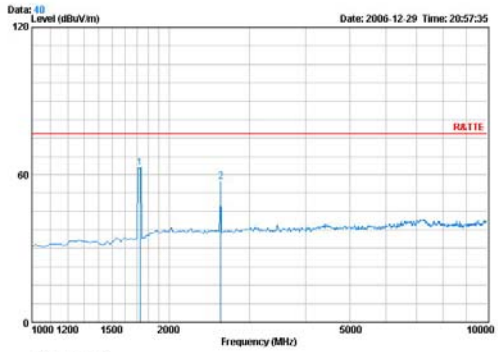
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	868.375	3.48	22.85	26.58	101.34	101.08	61.57	39.51



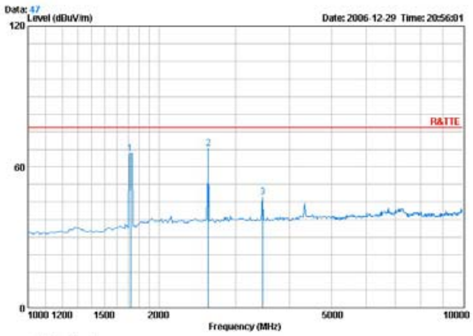
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	868.375	3.48	22.85	26.58	103.75	103.49	61.57	41.92



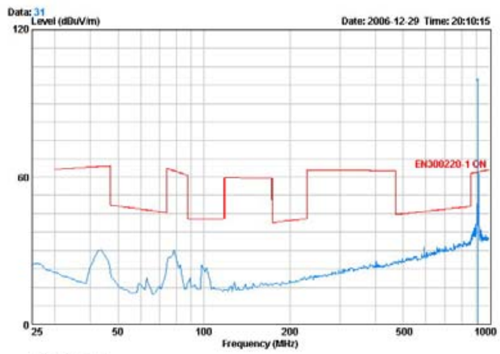
Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1729.000	1.59	29.86	44.70	76.11	62.86	77.00	-14.14
2	2602.000	2.04	32.54	44.80	67.38	57.16	77.00	-19.84



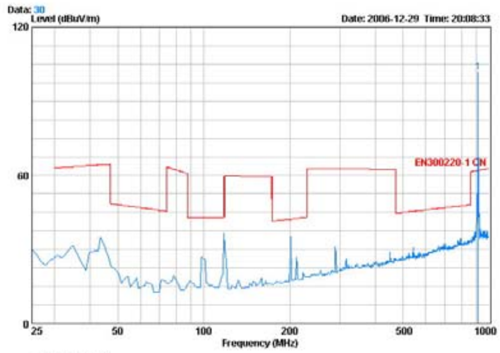
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1720.000	1.59	29.82	44.70	78.87	65.58	77.00	-11.42
2 @	2602.000	2.04	32.54	44.80	78.13	67.91	77.00	-9.09
3	3466.000	2.35	33.21	45.01	56.47	47.02	77.00	-29.98



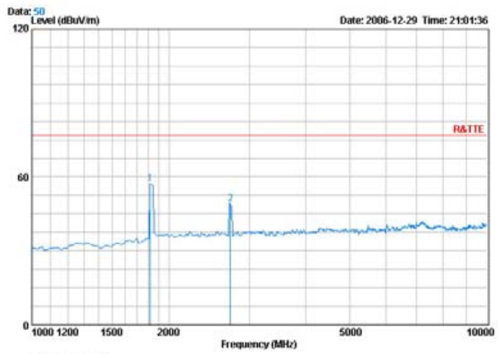
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	95.64	96.09	62.05	34.04



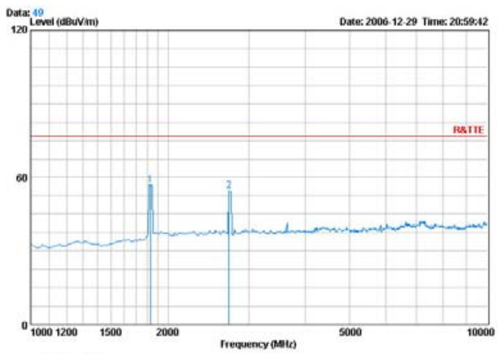
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	101.18	101.63	62.05	39.57



Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1819.000	1.65	30.61	44.69	69.51	57.09	77.00	-19.91
2	2728.000	2.09	32.82	44.84	58.95	49.03	77.00	-27.97



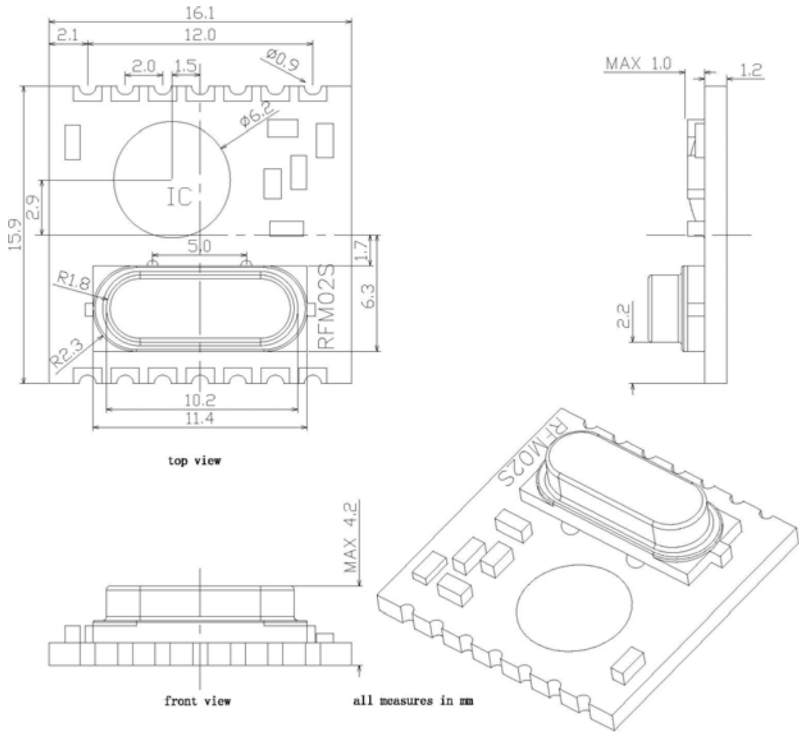
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1828.000	1.66	30.70	44.68	69.20	56.87	77.00	-20.13
2	2719.000	2.09	32.01	44.83	64.43	54.49	77.00	-22.51

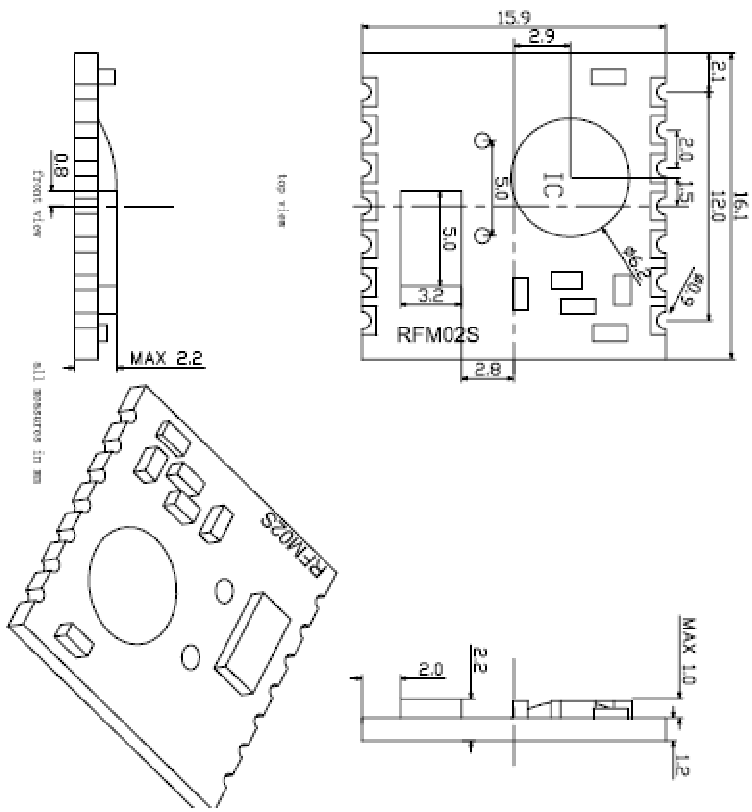
Mechanical Dimension:

（all dimensions in mm）

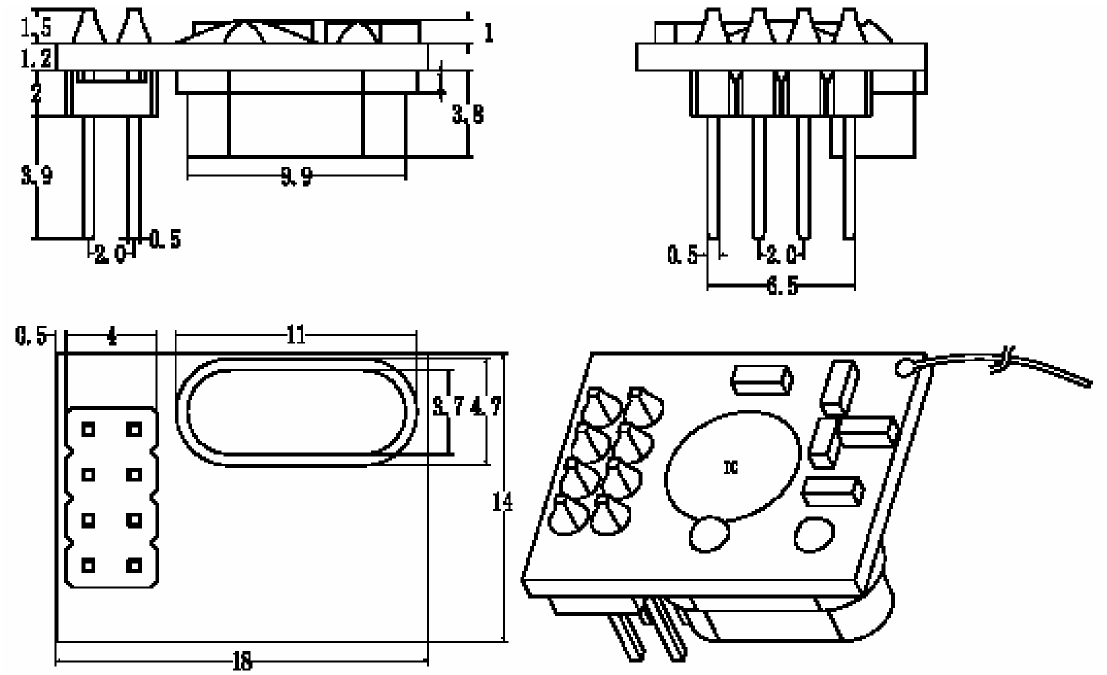
SMD PACKAGE（S1）



SMD PACKAGE（S2）



DIP PACKAGE（D）



Module Definition

model=module-operation band

RFM02B-433-D/S

module type operation band Package

eg：1，RFM02 module at 433MHz band, DIP : RFM02-433-D。

2，RFM02 module at 868MHz band, SMD, thickness at 4.2mm : RFM02-868-S1。

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RF02 programming guide

1. Brief description

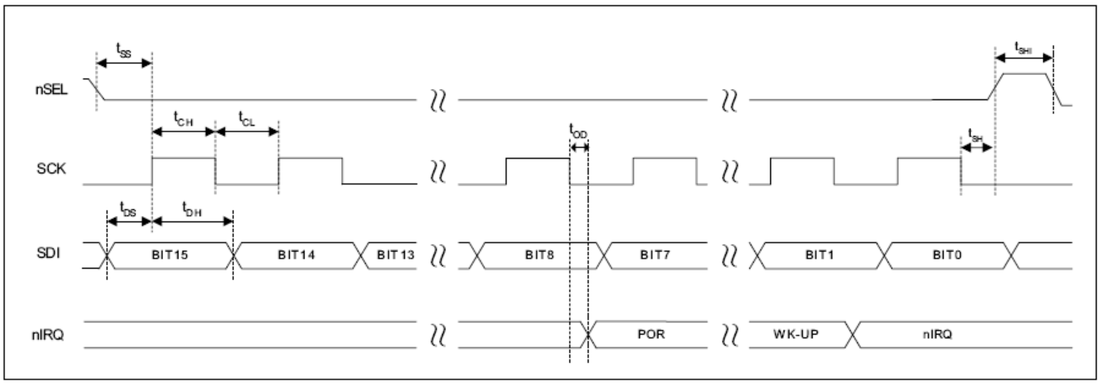
RF02 is a low cost FSK transmit IC witch integrated all RF functions in a single chip. It only need a MCU, a crystal, a decouple capacitor and antenna to build a hi reliable FSK transmitter. The operation frequency can cover 300 to 1000MHz.

RF02 supports a command interface to setup frequency, deviation, output power and also data rate. No need any hardware adjustment when using in frequency-hopping applications

RF02 can be used in applications such as remote control toys, wireless alarm, wireless sensor, wireless keyboard/mouse, home-automation and wireless data collection.

2. Commands

1. Timing diagram



2. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	d2	d1	d0	x3	x2	x1	x0	ms	m2	m1	m0	8080h

b1..b0: band select:

b1	b0	band[MHz]
0	1	433
1	0	868
1	1	915

d2..d0: select frequency of CLK pin

d2	d1	d0	CLK frequency[MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal.

If not used, please set bit “dc” to disable CLK output

x3..x0: select crystal load capacitor

x3	x2	x1	x0	Load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
……			……	
1	1	1	0	15.5
1	1	1	1	16.0

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

ms: select modulation polarity

m2..m0: select frequency deviation

m2	m1	m0	frequency deviation[kHz]
0	0	0	30
0	0	1	60
0	1	0	90
0	1	1	120
1	0	0	150
1	0	1	180
1	1	0	210

.

3. Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	a1	a0	ex	es	ea	eb	et	dc	C000h

a1： Crystal oscillator and synthesizer are enabled by Data transmit Command and disable by Sleep command.

a0： Power amplifier is enabled by Data transmit Command and disable by Sleep Command.

ex： Enable crystal oscillator

es： Enable synthesizer

ea： Enable power amplifier

eb： Enable low battery detection funciton

et： Enable wake-up timer

dc： Disable output of CLK pin

4. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A7D0h

f11..f0: set operation frequency:

433band: Fc=430+F*0.0025 MHz

868band: Fc=860+F*0.0050 MHz

915band: Fc=900+F*0.0075 MHz

Fc is carrier frequency

5. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	r7	r6	r5	r4	r3	r2	r1	r0	C800h

r7..r0: set data rate

BR=10000000/29/（R+1）

BR is data rate

6. Power Setting Command

bit	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	p2	p1	p0	B0h

p2..p0: set relative output power:

Pout=Pmax-P*3 [dBm]

Pmax is the max output power; it is related to the antenna impedance.

7. Low Battery Detector and Tx bit Synchronization Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	dwc	0	ebs	t4	t3	t2	t1	t0	C200h

dwc： Disable wake-up timer periodical calibration

ebs： Enable TX bit synchronization function

t4..t0: Set threshold voltage of Low battery detector

Vlb=2.2+T*0.1 [V]

8. Sleep Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0	C400h

If crystal oscillator, synthesizer and power amplifier are auto-controlled, this command will close power amplifier and synthesizer immediately, then stop crystal oscillator after S periods of CLK signal

9. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E000h

The wake-up timer period is determined by:

$T_{wake-up} = M * 2^R$ [ms]

For continual operation, bit ‘et’ must be cleared and set

10. Data Transmit Command

bit	7	6	5	4	3	2	1	0
	1	1	0	0	0	1	1	0

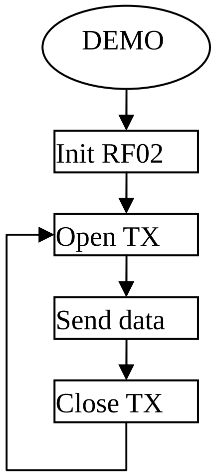
This command indicate that the following data on SDI pin is to be transmitted, the transmission stops if nSel return to hi.

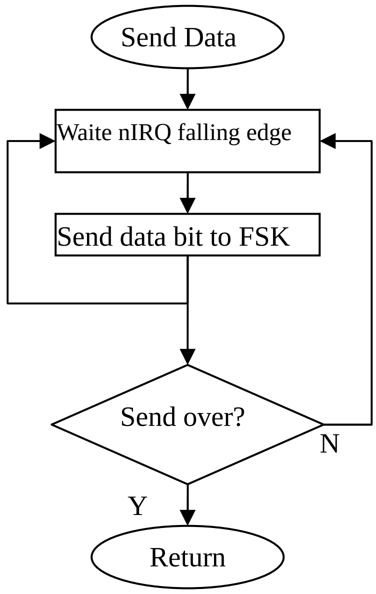
11. Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	--

This command is used to read internal status register content, output starts at 8_{th} clock of SCK.

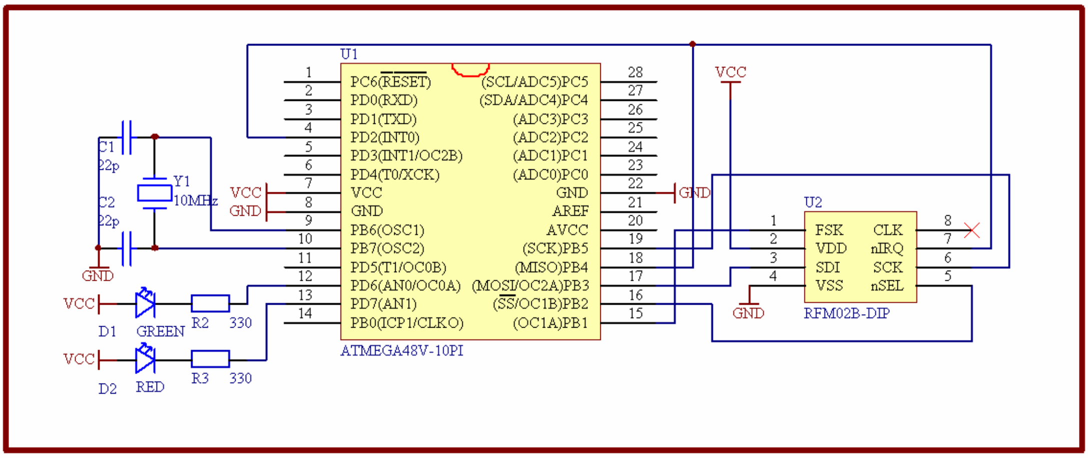
3. Transmission Demo flow diagram





Note: After RF02 initialization, Open transmitter and use nIRQ as data rate clock. MCU write data bit on FSK pin at nIRQ falling edge.

4. Example 1(for AVR microcontroller)

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    /*************************************************************
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Title:              RF02B simple example based on AVR C
Current version:    v1.0
Function:           Package send Demo
Processor           ATMEGA48
Clock:              10MHz Crystal
Operate frequency:  434MHz
Data rate:          4.8kbps
Package size:       23byte
Author:             Tank
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Date:               2006-10-24

                 Connections

      ATMEGA48 SIDE       RF02B SIDE
        SCK--------------->SCK
       MISO:NC
       MOSI--------------->SDI
         SS--------------->nSEL
        PB1--------------->FSK
       INT0<---------------nIRQ

       PC0~PC3: LED0~LED3
```

```
***********************************************************************/
#include <mega48.h>

#define DDR_IN          0
#define DDR_OUT         1

#define PORT_SEL        PORTB
#define PIN_SEL         PINB
#define DDR_SEL         DDRB

#define PORT_SDI        PORTB
#define PIN_SDI         PINB
#define DDR_SDI         DDRB

#define PORT_SCK        PORTB
#define PIN_SCK         PINB
#define DDR_SCK         DDRB

#define PORT_SDO        PORTB
#define PIN_SDO         PINB
#define DDR_SDO         DDRB

#define PB7             7//--\
#define PB6             6//  |
#define RFXX_SCK        5//  |
#define RFXX_SDO        4//  |RF_PORT
#define RFXX_SDI        3//  |
#define RFXX_SEL        2//  |
#define RFXX_DATA       1//  |
#define PB0             0//--/

#define SEL_OUTPUT()    DDR_SEL |= (1<<RFXX_SEL)
#define HI_SEL()        PORT_SEL|= (1<<RFXX_SEL)
#define LOW_SEL()       PORT_SEL&=~(1<<RFXX_SEL)

#define SDI_OUTPUT()    DDR_SDI |= (1<<RFXX_SDI)
#define HI_SDI()        PORT_SDI|= (1<<RFXX_SDI)
#define LOW_SDI()       PORT_SDI&=~(1<<RFXX_SDI)

#define SDO_INPUT()     DDR_SDO&= ~(1<<RFXX_SDO)
#define SDO_HI()        PIN_SDO&(1<<RFXX_SDO)

#define SCK_OUTPUT()    DDR_SCK |= (1<<RFXX_SCK)
#define HI_SCK()        PORT_SCK|= (1<<RFXX_SCK)
```

```
#define LOW_SCK()         PORT_SCK&=~(1<<RFXX_SCK)

void RFXX_PORT_INIT(void){
  HI_SEL();
  HI_SDI();
  LOW_SCK();
  SEL_OUTPUT();
  SDI_OUTPUT();
  SDO_INPUT();
  SCK_OUTPUT();
}
unsigned int RFXX_WRT_CMD(unsigned int aCmd){
  unsigned char i;
  unsigned int temp;
  LOW_SCK();
  LOW_SEL();
  for(i=0;i<16;i++){
    temp<<=1;
    if(SDO_HI()){
      temp|=0x0001;
    }
    LOW_SCK();
    if(aCmd&0x8000){
      HI_SDI();
    }else{
      LOW_SDI();
    }
    HI_SCK();
    aCmd<<=1;
  };
  LOW_SCK();
  HI_SEL();
  return(temp);
}

void RF02B_SEND(unsigned char aByte){
  unsigned char i;

  for(i=0;i<8;i++){
    while(PINB&(1<<RFXX_SDO));//Polling nIRQ
    while(!(PINB&(1<<RFXX_SDO)));
    if(aByte&0x80){
      PORTB|=(1<<RFXX_DATA);
    }else{
```

```
      PORTB&=~(1<<RFXX_DATA);
    }
    aByte<<=1;
  }

}

void main(void)
{
  unsigned int i,j,ChkSum;

  RFXX_PORT_INIT();

  RFXX_WRT_CMD(0xCC00);
  RFXX_WRT_CMD(0x8B61);//433BAND,+/-90kHz
  RFXX_WRT_CMD(0xA640);//434MHz
  RFXX_WRT_CMD(0xD040);//RATE/2
  RFXX_WRT_CMD(0xC823);//4.8kbps
  RFXX_WRT_CMD(0xC220);//ENABLE BIT SYNC
  RFXX_WRT_CMD(0xC001);//CLOSE ALL

  PORTB|=(1<<RFXX_DATA);
  DDRB|=(1<<RFXX_DATA);//SET DATA OUTPUT

  while(1){
    RFXX_WRT_CMD(0xC039);//START TX
    ChkSum=0;
    RF02B_SEND(0xAA);//PREAMBLE
    RF02B_SEND(0xAA);//PREAMBLE
    RF02B_SEND(0xAA);//PREAMBLE
    RF02B_SEND(0x2D);//HEAD HI BYTE
    RF02B_SEND(0xD4);//HEAD LOW BYTE
    RF02B_SEND(0x30);//DATA0
    ChkSum+=0x30;
    RF02B_SEND(0x31);//DATA1
    ChkSum+=0x31;
    RF02B_SEND(0x32);
    ChkSum+=0x32;
    RF02B_SEND(0x33);
    ChkSum+=0x33;
    RF02B_SEND(0x34);
    ChkSum+=0x34;
    RF02B_SEND(0x35);
    ChkSum+=0x35;
```

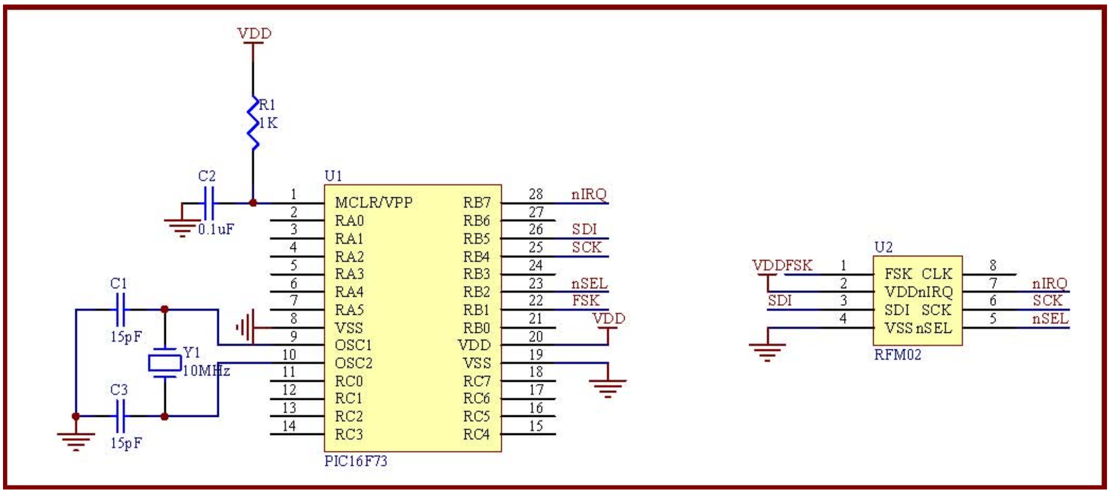
```
    RF02B_SEND(0x36);
    ChkSum+=0x36;
    RF02B_SEND(0x37);
    ChkSum+=0x37;
    RF02B_SEND(0x38);
    ChkSum+=0x38;
    RF02B_SEND(0x39);
    ChkSum+=0x39;
    RF02B_SEND(0x3A);
    ChkSum+=0x3A;
    RF02B_SEND(0x3B);
    ChkSum+=0x3B;
    RF02B_SEND(0x3C);
    ChkSum+=0x3C;
    RF02B_SEND(0x3D);
    ChkSum+=0x3D;
    RF02B_SEND(0x3E);
    ChkSum+=0x3E;
    RF02B_SEND(0x3F);//DATA15
    ChkSum+=0x3F;
    RF02B_SEND(ChkSum);//DATA16
    RF02B_SEND(0xAA);//DUMMY BYTE

    RFXX_WRT_CMD(0xC001);//CLOSE TX

    for(i=0;i<5000;i++)for(j=0;j<123;j++);

  };
}
```

5. Example 2(for PIC microcontroller)




```
/*****************************************************
    copyright (c) 2006
Title:             RF02B simple example based on PIC C
Current version:   v1.0
Function:          Package send Demo
Processor          PIC16F73
Clock:             10MHz Crystal
Operate frequency: 434MHz
Data rate:         4.8kbps
Package size:      23byte
Author:            Robben
Company:           Hope microelectronic Co.,Ltd.
Contact:           +86-0755-86106557
E-MAIL:            hopefsk@hoperf.com
Date:              2006-11-10
*****************************************************/
#include "pic.h"

typedef unsigned char uchar;
typedef unsigned int  uint;

#define SDI          RB5
#define SCK          RB4
#define nSEL         RB2
#define FSK          RB1
#define nIRQ         RB7
#define SDO          RB6
#define SDI_OUT()    TRISB5=0
#define SCK_OUT()    TRISB4=0
```

```
#define nSEL_OUT()      TRISB2=0
#define FSK_OUT()       TRISB1=0
#define nIRQ_IN()       TRISB7=1
#define SDO_IN()        TRISB6=1

void Write0( void );
void Write1( void );
void WriteCMD( uint CMD );
void RF2_Init( void );
void DelayUs( uint us );
void WriteFSKbyte( uchar DATA );
void DelayMs(uint ms);

__CONFIG(0x3FF2);
/***************************************
初始化端口
***************************************/
void RF2_Init( void )
{
  nSEL=1;
  SDI=1;
  SCK=0;
  FSK=0;
  nSEL_OUT();
  SDI_OUT();
  SDO_IN();
  SCK_OUT();
  FSK_OUT();
}
void main()
{
  uint ChkSum=0;

  RF2_Init( );

  WriteCMD( 0xCC00 );
  WriteCMD( 0x8B61 );
  WriteCMD( 0xA640 );
  WriteCMD( 0xD040 );
  WriteCMD( 0xC823 );
  WriteCMD( 0xC220 );
  WriteCMD( 0xC001 );

  while(1)
```

```
{
  WriteCMD( 0xC039 );

  WriteFSKbyte( 0xAA );
  WriteFSKbyte( 0xAA );
  WriteFSKbyte( 0xAA );
  WriteFSKbyte( 0x2D );
  WriteFSKbyte( 0xD4 );

  WriteFSKbyte( 0x30 );//DATA0
  ChkSum+=0x30;
  WriteFSKbyte( 0x31 );//DATA1
  ChkSum+=0x31;
  WriteFSKbyte( 0x32 );
  ChkSum+=0x32;
  WriteFSKbyte( 0x33 );
  ChkSum+=0x33;
  WriteFSKbyte( 0x34 );
  ChkSum+=0x34;
  WriteFSKbyte( 0x35 );
  ChkSum+=0x35;
  WriteFSKbyte( 0x36 );
  ChkSum+=0x36;
  WriteFSKbyte( 0x37 );
  ChkSum+=0x37;
  WriteFSKbyte( 0x38 );
  ChkSum+=0x38;
  WriteFSKbyte( 0x39 );
  ChkSum+=0x39;
  WriteFSKbyte( 0x3A );
  ChkSum+=0x3A;
  WriteFSKbyte( 0x3B );
  ChkSum+=0x3B;
  WriteFSKbyte( 0x3C );
  ChkSum+=0x3C;
  WriteFSKbyte(0x3D);
  ChkSum+=0x3D;
  WriteFSKbyte( 0x3E );
  ChkSum+=0x3E;
  WriteFSKbyte( 0x3F );//DATA15
  ChkSum+=0x3F;
  ChkSum&=0x0FF;
  WriteFSKbyte( ChkSum );
  WriteFSKbyte( 0xAA );
```

```
    WriteCMD( 0xC001 );
    DelayMs( 1000 );
  }
}
/*************************************
命令字写 0，提供时序
*************************************/
void Write0( void )
{
  SDI=0;
  SCK=0;
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  SCK=1;
  NOP();
}
/****************************************
命令字写 1，提供时序
****************************************/
void Write1( void )
{
  SDI=1;
  SCK=0;
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
```

```
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  NOP();
  SCK=1;
  NOP();
}
/**************************************
写一个字节发送数据
**************************************/
void WriteFSKbyte( uchar DATA )
{
  uchar n=8;
  nSEL=1;
  while(n--)
   {
     while(!nIRQ);
     while(nIRQ);
     if(DATA&0x80)
       FSK=1;
     else
       FSK=0;
     DATA=DATA<<1;
   }
}
/*************************************
写一条命令字
*************************************/
void WriteCMD( uint CMD )
{
  uchar n=16;
  SCK=0;
  nSEL=0;
  while(n--)
   {
     if(CMD&0x8000)
      Write1();
     else
      Write0();
```

```
    CMD=CMD<<1;
   }
  SCK=0;
  nSEL=1;
}
/*******************************************
延时
*******************************************/
void DelayUs( uint us )
{
  uint i;
  while( us-- )
    {
      i=2;
      while( i-- )
        {
          NOP();
        }
    }
}
/*************************************
延时
*************************************/
void DelayMs(uint ms)
{
  uchar i;
  while(ms--)
  {
   i=35;
   while(i--)
   {
     DelayUs(1);
   }
  }
}
```

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