TUSB8041-Q1 Automotive Four-Port USB 3.0 Hub

1 Features

- Four Port USB 3.0 Hub
- USB 2.0 Hub Features
  - Multi Transaction Translator (MTT) Hub: Four Transaction Translators
  - Four Asynchronous Endpoint Buffers Per Transaction Translator
- Supports Battery Charging
  - CDP Mode (Upstream Port Connected)
  - DCP Mode (Upstream Port Unconnected)
  - DCP Mode Complies with Chinese Telecommunications Industry Standard YD/T 1591-2009
  - D+/D- Divider Mode
- Supports Operation as a USB 3.0 or USB 2.0 Compound Device
- Per Port or Ganged Power Switching and Over-Current Notification Inputs
- OTP ROM, Serial EEPROM or I^2C/SMBus Slave Interface for Custom Configurations:
  - VID and PID
  - Port Customizations
  - Manufacturer and Product Strings (not by OTP ROM)
  - Serial Number (not by OTP ROM)
- Application Feature Selection Using Pin Selection or EEPROM/ or I^2C/SMBus Slave Interface
- Provides 128-Bit Universally Unique Identifier (UUID)
- Supports On-Board and In-System OTP/EEPROM Programming Via the USB 2.0 Upstream Port
- Single Clock Input, 24-MHz Crystal or Oscillator
- No Special Driver Requirements; Works Seamlessly on any Operating System with USB Stack Support
- 64-Pin HTQFP Package (PAP)

2 Applications

- Automotive
- Computer Systems
- Docking Stations
- Monitors
- Set-Top Boxes

3 Description

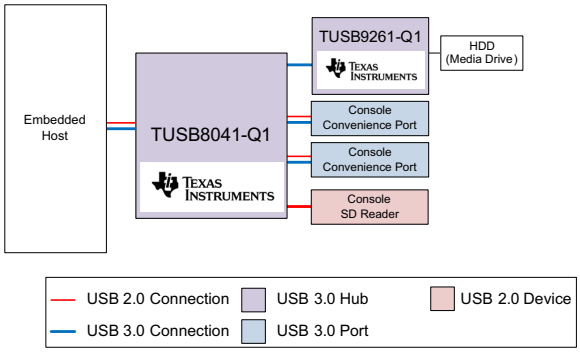
The TUSB8041-Q1 is a four-port USB 3.0 hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB8041-Q1	HTQFP (64)	10.00 mm ×10.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Diagram



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5 Revision History

Date	Revision	Notes
July 2014	*	Initial release.

6 Description (Continued)

The TUSB8041-Q1 supports per port or ganged power switching and over-current protection, and supports battery charging applications.

An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port power controlled hub senses an over-current event, only power to the affected downstream port will be switched off.

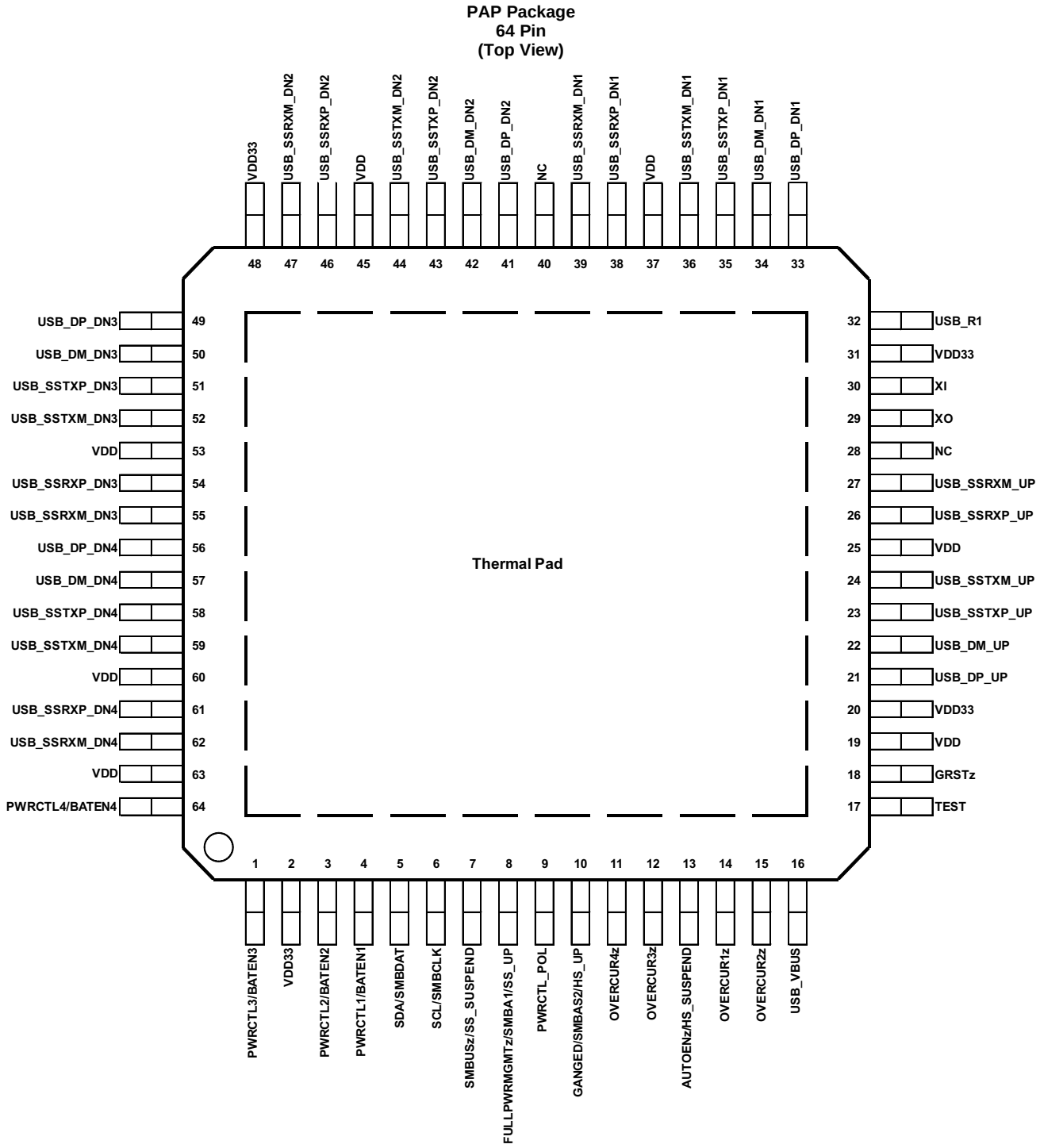
A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off.

The TUSB8041-Q1 downstream ports provide support for battery charging applications by providing Battery Charging Downstream Port (CDP) handshaking support. It also supports a Dedicated Charging Port (DCP) mode when the upstream port is not connected. The DCP mode supports USB devices which support with the USB Battery Charging and Chinese Telecommunications Industry Standard YD/T 1591-2009. In addition, an automatic mode provides transparent support for BC devices and devices supporting Divider Mode charging solutions when the upstream port unconnected.

The TUSB8041-Q1 provides pin strap configuration for some features including battery charging support, and also provides customization though OTP ROM, I^2C EEPROM or via an I^2C/SMBus slave interface for PID, VID, and custom port and phy configurations. Custom string support is also available when using an I^2C EEPROM or the I^2C/SMBus slave interface.

The device is available in a 64-pin PAP package and is designed for operation over the temperature range of -40°C to 85°C.

7 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Clock and Reset Signals			
GRSTz	18	I PU	Global power reset. This reset brings all of the TUSB8041-Q1 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.
XI	30	I	Crystal input. This pin is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	29	O	Crystal output. This pin is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
USB Upstream Signals			
USB_SSTXP_UP	23	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	24	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	26	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	27	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	21	I/O	USB High-speed differential transceiver (positive)
USB_DM_UP	22	I/O	USB High-speed differential transceiver (negative)
USB_R1	32	I	Precision resistor reference. A 9.53-kΩ ±1% resistor should be connected between USB_R1 and GND.
USB_VBUS	16	I	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9-KΩ ±1% resistor, and to ground through a 10-kΩ ±1% resistor from the signal to ground.
USB Downstream Signals			
USB_SSTXP_DN1	35	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN1	36	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN1	38	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN1	39	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN1	33	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN1	34	I/O	USB High-speed differential transceiver (negative)
PWRCTL1/BATEN1	4	I/O, PD	USB Port 1 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 1. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 1 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR1z	14	I, PU	USB Port 1 Over-Current Detection. This pin is used to connect the over current output of the downstream port power switch for Port 1. 0 = An over current event has occurred 1 = An over current event has not occurred This pin can be left unconnected if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN2	43	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN2	44	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN2	46	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN2	47	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN2	41	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN2	42	I/O	USB High-speed differential transceiver (negative)

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PWRCTL2/BATEN2	3	I/O, PD	USB Port 2 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 2. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 2 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR2z	15	I, PU	USB Port 2 Over-Current Detection. This pin is used to connect the over current output of the downstream port power switch for Port 2. 0 = An over current event has occurred 1 = An over current event has not occurred This pin be left unconnected if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN3	51	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN3	52	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN3	54	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN3	55	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN3	49	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN3	50	I/O	USB High-speed differential transceiver (negative)
PWRCTL3/BATEN3	1	I/O, PD	USB Port 3 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 3. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 3 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR3z	12	I, PU	USB Port 3 Over-Current Detection. This pin is used to connect the over current output of the downstream port power switch for Port 3. 0 = An over current event has occurred 1 = An over current event has not occurred This pin can be left unconnected if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN4	58	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN4	59	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN4	61	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN4	62	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN4	56	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN4	57	I/O	USB High-speed differential transceiver (negative)
PWRCTL4/BATEN4	64	I/O, PD	USB Port 4 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 4. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 4 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OVERCUR4z	11	I, PU	USB Port 4 Over-Current Detection. This pin is used to connect the over current output of the downstream port power switch for Port 4. 0 = An over current event has occurred 1 = An over current event has not occurred This pin can be left unconnected if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
I²C/SMBUS Signals			
SCL/SMBCLK	6	I/O, PD	I²C clock/SMBus clock. Function of pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin acts as the serial clock interface for an I²C EEPROM. When SMBUSz = 0, this pin acts as the serial clock interface for an SMBus host. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	5	I/O, PD	I²C data/SMBus data. Function of pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin acts as the serial data interface for an I²C EEPROM. When SMBUSz = 0, this pin acts as the serial data interface for an SMBus host. Can be left unconnected if external interface not implemented.
SMBUSz/SS_SUSPEND	7	I/O, PU	I²C/SMBus mode select/SuperSpeed USB Suspend Status. The value of the pin is sampled at the de-assertion of reset set I²C or SMBus mode as follows: 1 = I²C Mode Selected 0 = SMBus Mode Selected Can be left unconnected if external interface not implemented. After reset, this signal indicates the SuperSpeed USB Suspend status of the upstream port if enabled through the Additional Feature Configuration register. When enabled a value of 1 indicates the connection is suspended.
Test and Miscellaneous Signals			
FULLPWRMGMTz/ SMBA1/SS_UP	8	I/O, PD	Full power management enable/SMBus address bit 1/SuperSpeed USB Connection Status Upstream port. The value of the pin is sampled at the de-assertion of reset to set the power switch control follows: 0 = Power switching and over current inputs supported 1 = Power switching and over current inputs not supported Full power management is the ability to control power to the downstream ports of the TUSB8041-Q1 using PWRCTL[4:1]/BATEN[4:1]. When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus slave address bit 1. Can be left unconnected if full power management and SMBus are not implemented. After reset, this signal indicates the SuperSpeed USB connection status of the upstream port if enabled through the Additional Feature Configuration register. When enabled a value of 1 indicates the upstream port is connected to a SuperSpeed USB capable port.
PWRCTL_POL	9	I/O, PU	Power Control Polarity. The value of the pin is sampled at the de-assertion of reset to set the polarity of PWRCTL[4:1]. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GANGED/SMBA2/ HS_UP	10	I/O, PD	Ganged operation enable/SMBus Address bit 2/HS Connection Status Upstream Port. The value of the pin is sampled at the de-assertion of reset to set the power switch and over current detection mode as follows: 0 = Individual power control supported when power switching is enabled 1 = Power control gangs supported when power switching is enabled When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus slave address bit 2. After reset, this signal indicates the High-speed USB connection status of the upstream port if enabled through the Additional Feature Configuration register. When enabled a value of 1 indicates the upstream port is connected to a High-speed USB capable port.
AUTOENz/ HS_SUSPEND	13	I/O, PU	Automatic Charge Mode Enable/HS Suspend Status. The value of the pin is sampled at the de-assertion of reset to determine if automatic mode is enabled as follows: 0 = Automatic Mode is enabled on ports that are enabled for battery charging when the hub is unconnected. Please note that CDP is not supported on Port 1 when operating in Automatic mode. 1 = Automatic Mode is disabled This value is also used to set the autoEnz bit in the Battery Charging Support Register. After reset, this signal indicates the High-speed USB Suspend status of the upstream port if enabled through the Additional Feature Configuration register. When enabled a value of 1 indicates the connection is suspended.
TEST	17	I, PD	This pin is reserved for factory test.
Power and Ground Signals			
VDD	19, 25, 37, 45 53, 60, 63	PWR	1.1-V power rail
VDD33	2, 20, 31, 48	PWR	3.3-V power rail
VSS	THERMAL PAD	PWR	Ground. Thermal pad must be connected to ground.
NC	28, 40	—	No connect, leave floating

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage Range	V_{DD} Steady-state supply voltage	–0.3	1.4	V
	V_{DD33} Steady-state supply voltage	–0.3	3.8	V
Voltage Range	USB_SSRXP_UP, USB_SSRXN_UP, USB_SSRXP_DN[4:1], USB_SSRXN_DP[4:1] and USB_VBUS terminals	-0.3	1.4	V
	XI terminals	-0.3	2.45	V
	All other terminals	-0.3	3.8	V

8.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 Classification Level H2, all pins(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011 Classification Level C4B	Corner pins	–750	750	
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	1.V1 supply voltage	0.99	1.1	1.26	V
VDD33	3.3V supply voltage	3	3.3	3.6	V
USB_VBUS	Voltage at USB_VBUS PAD	0		1.155	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

8.4 Thermal Information

THERMAL METRIC(1)		TUSB8041-Q1 PAP 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	26.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance(3)	11.5	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	10.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	10.3	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance(7)	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

8.5 Electrical Characteristics, 3.3-V I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(1)	VDD33		2	VDD33	V
V_{IL}	Low-level input voltage(1)	VDD33		0	0.8	V
			JTAG pins only	0	0.55	
V_I	Input voltage			0	VDD33	V
V_O	Output voltage(2)			0	VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis(3)				0.13 x VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = -4 mA	2.4		V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA		0.4	V
I_{OZ}	High-impedance, output current(2)	VDD33	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	VDD33	V_I = 0 to VDD33		±250	µA
I_I	Input current(5)	VDD33	V_I = 0 to VDD33		±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to GRSTz.
(4) Applies to pins with internal pullups/pulldowns.
(5) Applies to external input buffers.

8.6 Timing Requirements, Power-Up

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{d1}	VDD33 stable before VDD stable. There is no timing relationship between VDD33 and VDD.				ms
t_{d2}	VDD and VDD33 stable before de-assertion of GRSTz	3			ms
t_{su_io}	Setup for MISC inputs(1) sampled at the de-assertion of GRSTz	0.1			µs
t_{hd_io}	Hold for MISC inputs(1) sampled at the de-assertion of GRSTz	0.1			µs
t_{VDD33_RAMP}	VDD33 supply ramp requirements	0.2		100	ms
t_{VDD_RAMP}	VDD supply ramp requirements	0.2		100	ms

(1) MISC pins sampled at de-assertion of GRSTZ: FULLPWRMGMTz, GANGED, PWRCTL_POL, SMBUSz, BATEN[4:1], and AUTOENz.

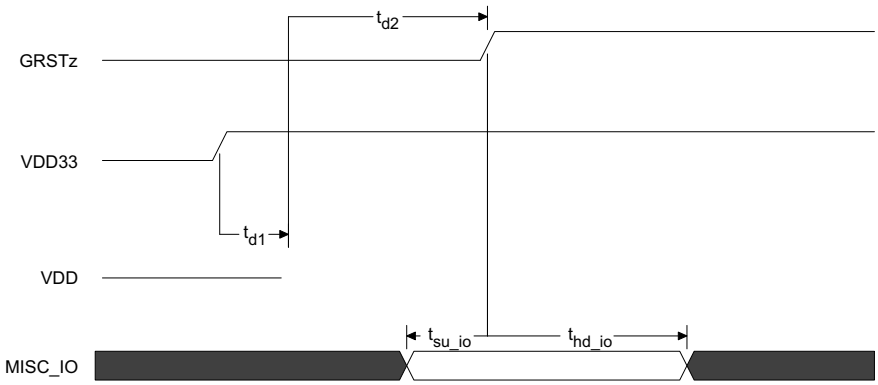


Figure 2. Power-Up Timing Requirements

8.7 Hub Input Supply Current

Typical values measured at T_A = 25°C

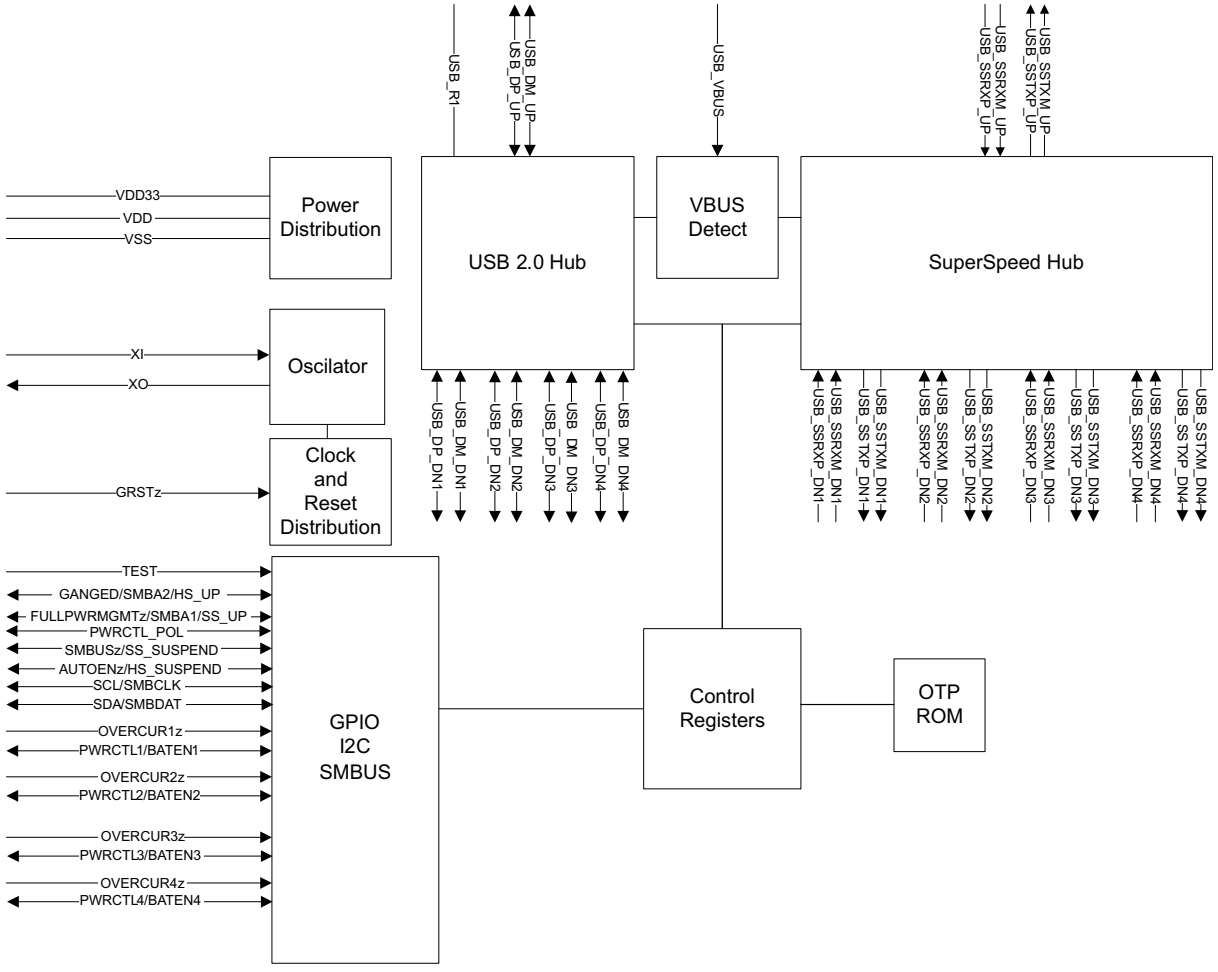
PARAMETER	VDD33	VDD	UNIT
	3.3 V	1.1 V	
LOW POWER MODES			
Power On (after Reset)	2.3	28	mA
Upstream Disconnect	2.3	28	mA
Suspend	2.5	33	mA
ACTIVE MODES (US state / DS State)			
3.0 host / 1 SS Device and Hub in U1 / U2	49	225	mA
3.0 host / 1 SS Device and Hub in U0	49	366	mA
3.0 host / 2 SS Devices and Hub in U1 / U2	49	305	mA
3.0 host / 2 SS Devices and Hub in U0	49	508	mA
3.0 host / 3 SS Devices and Hub in U1 / U2	49	380	mA
3.0 host / 3 SS Devices and Hub in U0	49	661	mA
3.0 host / 4 SS Devices and Hub in U1 / U2	49	455	mA
3.0 host / 4 SS Devices and Hub in U0	49	778	mA
3.0 host / 1 SS Device in U0 and 1 HS Device	85	395	mA
3.0 host / 2 SS Devices in U0 and 2 HS Devices	99	554	mA
2.0 host / HS Device	45	63	mA
2.0 host / 4 HS Devices	76	86	mA

9 Detailed Description

9.1 Overview

The TUSB8041-Q1 is a four-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Battery Charging Features

The TUSB8041 provides support for USB Battery Charging. Battery charging support may be enabled on a per port basis through the REG_6h(batEn[3:0]).

Battery charging support includes both Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

Feature Description (continued)

In addition, to standard DCP mode, the TUSB8041 provides a mode (AUTOMODE) which automatically provides support for DCP devices and devices that support custom charging indication. When in AUTOMODE, the port will automatically switch between a divider mode and the DCP mode depending on the portable device connected. The divided mode places a fixed DC voltage on the ports DP and DM signals which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 5W. The divider mode can be configured to report a high-current setting (up to 10 W) through REG_Ah(HiCurAcpModeEn).

The battery charging mode for each port is dependent on the state of Reg_6h(batEn[n]), the status of the VBUS input, and the state of REG_Ah(autoModeEnz) upstream port as identified in Table 1.

Table 1. TUSB8041 Battery Charging Modes

batEn[n]	VBUS	autoModeEnz	BC Mode Port x (x = n + 1)
0	Don't Care	Don't Care	Don't Care
1	< 4 V	0	Automode(1) (2)
		1	DCP(3) (4)
	> 4 V	Don't Care	CDP(3)

(1) Auto-mode automatically selects divider-mode or DCP mode.
(2) Divider mode can be configured for high-current mode through register or OTP settings.
(3) USB Device is USB Battery Charging Specification Revision 1.2 Compliant
(4) USB Device is Chinese Telecommunications Industry Standard YD/T 1591-2009

9.3.2 USB Power Management

The TUSB8041 can be configured for power switched applications using either per-port or ganged power-enable controls and over-current status inputs.

Power switch support is enabled by REG_5h(fullPwrMgmtz) and the per-port or ganged mode is configured by REG_5h(ganged).

The TUSB8041 supports both active high and active low power-enable controls. The PWRCTL[4:1] polarity is configured by REG_Ah(pwrctlPol).

9.3.3 One Time Programmable (OTP) Configuration

The TUSB8041 allows device configuration through one time programmable non-volatile memory (OTP). The programming of the OTP is supported using vendor-defined USB device requests. For details using the OTP features please contact your TI representative.

The table below provides a list features which may be configured using the OTP.

Table 2. OTP Configurable Features

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_01h	[7:0]	Vendor ID LSB
REG_02h	[7:0]	Vendor ID MSB
REG_03h	[7:0]	Product ID LSB
REG_04h	[7:0]	Product ID MSB
REG_07h	[0]	Port removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_07h	[1]	Port removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_07h	[2]	Port removable configuration for downstream ports 3. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.

Table 2. OTP Configurable Features (continued)

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_07h	[3]	Port removable configuration for downstream ports 4. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_0Ah	[3]	Enable Device Attach Detection..
REG_0Ah	[4]	High-current divider mode enable.
REG_0Bh	[0]	USB 2.0 port polarity configuration for downstream ports 1.
REG_0Bh	[1]	USB 2.0 port polarity configuration for downstream ports 2.
REG_0Bh	[2]	USB 2.0 port polarity configuration for downstream ports 3.
REG_0Bh	[3]	USB 2.0 port polarity configuration for downstream ports 4.
REG_F0h	[3:1]	USB power switch power-on delay.

9.3.4 Clock Generation

The TUSB8041-Q1 accepts a crystal input to drive an internal oscillator or an external clock source. If a clock is provided to XI instead of a crystal, XO is left open. Otherwise, if a crystal is used, the connection needs to follow the guidelines below. Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by shielding C1 and C2 with the clean ground lines.

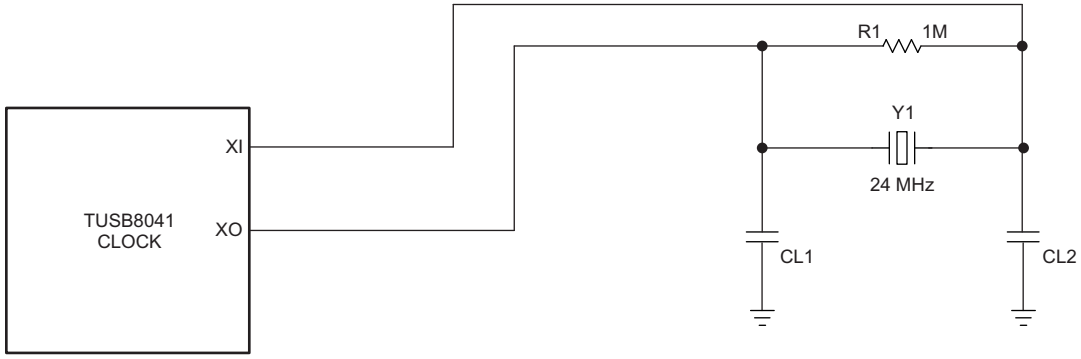


Figure 3. TUSB8041-Q1 Clock

9.3.5 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 pF - 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, a maximum crystal equivalent series resistance (ESR) of 50 Ω is recommended. A parallel load capacitor should be used if a crystal source is used. The exact load capacitance value used depends on the crystal vendor. Refer to application note *Selection and Specification for Crystals for Texas Instruments USB2.0 devices* (SLLA122) for details on how to determine the load capacitance value.

9.3.6 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating.

9.3.7 Power-Up and Reset

The TUSB8041-Q1 does not have specific power sequencing requirements with respect to the core power (VDD) or I/O and analog power (VDD33). The core power (VDD) or I/O power (VDD33) may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

9.4 Device Functional Modes

9.4.1 External Configuration Interface

The TUSB8041-Q1 supports a serial interface for configuration register access. The device may be configured by an attached I^2C EEPROM or accessed as a slave by an SMBus capable host controller. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT pins are pulled up to 3.3 V at the de-assertion of reset. The mode, I^2C master or SMBus slave, is determined by the state of SMBUSz/SS_SUSPEND pin at reset.

9.4.2 I^2C EEPROM Operation

The TUSB8041-Q1 supports a single-master, standard mode (100 kbit/s) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB8041-Q1 reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0.

If the value of the EEPROM contents at byte 00h equals 55h, the TUSB8041-Q1 loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8041-Q1 exits the I^2C mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed. If the hub detected an un-programmed EEPROM (value other than 55h), the hub will enter Programming Mode and a Programming Endpoint within the hub will be enabled.

Note, the bytes located above offset Ah are optional. The requirement for data in those addresses is dependent on the options configured in the Device Configuration, and Device Configuration 2 registers.

For details on I^2C operation refer to the UM10204 I^2C-bus Specification and User Manual.

9.4.3 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8041-Q1 supports read block and write block protocols as a slave-only SMBus device.

The TUSB8041-Q1 slave address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP pin at reset,
- y is the state of FULLPWRMGMTz/SMBA1/SS_UP pin at reset, and
- z is the read/write bit; 1 = read access, 0 = write access.

If the TUSB8041-Q1 is addressed by a host using an unsupported protocol it will not respond. The TUSB8041-Q1 will wait indefinitely for configuration by the SMBus host and will not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements refer to the System Management Bus Specification.

9.5 Register Maps

9.5.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be over-written when the TUSB8041-Q1 is in I^2C or SMBus mode.

Table 3. TUSB8041-Q1 Register Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	No
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved	Yes, program to 00h
0Ah	Device Configuration Register 2	Yes
0Bh	USB 2.0 Port Polarity Control Register	Yes
0Ch-0Fh	Reserved	No
10h-1Fh	UUID Byte [15:0]	No
20h-21h	LangID Byte [1:0]	Yes, if customStrings is set
22h	Serial Number String Length	Yes, if customSerNum is set
23h	Manufacturer String Length	Yes, if customStrings is set
24h	Product String Length	Yes, if customStrings is set
25h-2Fh	Reserved	No
30h-4Fh	Serial Number String Byte [31:0]	Yes, if customSerNum is set
50h-8Fh	Manufacturer String Byte [63:0]	Yes, if customStrings is set
90h-CFh	Product String Byte [63:0]	Yes, if customStrings is set
D0-DFh	Reserved	No
F0h	Additional Feature Configuration Register	Yes
F1-F7h	Reserved	No
F8h	Device Status and Command Register	No
F9-FFh	Reserved	No

9.5.2 ROM Signature Register

Table 4. Register Offset 0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5. Bit Descriptions – ROM Signature Register

Bit	Field Name	Access	Description
7:0	romSignature	RW	ROM Signature Register. This register is used by the TUSB8041-Q1 in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8041-Q1 aborts the EEPROM load and executes with the register defaults.

9.5.3 Vendor ID LSB Register

Table 6. Register Offset 1h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	1	0	0	0	1

Table 7. Bit Descriptions – Vendor ID LSB Register

Bit	Field Name	Access	Description
7:0	vendorIdLsb	RO/RW	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero the value when reading this register shall reflect the OTP ROM value.

9.5.4 Vendor ID MSB Register

Table 8. Register Offset 2h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

Table 9. Bit Descriptions – Vendor ID MSB Register

Bit	Field Name	Access	Description
7:0	vendorIdMsb	RO/RW	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero the value when reading this register shall reflect the OTP ROM value.

9.5.5 Product ID LSB Register

Table 10. Register Offset 3h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	0	0	0	0	0

Table 11. Bit Descriptions – Product ID LSB Register

Bit	Field Name	Access	Description
7:0	productIdLsb	RO/RW	Product ID LSB. Least significant byte of the product ID assigned by Texas Instruments and reported in the SuperSpeed Device descriptor. the default value of this register is 40h representing the LSB of the SuperSpeed product ID assigned by Texas Instruments The value reported in the USB 2.0 Device descriptor is the value of this register bit wise XORed with 00000010b. The value may be over-written to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero the value when reading this register will reflect the OTP ROM value.

9.5.6 Product ID MSB Register

Table 12. Register Offset 4h

Bit No.	7	6	5	4	3	2	1	0
Reset State	1	0	0	0	0	0	0	1

Table 13. Bit Descriptions – Product ID MSB Register

Bit	Field Name	Access	Description
7:0	productIdMsb	RO/RW	Product ID MSB. Most significant byte of the product ID assigned by Texas Instruments; the default value of this register is 81h representing the MSB of the product ID assigned by Texas Instruments. The value may be over-written to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register will reflect the OTP ROM value.

9.5.7 Device Configuration Register

Table 14. Register Offset 5h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	X	X	0	0

Table 15. Bit Descriptions – Device Configuration Register

Bit	Field Name	Access	Description
7	customStrings	RW	Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers 0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only 1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0.
6	customSernum	RW	Custom serial number enable. This bit controls the ability to write to the serial number registers. 0 = The Serial Number String Length and Serial Number String registers are read only 1 = Serial Number String Length and Serial Number String registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0.
5	u1u2Disable	RW	U1 U2 Disable. This bit controls the U1/U2 support. 0 = U1/U2 support is enabled 1 = U1/U2 support is disabled, the TUSB8041-Q1 will not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP. After receiving or sending an FLPMA LMP, it will continue to enable U1 and U2 according to USB 3.0 protocol until it gets a power-on reset or is disconnected on its upstream port. When the TUSB8041-Q1 is in I^2C mode, the TUSB8041-Q1 loads this bit from the contents of the EEPROM. When the TUSB8041-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
4	RSVD	RO	Reserved. This bit is reserved and returns 1 when read.

Table 15. Bit Descriptions – Device Configuration Register (continued)

3	ganged	RW	Ganged. This bit is loaded at the de-assertion of reset with the value of the GANGED/SMBA2/HS_UP pin. 0 = When fullPwrMgmtz = 0, each port is individually power switched and enabled by the PWRCTL[4:1]/BATEN[4:1] pins 1 = When fullPwrMgmtz = 0, the power switch control for all ports is ganged and enabled by the PWRCTL[4:1]/BATEN1 pin When the TUSB8041-Q1 is in I^2C mode, the TUSB8041-Q1 loads this bit from the contents of the EEPROM. When the TUSB8041-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
2	fullPwrMgmtz	RW	Full Power Management. This bit is loaded at the de-assertion of reset with the value of the FULLPWRMGMTz/SMBA1/SS_UP pin. 0 = Port power switching status reporting is enabled 1 = Port power switching status reporting is disabled When the TUSB8041-Q1 is in I^2C mode, the TUSB8041-Q1 loads this bit from the contents of the EEPROM. When the TUSB8041-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
1	RSVD	RW	Reserved. This field is reserved and should not be altered from the default.
0	RSVD	RO	Reserved. This field is reserved and returns 0 when read.

9.5.8 Battery Charging Support Register

Table 16. Register Offset 6h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

Table 17. Bit Descriptions – Battery Charging Support Register

Bit	Field Name	Access	Description
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	batEn[3:0]	RW	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. 0 = The port is not enabled for battery charging support features 1 = The port is enabled for battery charging support features Each bit corresponds directly to a downstream port, i.e. batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2. The default value for these bits are loaded at the de-assertion of reset with the value of PWRCTL/BATEN[3:0]. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host.

9.5.9 Device Removable Configuration Register

Table 18. Register Offset 7h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

Table 19. Bit Descriptions – Device Removable Configuration Register

Bit	Field Name	Access	Description
7	customRmbl	RW	Custom Removable. This bit controls the ability to write to the port removable bits. 0 = rmbl[3:0] are read only and the values are loaded from the OTP ROM 1 = rmbl[3:0] are read/write and can be loaded by EEPROM or written by SMBus This bit may be written simultaneously with rmbl[3:0].
6:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	rmbl[3:0]	RW	Removable. The bits in this field indicate whether a device attached to downstream ports 4 through 1 are removable or permanently attached. 0 = The device attached to the port is not removable 1 = The device attached to the port is removable Each bit corresponds directly to a downstream port n + 1, i.e. rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, etc. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this filed reflects the inverted values of the OTP ROM non_rmb[3:0] field.

9.5.10 Port Used Configuration Register

Table 20. Register Offset 8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	1	1	1

Table 21. Bit Descriptions – Port Used Configuration Register

Bit	Field Name	Access	Description
7:4	RSVD	RO	Reserved. Read only.
3:0	used[3:0]	RW	Used. The bits in this field indicate whether a port is enabled. 0 = The port is disabled 1 = The port is enabled Each bit corresponds directly to a downstream port, i.e. used0 corresponds to downstream port 1, used1 corresponds to downstream port 2, etc. All combinations are supported with the exception of both ports 1 and 3 marked as disabled.

9.5.11 Device Configuration Register 2

Table 22. Register Offset Ah

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	X	0	0	0	X	0

Table 23. Bit Descriptions – Device Configuration Register 2

Bit	Field Name	Access	Description
7	Reserved	RO	Reserved. Read-only, returns 0 when read.
6	customBCfeatures	RW	Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls. 0 = The HiCurAcpModeEn and cpdEN bits are read only and the values are loaded from the OTP ROM. 1 = The HiCurAcpModeEn and cpdEN, bits are read/write and can be loaded by EEPROM or written by SMBus. from this register. This bit may be written simultaneously with HiCurAcpModeEn and cpdEN.
5	pwrctlPol	RW	Power enable polarity. This bit is loaded at the de-assertion of reset with the value of the PWRCTL_POL pin. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high When the TUSB8041-Q1 is in I^2C mode, the TUSB8041-Q1 loads this bit from the contents of the EEPROM. When the TUSB8041-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
4	HiCurAcpModeEn	RO/RW	High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. 0 = High current divider mode disabled 1 = High current divider mode enabled This bit is read only unless the customBCfeatures bit is set to 1. If customBCfeatures is 0, the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit.
3	cpdEN	RORW	Enable Device Attach Detection. This bit enables device attach detection (aka, cell phone detect) when autoMode is enabled. 0 = Device Attach detect is disabled in automode. 1 = Device Attach detect is enabled in automode.. This bit is read only unless the customBCfeatures bit is set to 1. If customBCfeatures is 0 the value of this bit reflects the value of the OTP ROM cpdEN bit.
2	dsportEcr_en	RW	DSPORT ECR Enable. This bit enables full implementation of the DSPORT ECR (April 2013). 0 = The DSPORT ECR (April 2013) is enabled with exception of the following: Changes related to when CCS bit is set upon entering U0, and Changes related to avoiding or reporting compliance mode entry 1 = The full DSPORT ECR (April 2013) is enabled. The default value of this bit is 0. The value returned from this register will be the OR of this bit and the OTP ROM dsport_ecr_en bit.

Table 23. Bit Descriptions – Device Configuration Register 2 (continued)

1	autoModeEnz	RW	Automatic Mode Enable. This bit is loaded at the de-assertion of reset with the value of the AUTOENz/HS_SUSPEND pin. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions: 0 = Automatic mode battery charging features are enabled. 1 = Automatic mode is disabled; only Battery Charging DCP and CDP mode is supported. NOTE: When the upstream port is connected, Battery Charging CDP mode will be supported on all ports that enabled for battery charging support regardless of the value of this bit with the exception of Port 1. CDP on Port 1 is not supported when Automatic Mode is enabled.
0	RSVD	RO	Reserved. Read only, returns 0 when read.

9.5.12 USB 2.0 Port Polarity Control Register

Table 24. Register Offset Bh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 25. Bit Descriptions – USB 2.0 Port Polarity Control Register

Bit	Field Name	Access	Description
7	customPolarity	RW	Custom USB 2.0 Polarity. This bit controls the ability to write the p[4:0]_usb2pol bits. 0 = The p[4:0]_usb2pol bits are read only and the values are loaded from the OTP ROM. 1 = The p[4:0]_usb2pol bits are read/write and can be loaded by EEPROM or written by SMBus. from this register This bit may be written simultaneously with the p[4:0]_usb2pol bits
6:5	RSVD	RO	Reserved. Read only, returns 0 when read.
4	p4_usb2pol	RO/RW	Downstream Port 4 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p4_usb2pol bit.
3	p3_usb2pol	RO/RW	Downstream Port 3 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p3_usb2pol bit.
2	p2_usb2pol	RO/RW	Downstream Port 2 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p2_usb2pol bit.

Table 25. Bit Descriptions – USB 2.0 Port Polarity Control Register (continued)

1	p1_usb2pol	RORW	Downstream Port 1 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p1_usb2pol bit.
0	p0_usb2pol	RO/RW	Upstream Port DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p0_usb2pol bit.

9.5.13 UUID Registers

Table 26. Register Offset 10h-1Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	X	X	X	X	X	X

Table 27. Bit Descriptions – UUID Byte N Register

Bit	Field Name	Access	Description
7:0	uuidByte[n]	RO	UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

9.5.14 Language ID LSB Register

Table 28. Register Offset 20h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	1

Table 29. Bit Descriptions – Language ID LSB Register

Bit	Field Name	Access	Description
7:0	langIdLsb	RO/RW	Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8041-Q1 only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

9.5.15 Language ID MSB Register

Table 30. Register Offset 21h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

Table 31. Bit Descriptions – Language ID MSB Register

Bit	Field Name	Access	Description
7:0	langIdMsb	RO/RW	Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8041-Q1 only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

9.5.16 Serial Number String Length Register

Table 32. Register Offset 22h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	1	0	0	0

Table 33. Bit Descriptions – Serial Number String Length Register

Bit	Field Name	Access	Description
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RO/RW	Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24 byte serial number string is supported. The maximum string length is 32 bytes. When customSernum is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

9.5.17 Manufacturer String Length Register

Table 34. Register Offset 23h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 35. Bit Descriptions – Manufacturer String Length Register

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RO/RW	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

9.5.18 Product String Length Register

Table 36. Register Offset 24h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 37. Bit Descriptions – Product String Length Register

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RO/RW	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 3 from the data contained in the Product String registers.

9.5.19 Serial Number String Registers

Table 38. Register Offset 30h-4Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	x	x	x	x	x	x

Table 39. Bit Descriptions – Serial Number Registers

Bit	Field Name	Access	Description
7:0	serialNumber[n]	RO/RW	Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is assigned by TI. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host.

9.5.20 Manufacturer String Registers

Table 40. Register Offset 50h-8Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 41. Bit Descriptions – Manufacturer String Registers

Bit	Field Name	Access	Description
7:0	mfgStringByte[n]	RW	Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

9.5.21 Product String Registers

Table 42. Register Offset 90h-CFh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 43. Bit Descriptions – Product String Byte N Register

Bit	Field Name	Access	Description
7:0	prodStringByte[n]	RO/RW	Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

9.5.22 Additional Feature Configuration Register

Table 44. Register Offset F0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 45. Bit Descriptions – Additional Feature Configuration Register

Bit	Field Name	Access	Description
7:5	RSVD	RO	Reserved. Read only, returns 0 when read.
4	stsOutputEn	RO/RW	Status output enable. This bit enables the HS, HS_SUSPEND, SS, and SS_SUSPEND outputs.. 0 = HS, HS_SUSPEND, SS, and SS_SUSPEND outputs are disabled and tri-stated. 1 = HS, HS_SUSPEND, SS, and SS_SUSPEND outputs are enabled. This field may be over-written by EEPROM contents or by an SMBus Host.
3:1	pwronTime	RW	Power On Delay Time. When OTP ROM pwronTime field is all zero , this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from a custom charging mode to Dedicated Charging Port Mode. The nominal timing is defined as follows: TPWRON_EN = (pwronTime + 1) x 200 ms (1) This field may be over-written by EEPROM contents or by an SMBus host.
0	usb3spreadDis	RW	USB3 Spread Spectrum Disable. This bit allows firmware to disable the spread spectrum function of the USB3 phy PLL. 0 = Spread spectrum function is enabled 1= Spread spectrum function is disabled

9.5.23 Device Status and Command Register

Table 46. Register Offset F8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 47. Bit Descriptions – Device Status and Command Register

Bit	Field Name	Access	Description
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1	smbusRst	RSU	SMBus interface reset. This bit loads the registers back to their GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	RCU	Configuration active. This bit indicates that configuration of the TUSB8041-Q1 is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB8041-Q1 shall not connect on the upstream port while this bit is 1. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

10 Applications and Implementation

10.1 Application Information

The TUSB8041-Q1 is a four-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low speed connections on the downstream port. The TUSB8041-Q1 can be used in any application that needs additional USB compliant ports. For example, a specific notebook may only have two downstream USB ports. By using the TUSB8041-Q1, the notebook can increase the downstream port count to five.

10.2 Typical Application

10.2.1 Discrete USB Hub Product

A common application for the TUSB8041-Q1 is as a self powered standalone USB hub product. The product is powered by an external 5V DC Power adapter. In this application, using a USB cable TUSB8041-Q1's upstream port is plugged into a USB Host controller. The downstream ports of the TUSB8041-Q1 are exposed to users for connecting USB hard drives, cameras, flash drives, and so forth.

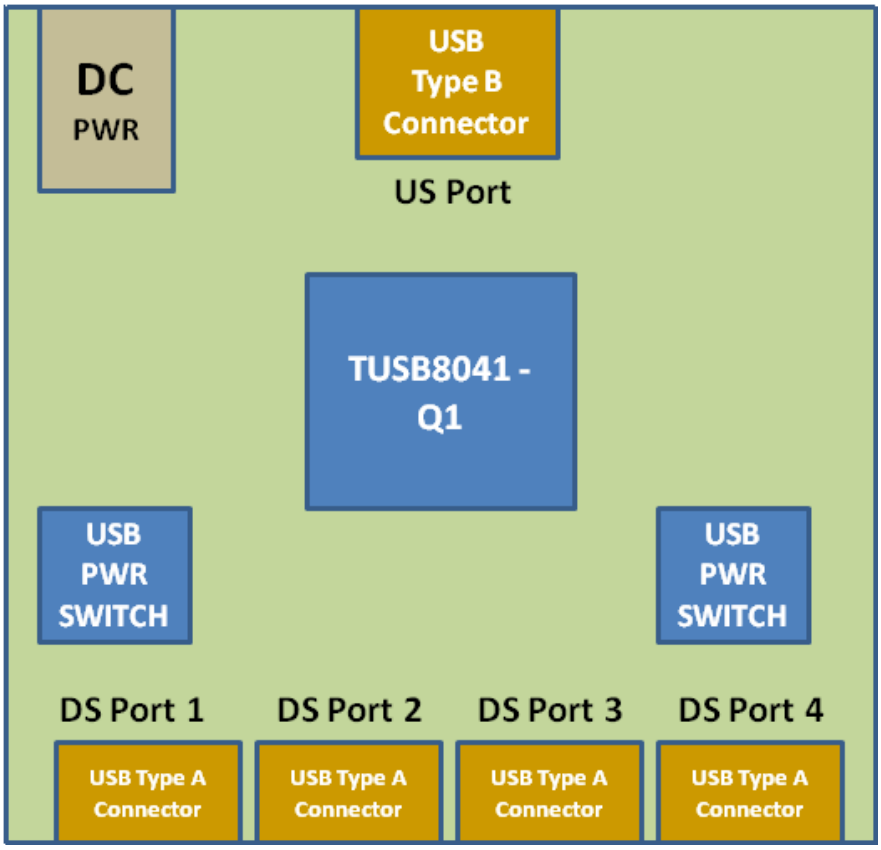


Figure 4. Discrete USB Hub Product

Typical Application (continued)

10.2.1.1 Design Requirements

Table 48. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD Supply	1.1V
VDD33 Supply	3.3V
Upstream Port USB Support (SS, HS, FS)	SS, HS, FS
Downstream Port 1 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 2 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 3 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 4 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Number of Removable Downstream Ports	4
Number of Non-Removable Downstream Ports	0
Full Power Management of Downstream Ports	Yes. (FULLPWRMGMTZ = 0)
Individual Control of Downstream Port Power Switch	Yes. (GANGED = 0)
Power Switch Enable Polarity	Active High. (PWRCTL_POL = 0)
Battery Charge Support for Downstream Port 1	Yes
Battery Charge Support for Downstream Port 2	Yes
Battery Charge Support for Downstream Port 3	Yes
Battery Charge Support for Downstream Port 4	Yes
I2C EEPROM Support	No.
24MHz Clock Source	Crystal

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Upstream Port Implementation

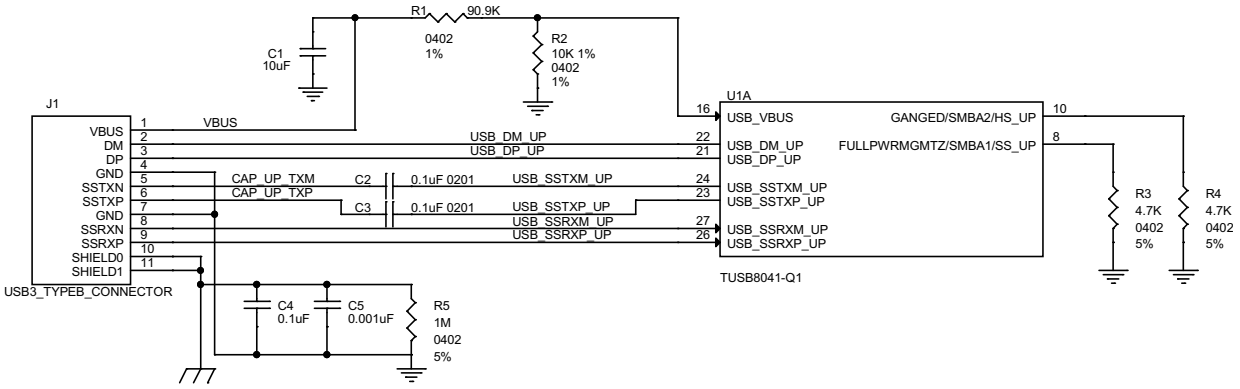


Figure 5. Upstream Port Implementation

The upstream of the TUSB8041-Q1 is connected to a USB3 Type B connector. This particular example has GANGED pin and FULLPWRMGMTZ pin pulled low which results in individual power support each downstream port. The VBUS signal from the USB3 Type B connector is feed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements

10.2.1.2.2 Downstream Port 1 Implementation

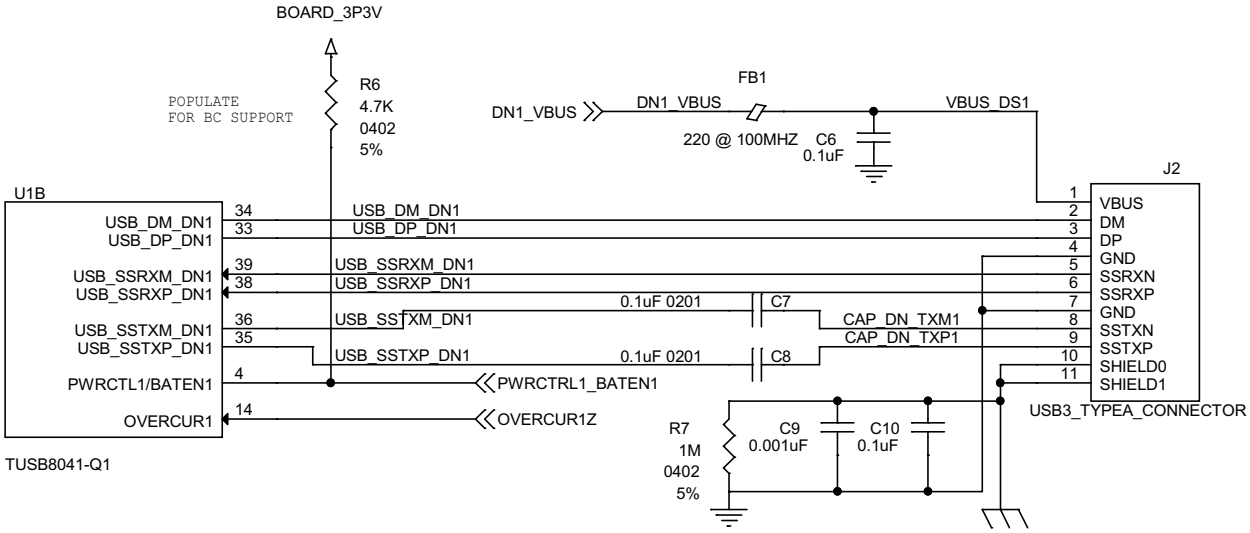


Figure 6. Downstream Port 1 Implementation

The downstream port 1 of the TUSB8041-Q1 is connected to a USB3 Type A connector. With BATEN1 pin pulled up, Battery Charge support is enabled for Port 1. If Battery Charge support is not needed, then pull-up resistor on BATEN1 should be uninstalled.

10.2.1.2.3 Downstream Port 2 Implementation

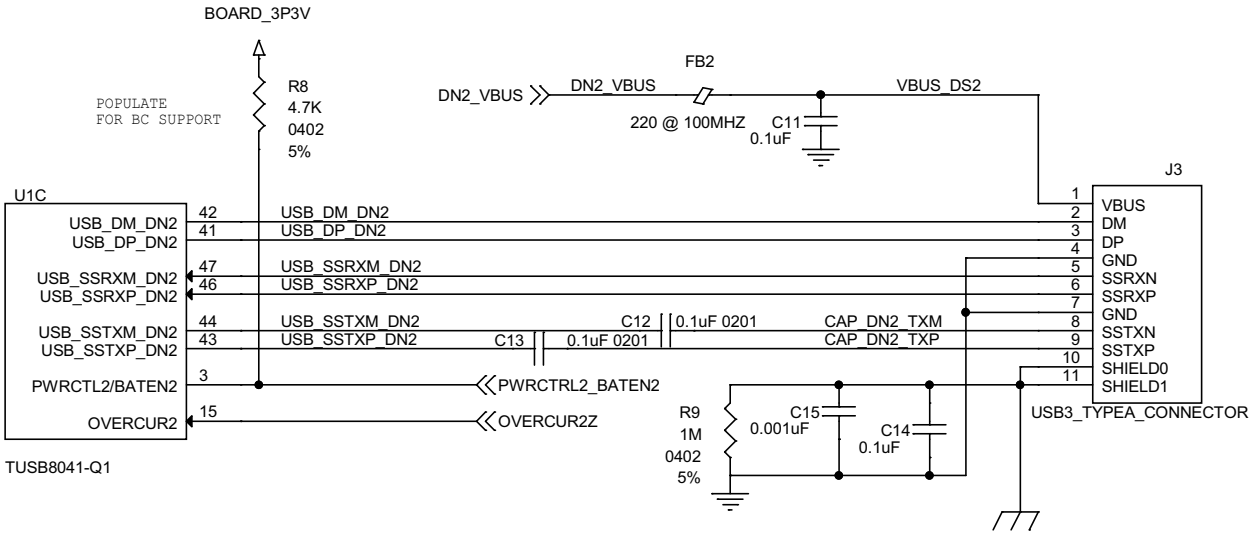


Figure 7. Downstream Port 2 Implementation

The downstream port 2 of the TUSB8041-Q1 is connected to a USB3 Type A connector. With BATEN2 pin pulled up, Battery Charge support is enabled for Port 2. If Battery Charge support is not needed, then pull-up resistor on BATEN2 should be uninstalled.

10.2.1.2.4 Downstream Port 3 Implementation

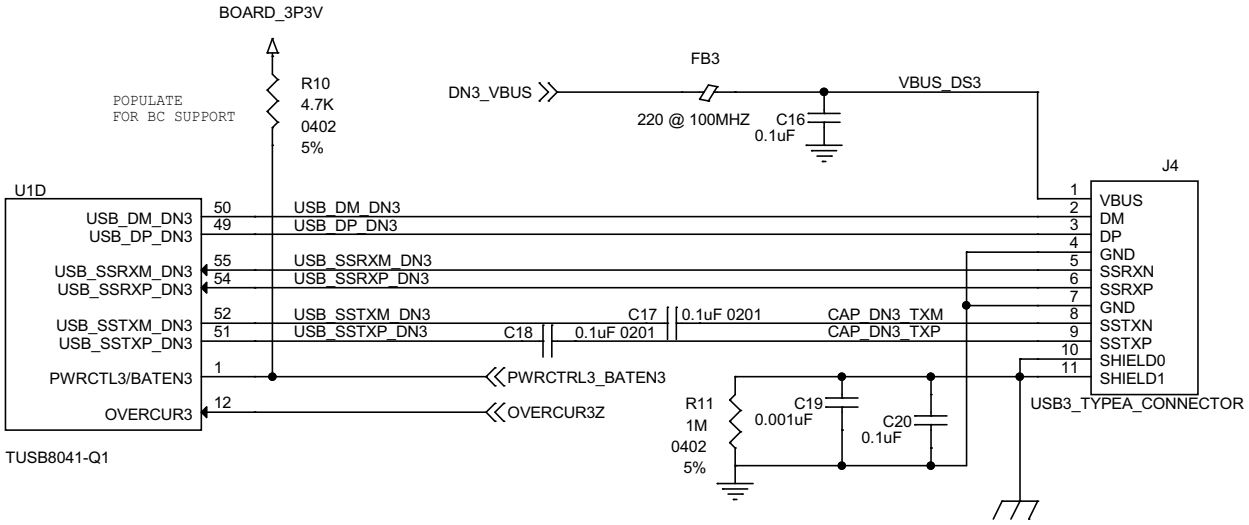


Figure 8. Downstream Port 3 Implementation

The downstream port3 of the TUSB8041-Q1 is connected to a USB3 Type A connector. With BATEN3 pin pulled up, Battery Charge support is enabled for Port 3. If Battery Charge support is not needed, then pull-up resistor on BATEN3 should be uninstalled.

10.2.1.2.5 Downstream Port 4 Implementation

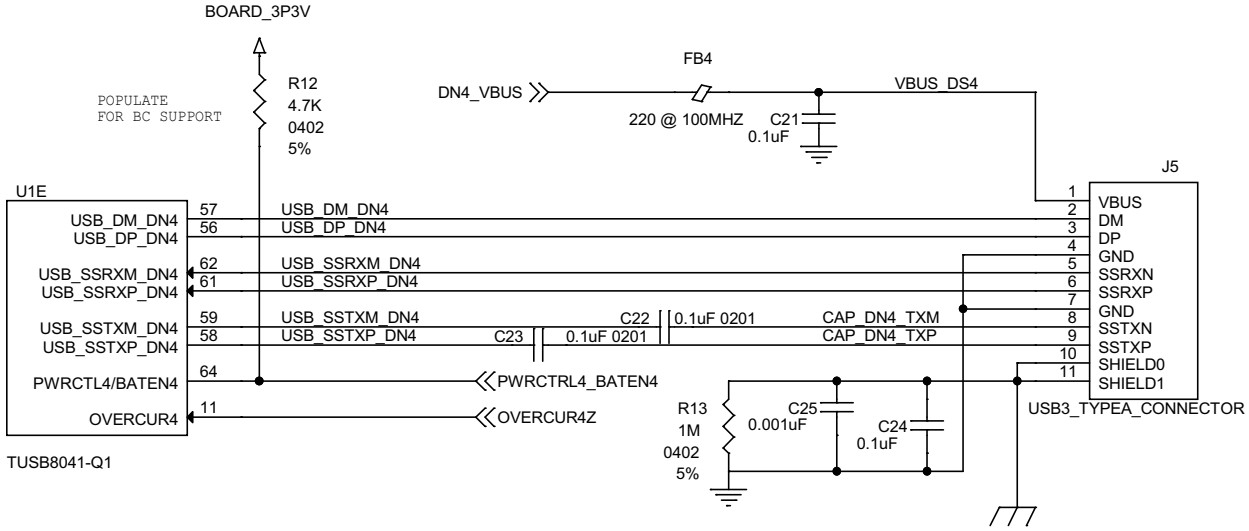


Figure 9. Downstream Port 4 Implementation

The downstream port 4 of the TUSB8041-Q1 is connected to a USB3 Type A connector. With BATEN4 pin pulled up, Battery Charge support is enabled for Port 4. If Battery Charge support is not needed, then pull-up resistor on BATEN4 should be uninstalled.

10.2.1.2.6 VBUS Power Switch Implementation

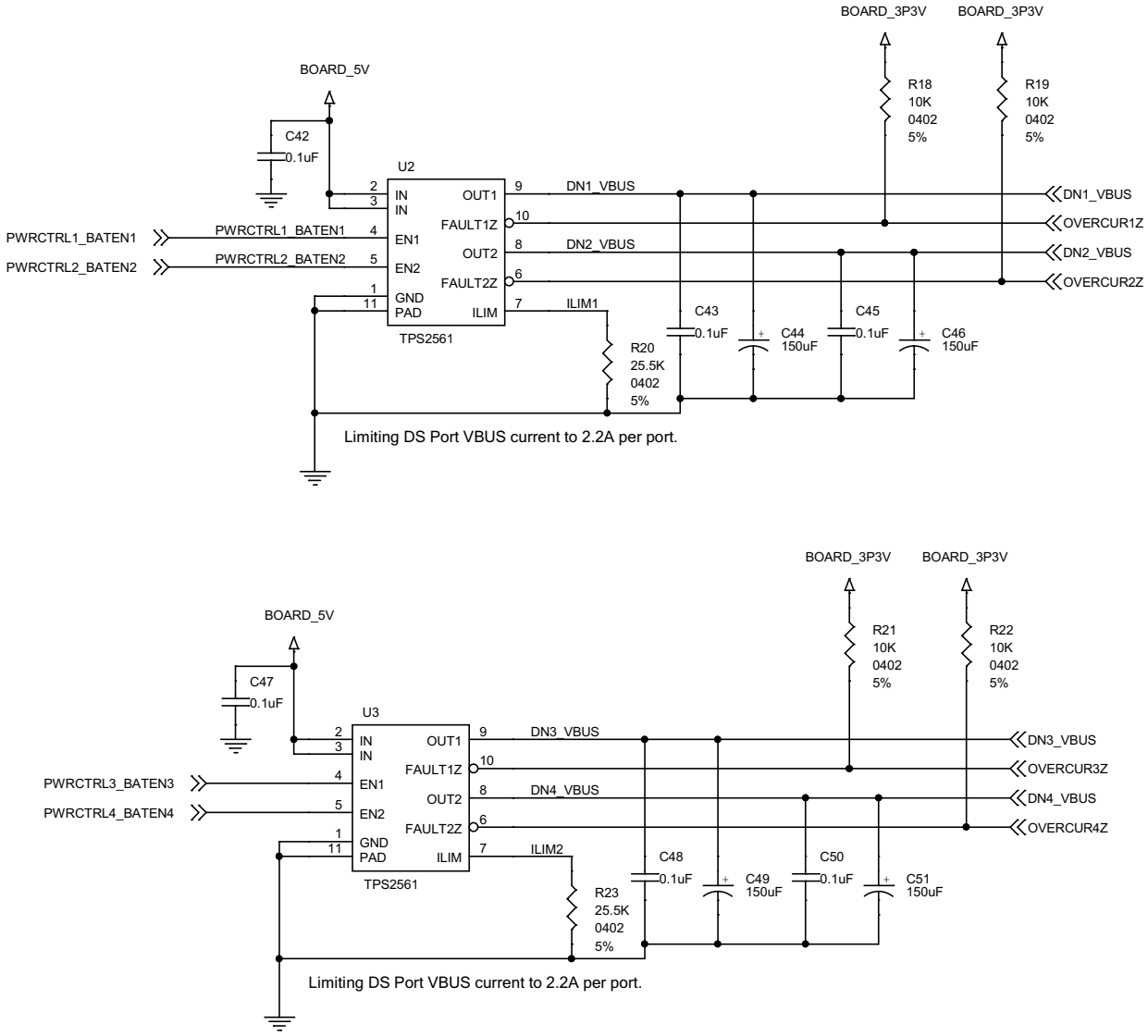


Figure 10. VBUS Power Switch Implementation

This particular example uses the Texas Instruments TPS2561 Dual Channel Precision Adjustable Current-Limited power switch. For details on this power switch or other power switches available from Texas Instruments, refer to the Texas Instruments website.

10.2.1.2.7 Clock, Reset, and Misc

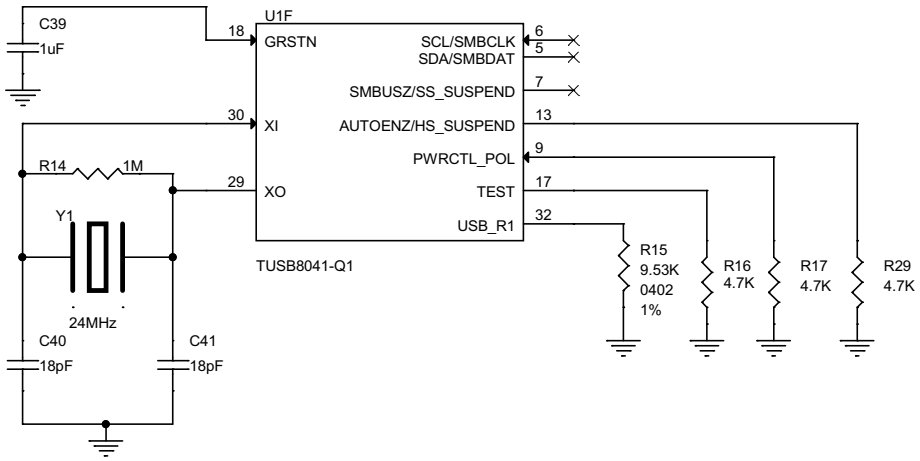


Figure 11. Clock, Reset, and Misc

The PWRCTL_POL is pulled down which will result in active high power enable (PWRCTL1, PWRCTL2, PWRCTL3, and PWRCTL4) for a USB VBUS power switch. The 1µF capacitor on the GRSTN pin can only be used if the VDD11 supply is stable before the VDD33 supply. The depending on the supply ramp of the two supplies the capacitor may have to be adjusted.

10.2.1.2.8 TUSB8041-Q1 Power Implementation

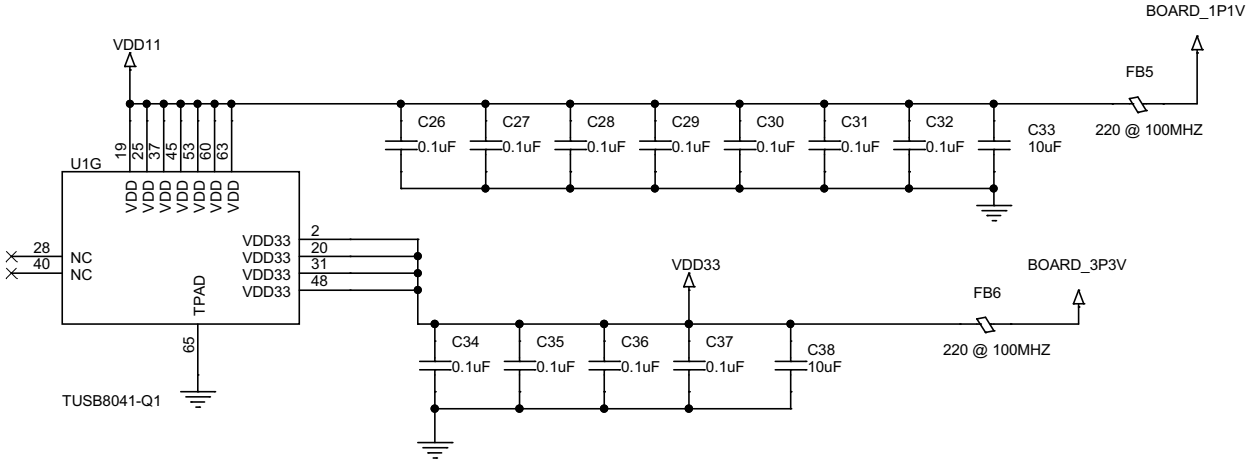


Figure 12. TUSB8041-Q1 Power Implementation

10.2.1.3 Application Curves

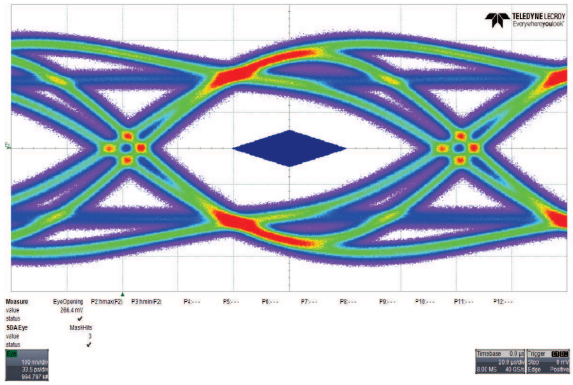


Figure 13. Upstream Port

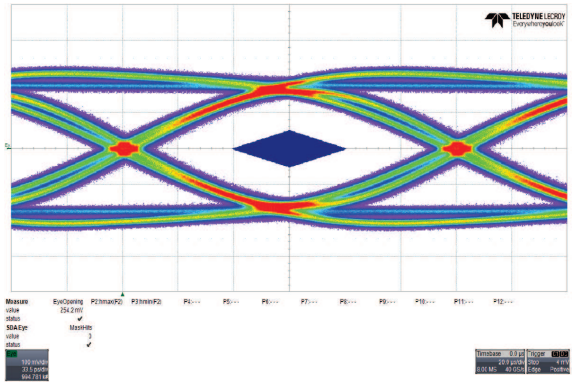


Figure 14. Downstream Port 1

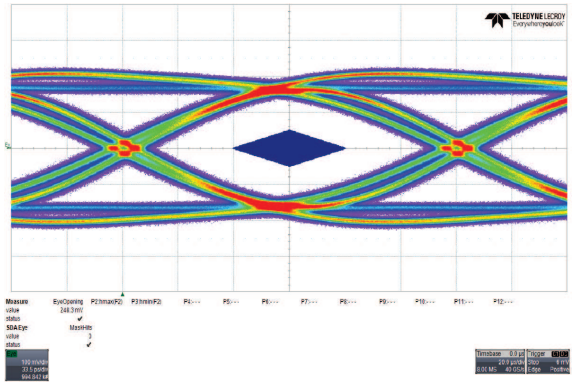


Figure 15. Downstream Port 2

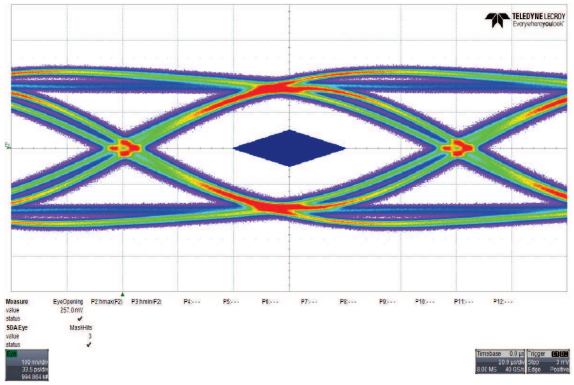


Figure 16. Downstream Port 3

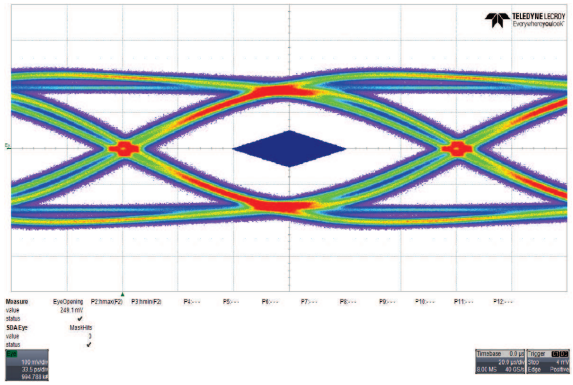


Figure 17. Downstream Port 4

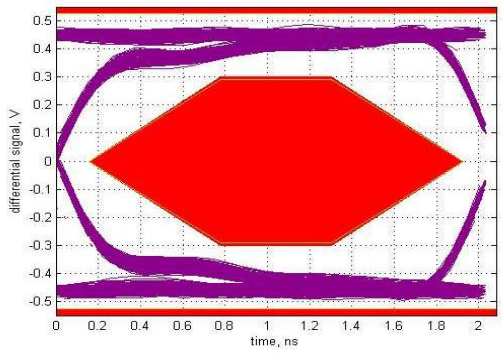


Figure 18. High-Speed Upstream Port

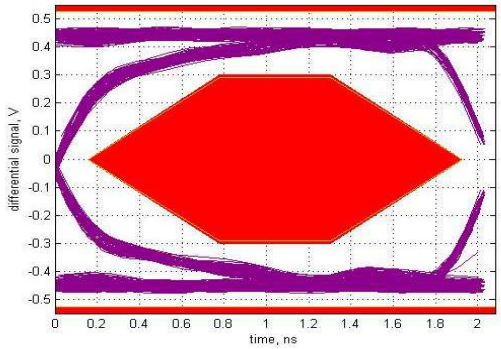


Figure 19. High-Speed Downstream Port 1

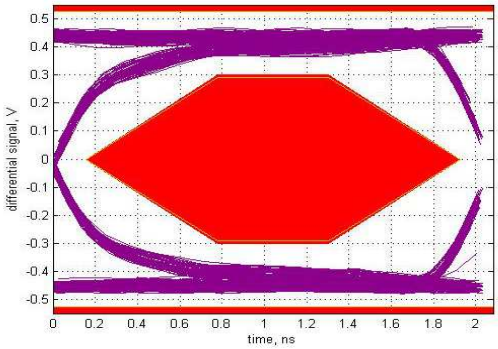


Figure 20. High-Speed Downstream Port 2

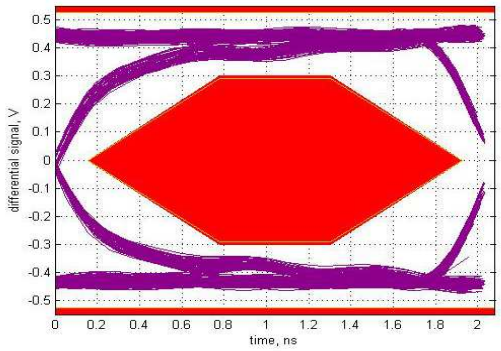


Figure 21. High-Speed Downstream Port 3

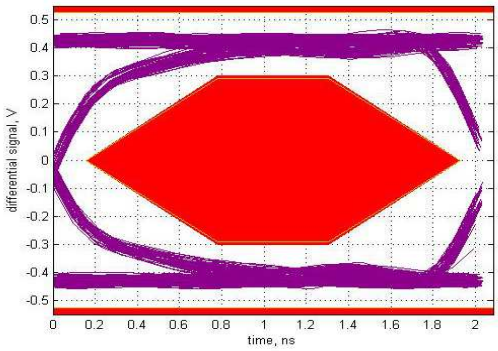


Figure 22. High-Speed Downstream Port 4

11 Power Supply Recommendations

11.1 TUSB8041-Q1 Power Supply

V_{DD} should be implemented as a single power plane, as should V_{DD33}.

- The V_{DD} pins of the TUSB8041-Q1 supply 1.1 V (nominal) power to the core of the TUSB8041-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the core voltage regulator may need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The V_{DD33} pins of the TUSB8041-Q1 supply 3.3 V power rail to the I/O of the TUSB8041-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10 µF capacitor or 1 µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB8041-Q1 power pins as possible with an optimal grouping of two of differing values per pin.

11.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5V and up to 900 mA per port. Downstream port power switches can be controlled by the TUSB8041-Q1 signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 µF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1µF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

11.3 Ground

It is recommended that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB8041-Q1 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

12 Layout

12.1 Layout Guidelines

12.1.1 Placement

1. 9.53K +/-1% resistor connected to pin USB_R1 should be placed as close as possible to the TUSB8041-Q1.
2. A 0.1 µF should be placed as close as possible on each VDD and VDD33 power pin.
3. The 100 nF capacitors on the SSTXP and SSTXM nets should be placed close to the USB connector (Type A, Type B, and so forth).
4. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
5. If a crystal is used, it must be placed as close as possible to the TUSB8041-Q1's XI and XO pins.
6. Place voltage regulators as far away as possible from the TUSB8041-Q1, the crystal, and the differential pairs.
7. In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.

12.1.2 Package Specific

1. The TUSB8041-Q1 package has a 0.5-mm pin pitch.
2. The TUSB8041-Q1 package has a 4.64-mm x 4.64-mm thermal pad. This thermal pad must be connected to ground through a system of vias.
3. All vias under device, except for those connected to thermal pad, should be solder masked to avoid any potential issues with thermal pad layouts.

12.1.3 Differential Pairs

This section describes the layout recommendations for all the TUSB8041-Q1 differential pairs: USB_DP_XX, USB_DM_XX, USB_SSTXP_XX, USB_SSTXM_XX, USB_SSRXP_XX, and USB_SSRXM_XX.

1. Must be designed with a differential impedance of 90 Ω +/- 10%.
2. In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width. Separating with ground as depicted in the layout example will also help minimize cross talk.
3. Route all differential pairs on the same layer adjacent to a solid ground plane.
4. Do not route differential pairs over any plane split.
5. Adding test points will cause impedance discontinuity and will therefore negative impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
6. Avoid 90 degree turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SS differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
8. Match the etch lengths of the differential pair traces (i.e. DP and DM or SSRXP and SSRXM or SSTXP and SSTXM). There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
9. The etch lengths of the differential pair groups do not need to match (i.e. the length of the SSRX pair to that of the SSTX pair), but all trace lengths should be minimized.
10. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB8041-Q1 device.
11. To ease routing, the polarity of the SS differential pairs can be swapped. This means that SSTXP can be routed to SSTXM or SSRXM can be routed to SSRXP.

Layout Guidelines (continued)

12. To ease routing of the USB2 DP and DM pair, the polarity of these pins can be swapped. If this is done, the appropriate Px_usb2pol register, where x = 0, 1, 2, 3, or 4, must be set.
13. Do not place power fuses across the differential pair traces.

12.2 Layout Examples

12.2.1 Upstream Port

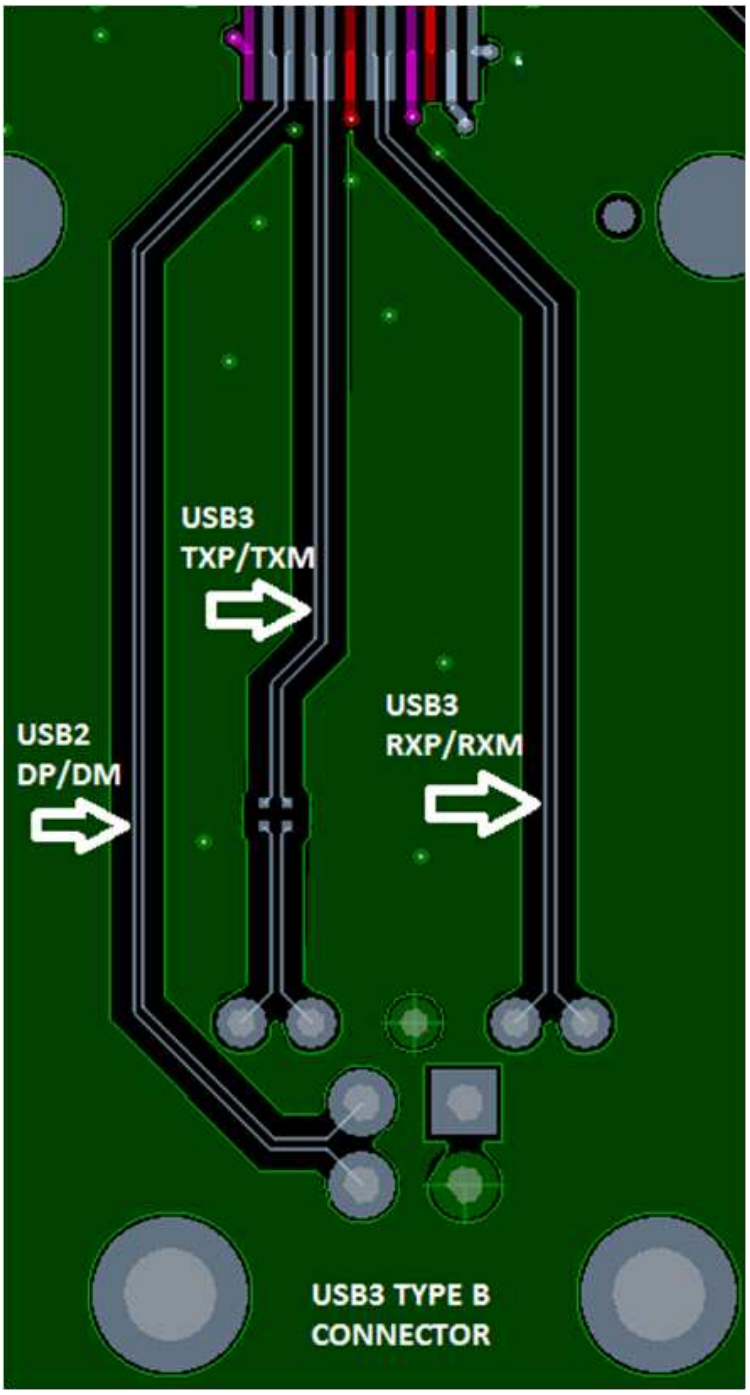


Figure 23. Example Routing of Upstream Port

Layout Examples (continued)

12.2.2 Downstream Port

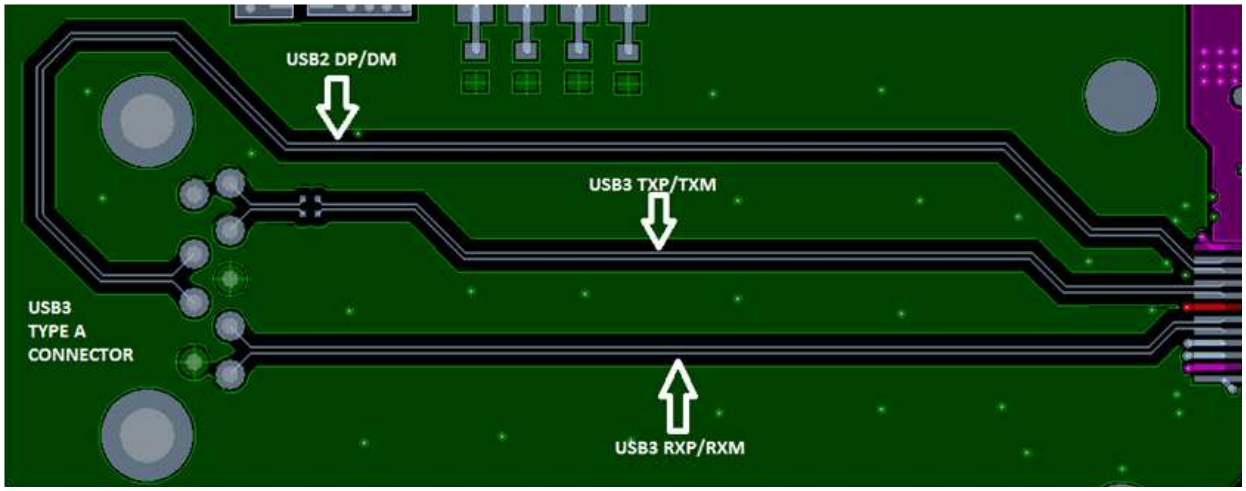


Figure 24. Example Routing of Downstream Port

The remaining three downstream ports routing can be similar to the example provided.

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB8041IPAPQ1	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8041I Q1	Samples
TUSB8041IPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8041I Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB8041-Q1 :

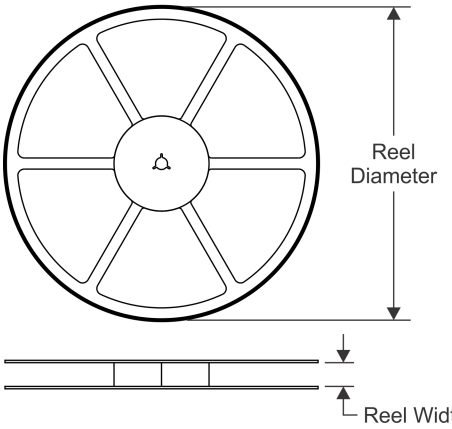
- Catalog: TUSB8041

NOTE: Qualified Version Definitions:

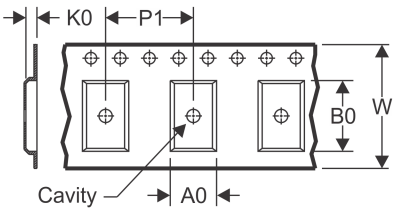
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

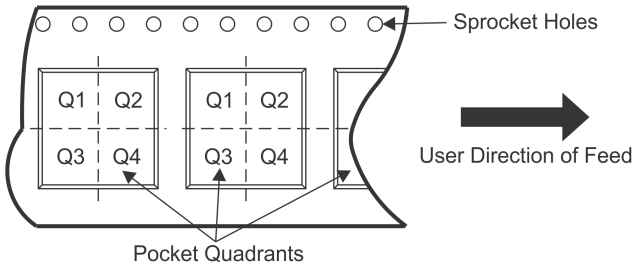


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

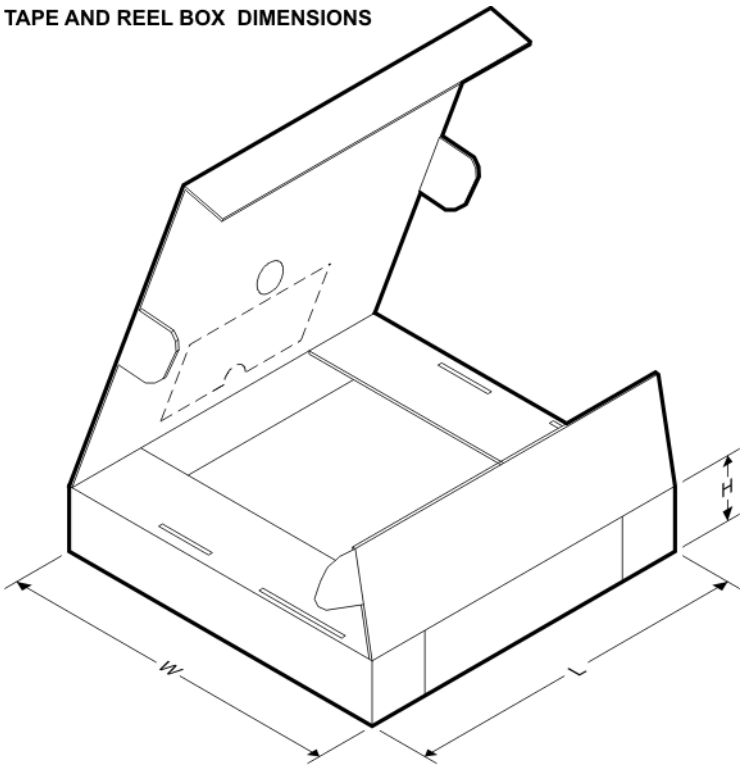
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB8041IPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

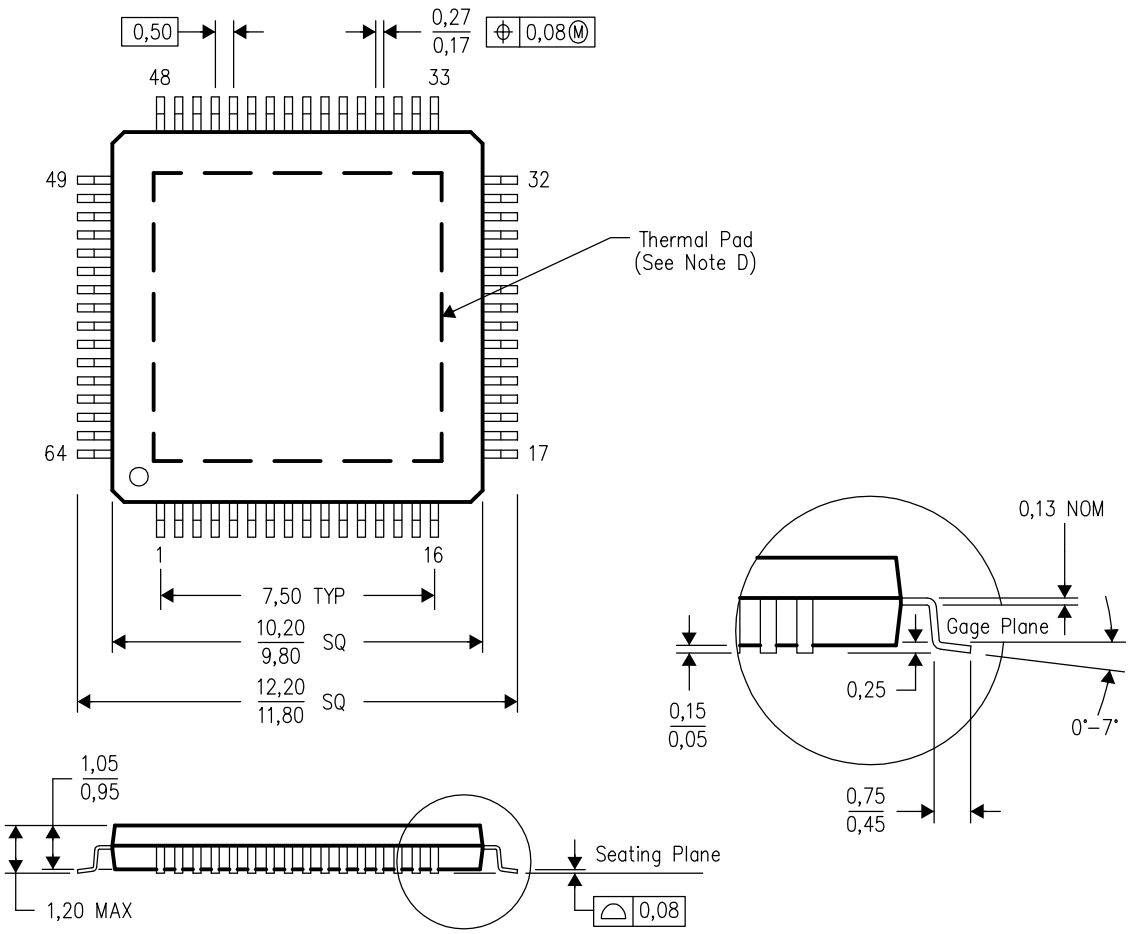
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB8041IPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

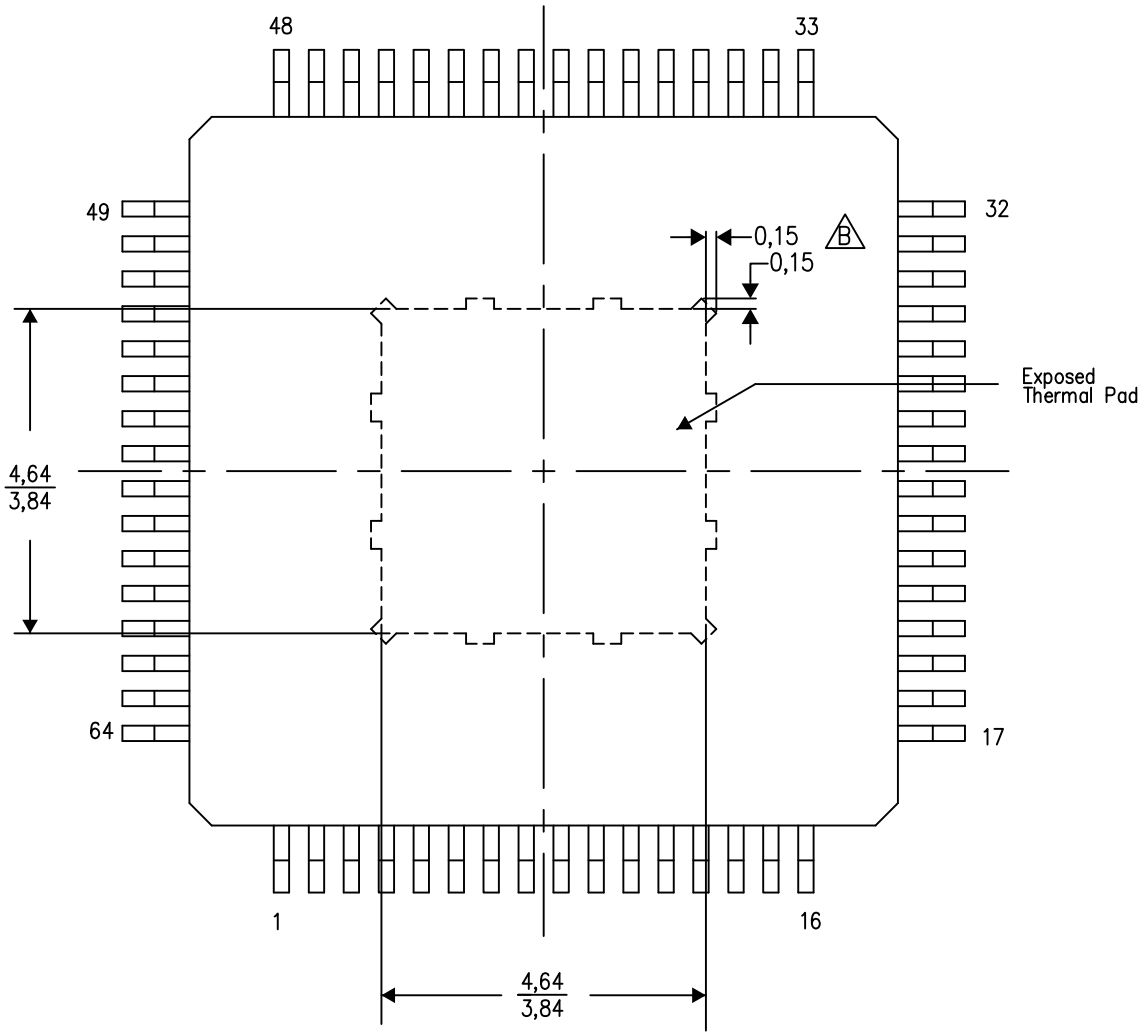
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–14/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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