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Advanced Information

Proximity Capacitive Touch Sensor Controller

MPR121

Capacitive Touch Sensor Controller

Bottom View

20-PIN QFN CASE 2059-01

Top View

Pin Connections

MPR121 OVERVIEW

The MPR121 is the second generation capacitive touch sensor controller after the initial release of the MPR03x series devices. The MPR121 features increased internal intelligence, some of the major additions include an increased electrode count, a hardware configurable I^2C address, an expanded filtering system with debounce, and completely independent electrodes with auto-configuration built in. The device also features a 13th simulated sensing channel dedicated for near proximity detection using the multiplexed sensing inputs.

Features
- Low power operation
  - 1.71 V to 3.6 V supply operation
  - 29 µA supply current at 16 ms sampling interval period
  - 3 µA Stop mode current
- 12 capacitance sensing inputs
  - 8 inputs are multifunctional for LED driver and GPIO
- Complete touch detection
  - Auto-configuration for each sensing input
  - Auto-calibration for each sensing input
  - Touch/release threshold and debounce for touch detection
- I^2C interface, with Interrupt output
- 3 mm x 3 mm x 0.65 mm 20 lead QFN package
- -40°C to +85°C operating temperature range

Implementations
- General Purpose Capacitive Detection
- Switch Replacements
- Touch Buttons
- Touch Keypad
- Touch Slide bar
- Touch Wheel
- Touchpad
- Touch Panel
- Near Proximity Detection

Typical Applications
- PC Peripherals
- MP3 Players
- Remote Controls
- Mobile Phones
- Lighting Controls
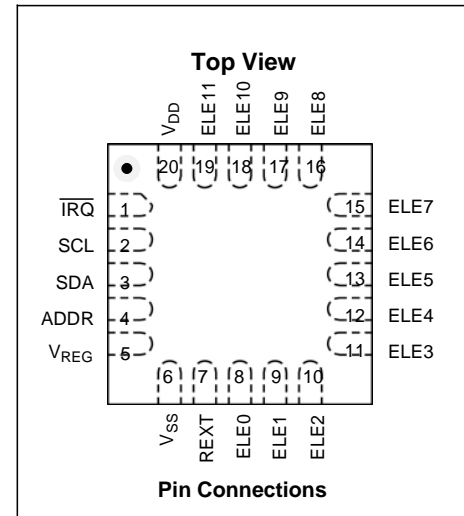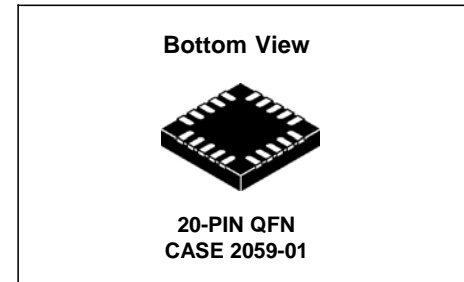
ORDERING INFORMATION

Device Name	Temperature Range	Case Number	Touch Pads	I^2C Address	Shipping
MPR121QR2	-40°C to +85°C	2059 (20-Pin QFN)	12-pads	0x5A - 0x5D	Tape & Reel

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PIN DESCRIPTION

Pin No.	Pin Name	Description
1	IRQ	Active Low Open-drain Interrupt Output
2	SCL	I^{2}C Serial Clock
3	SDA	I^{2}C Serial Data
4	ADDR	I²C Slave Address Pin Selects. Connect to VSS, VDD, SDA, SCL to choose address 0x5A, 0x5B, 0x5C, 0x5D respectively.
5	VREG	Internal Supply Voltage. Internal regulator output. Bypass to VSS with a 0.1 µF capacitor. Connect to VDD when supply below 2.75V
6	VSS	Ground
7	REXT	Reference Resistor Connection. Connect a 75k±1% resistor from REXT to VSS
8	ELE0	Electrode 0 Connection
9	ELE1	Electrode 1 Connection
10	ELE2	Electrode 2 Connection
11	ELE3	Electrode 3 Connection
12	ELE4/LED0	Electrode 4, or LED0, or GPIO4 Connection
13	ELE5/LED1	Electrode 5, or LED1, or GPIO5 Connection
14	ELE6/LED2	Electrode 6, or LED2, or GPIO6 Connection
15	ELE7/LED3	Electrode 7, or LED3, or GPIO7 Connection
16	ELE8/LED4	Electrode 8, or LED4, or GPIO8 Connection
17	ELE9/LED5	Electrode 9, or LED5, or GPIO9 Connection
18	ELE10/LED6	Electrode 10, or LED6, or GPIO10 Connection
19	ELE11/LED7	Electrode 11, or LED7, or GPIO11 Connection
20	VDD	Power Supply Input. Bypass to VSS by a 0.1 µF capacitor.

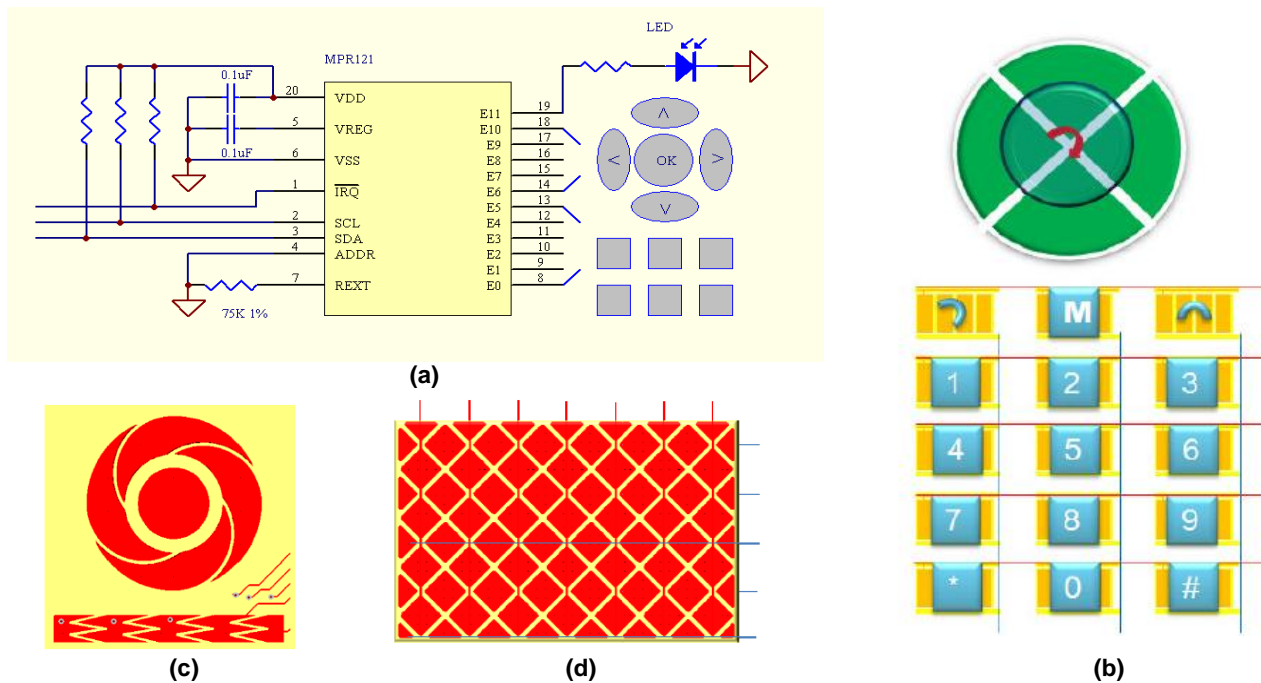## TYPICAL APPLICATION EXAMPLE AND ELECTRODE PATTERN

Figure 1. (a) Typical application circuit
(b) Button matrix pattern using 12 channels for 20 touch buttons
(c) Slide wheel and slide bar pattern using 10 channels
(d) Touchpad 5x7 pattern using 12 channels

DEVICE OPERATION OVERVIEW

Power Supply

MPR121 has two supply pins VDD and VREG. Power supply should always be connected to the VDD pin, which should be decoupled with a 0.1uF ceramic decoupling capacitor from VDD to VSS. The VDD should be clean without excessive noise, for example, noise ripple big than 100mV may result false function in some case.

To operate from a supply voltage in the range 2.0V to 3.6V, apply the voltage to VDD and internal voltage regulator will regulate a lower operating voltage on VREG. Connect a 0.1uF ceramic decoupling capacitor between VREG and VSS, but otherwise do not load VREG.

When power supply voltage is in the range 1.71V to 2.75V, the supply can also be routed into VREG directly to bypass internal voltage regulator. Bypass VDD and VREG together with a 0.1uF ceramic decoupling capacitor from VDD to VSS. Refer to Figure 2.

Note: The **absolute maximum rating** for VREG pin is 2.75V, the voltage applied should be carefully below this limit. The VDD pin should be always connected with VREG in this case.
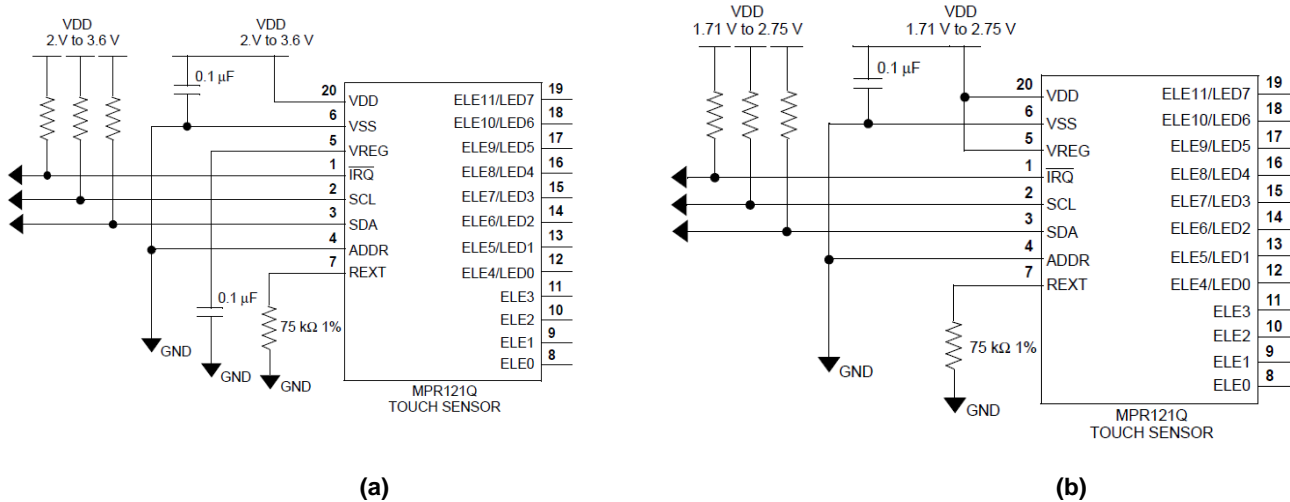

(a)   **(b)**

Figure 2. Typical MPR121 power supply connection.
(a) MPR121 runs from a 2.0 V to 3.6 V supply.
(b) MPR121 runs from a 1.71 V to 2.75 V supply.

Serial Communication

The MPR121 is an Inter-Integrated Circuit (I^2C) compliant device with an additional interrupt that is triggered any time a touch or release of a button is detected. The device has a configurable I^2C address by connecting the ADDR pin to the VSS, VDD, SDA or SCL lines, the resulting I^2C addresses are 0x5A, 0x5B, 0x5C and 0x5D respectively. The specific details of this system are described at the end of this document.

LED Driver and GIPO Function

Among the 12 sensing input pins, 8 pins are multifunctional pins capable for LED driver and GPIO functions. When these sensing input pins are not configured as electrodes inputs, they may be used to drive LEDs or for GPIO functions. When used for LED driver, connect these electrodes output to LED anodes and a series current limiting resistor to ground. The configuration of the LED driver and GPIO system is described in application note AN3894.

Capacitance Measurement and Touch Sensing

1. Capacitance Measurement

The complete capacitance measurement system is composed by sensing electrode pads connected to the MPR121 sensing inputs, and the MPR121 communicating with the host processor via the I^{2}C bus and Interrupt output. The total measureable sensing channels is 13 channels, including 12 physical electrode inputs and one multiplexed 13th channel for proximity detection. A multiplexer is included internally at the front end, so the 13 channels are measured sequentially in time. After the capacitance is measured, it then get noise filtered and finally touch /release status is determined.

Apart from touch sensing, MPR121 can also be used for general purpose capacitive detection in various industry applications. The 10bit output data (or even the 8bit baseline value providing an even higher level of noise rejection for slowly changing mediums) can be used as the capacitance measurement output relating to the measured parameters such as the water level, displacement, or medium content change.
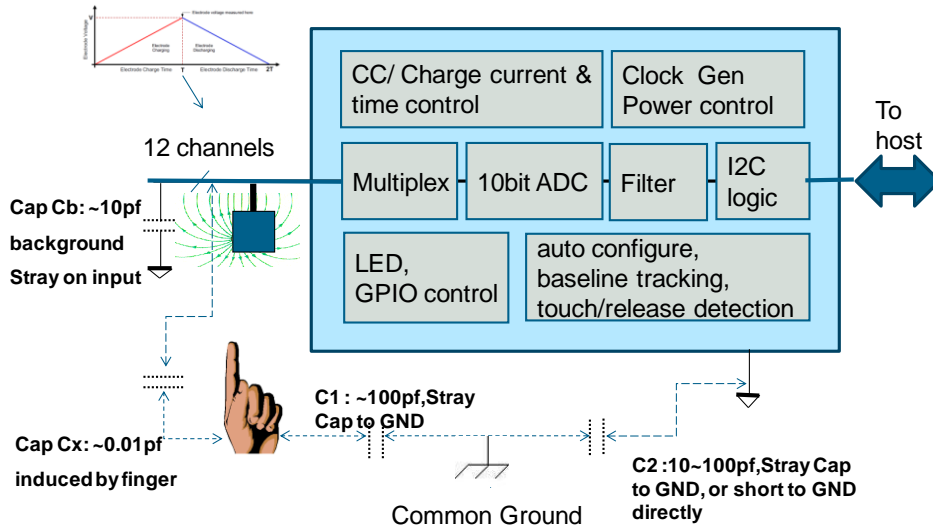

Figure 3. MPR121 Block Diagram and Capacitance Measurement

The capacitance measured on each sensing channel, is the total capacitance to ground which can be the combination of background parasitic capacitance to ground (Cb) and finger touch induced capacitance to ground (Cx). This ground refers to the common ground when the device is not electrically floated, and refers to the MPR121 device ground when the device is floated for example powered by batteries. For a typical application, for example the Cb can be about 10pF, and the Cx can be below 1pF. The two values can be much smaller in battery powered portable application, which requires more attention on touch sensitivity design.

The MPR121 uses a constant DC charge current scheme for capacitance measurement. Each channel is charged and then discharged completely to ground periodically to measure the capacitance (see Figure 4). All the channels are measured sequentially, when one channel is in the charge/discharge and measurement period the other channels are shorted to ground.
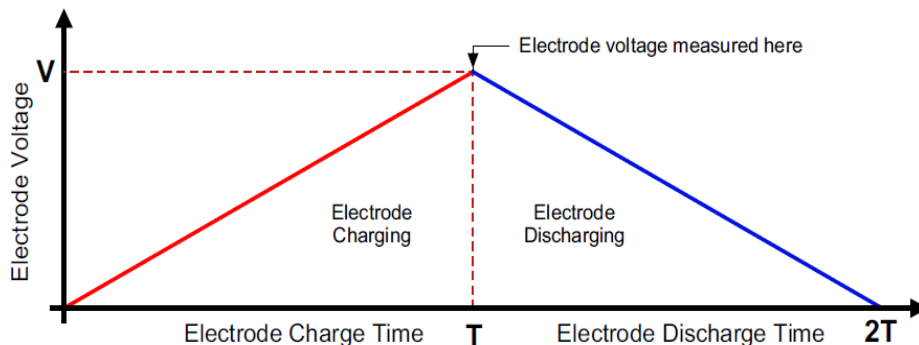

Figure 4. MPR121 Capacitance Measurement

The amount of charge (**Q**) applied is programmable by setting the charge current (**I**), and the charge time (**T**). Once the electrode is charged, the peak voltage (**V**) at the end of charge is measured by internal 10bit ADC. This voltage V (that is the ADC counts) is reverse proportional to the capacitance (**C**) on the sensing channel.

$$C = \frac{Q}{V} = \frac{I \times T}{V}, \qquad V = \frac{Q}{C} = \frac{I \times T}{C}$$

The programmable range for the current **I** is 1uA~63uA, see description on **AFE Configuration 1 Register (0x5C)**. The programmable range for time **T** is 0.5uS~32uS, see description on **AFE Configuration 2 Register (0x5D)**. To maintain the linearity of internal current source, the voltage on the sensing input suggested range is 0.7V ~ VDD-0.7V. Using these setting limits for the above equation, the **C** measurable range can be calculated.

Taking VDD=1.8V as an example:

$$Clow = \frac{Imin \times Tmin}{Vmax} = \frac{0.5uS \times 1uA}{1.8V - 0.7V} = 0.45pF$$

$$Chigh = \frac{Imax \times Tmax}{Vmin} = \frac{32uS \times 63uA}{0.7V} = 2880pF$$
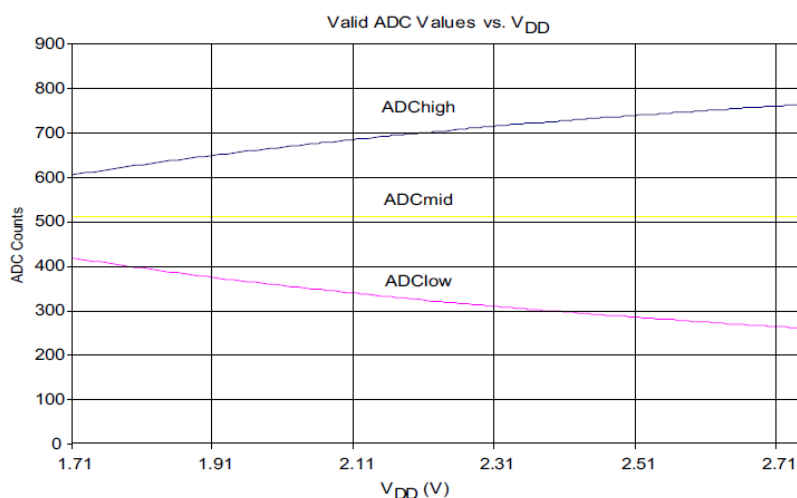

Figure 5. MPR121 linear voltage range by the supply voltage

Note: If the exact C value is not cared and MPR121 is only used for touch detection, then the current source linearity is not an issue and sensitivity is critical, the electrode can be charged up to the supply limit so maximum charge can be generated for higher touch detection sensitivity. However, charge should not be so high that the voltage is clipped by supply rail which can cause a reverse impact on sensitivity.

Since the ADC is 10bit, the equation for ADC reading result is as below:

$$ADC\ counts = \frac{V}{Vdd} \times 1024 = \frac{I \times T}{C} \times \frac{1}{Vdd} \times 1024$$

Re-arrange above equation, the capacitance **C** can be calculated as below:

$$C = \frac{I \times T}{ADC\ counts} \times \frac{1}{Vdd} \times 1024$$

To calculate the capacitance resolution per ADC counts,

$$\frac{dC}{dADC\ counts} = \frac{I \times T}{(ADC\ counts)^2} \times \frac{1}{Vdd} \times 1024 = \frac{C}{ADC\ counts}$$

From above equation, the resolution is dependent on the capacitance under measurement and the ADC reading counts. It's easy to understand smaller **C** or higher **ADC counts** result higher resolution.

To get the maximum resolution for a given **C**, the highest ADC counts is used, which gives out:

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$$\left(\frac{dC}{dADC\ counts}\right)_{min} = \frac{C}{(ADC\ counts)_{max}} = \frac{C}{1024} \approx 0.001C$$

For example, with **C**=10pF, when setting **I** and **T** so that the ADC reading counts is 1000, the sensing resolution for this capacitance at this reading counts will be 0.01pF. The conclusion is that to get the maximum sensing resolution, the capacitance shall be charged close to the upper counts limit. This scheme is used by the MPR121 in electrode auto-configuration where the optimized **I** and **T** are chosen to set the reading counts close to upper counts limit for the capacitance on the electrode.

For touch sensing application, to achieve the best sensing sensitivity, smaller C is desired, which means unnecessary stray capacitance on the channel inputs shall be kept as little as possible. The stray capacitance (**Cb**) can cause the sensing charge field return back to ground directly without following through **Cx** (See **Figure 3**) which is the capacitance change need to be detected. So ground layer and shield shall be carefully decided and designed so that both the EMC design consideration and the sensitivity target can be both achieved. Refer to MPR121 design guideline for more information on sensitivity issue.

2. Three levels of filtering

The ADC raw data outputs run through 3 levels of digital filtering to filter out the high frequency and low frequency noise encountered.

The first level filter is a simple running average filter configured by **FFI** (see description on **AFE Configuration 1 Register (0x5C)**) which is the number of samples used for the filter.

The 2nd level filter result is 10bit and stored in the output data registers 0x04~0x1D as the immediate capacitance of each sensing input (see description on **Filtered Data Registers**). The filter control parameter is **SFI** and **ESI** (see description on **AFE Configuration 2 Register (0x5D)**).

The 3rd level filter result is an even lower frequency content of signal change using the 2nd level filter output, and is mainly used as the baseline value representing the capacitance variation over the long term and slow environment change such as atmospheric moisture and dirt for touch detection. There are two sets of filter control parameters, all the 12 electrodes' baseline share the same set of parameters, while the 13th channel ELEPROX is controlled by another independent set of parameters (refer to description on **Baseline Filter Control Registers**).

The 3rd level filtered result is internally 10bit but only high 8 bits are readable from registers 0x1E~0x2A as the baseline value output for each channel (see description on **Baseline Value Registers**).
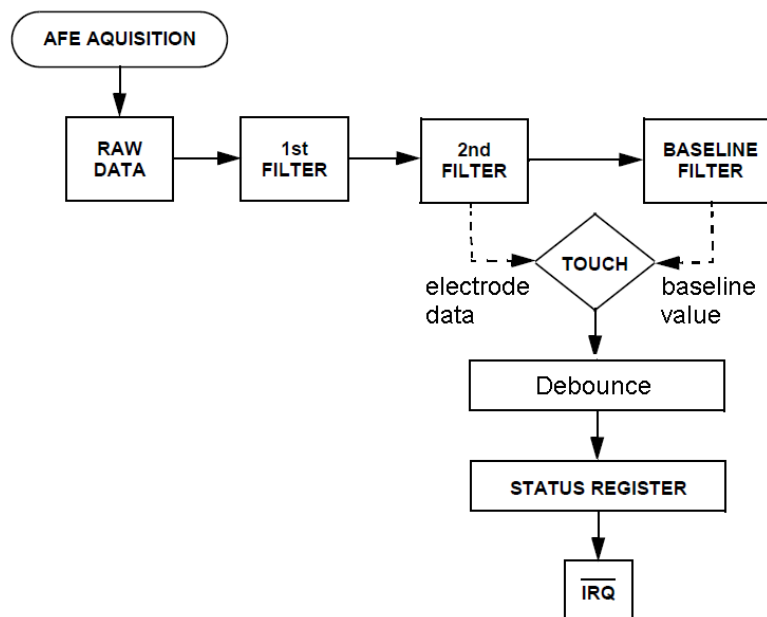

Figure 4. MPR121 Capacitance Measurement

3. Electrode Auto-Configuration

Given by a user defined target charge level, MPR121 can automatically run to get an optimized setting of charge current and charge time for each electrode without knowing the specific capacitance value on the electrode input. This smart auto-configuration feature greatly reduces the trial and fine tune time during the real system development period. The independent control and setting for each electrode allow for a great deal of flexibility in electrode pattern design. For information on how to use the auto-configuration function refer to application note AN3889.

4. Environment Auto-Calibration

MPR121 incorporates auto-calibration function which continually learns the background baseline capacitance of each individual electrode, so the system only has to program the amount of small change from these baselines that represents a touch or release. The 3rd level filtered result is used as the baseline value representing the capacitance variation of each electrode over the long term and slow environment change such as atmospheric moisture and dirt. For information on how to set up the background baseline tracking system refer to application note AN3891 and AN3892.

5. Touch and Release Detection

Touch and release is determined by comparing the immediate capacitance deviation that is the electrode 2nd level filtered output data deviation to the baseline value. If the deviation passed the setting threshold, then a touch or release status is detected and reported in the status register. The touch threshold and release threshold are independent and individually programmable for each electrode, providing hysteresis and electrode independence. Debounce setting can be used for further noise filtering to provide glitch free touch and release detection.
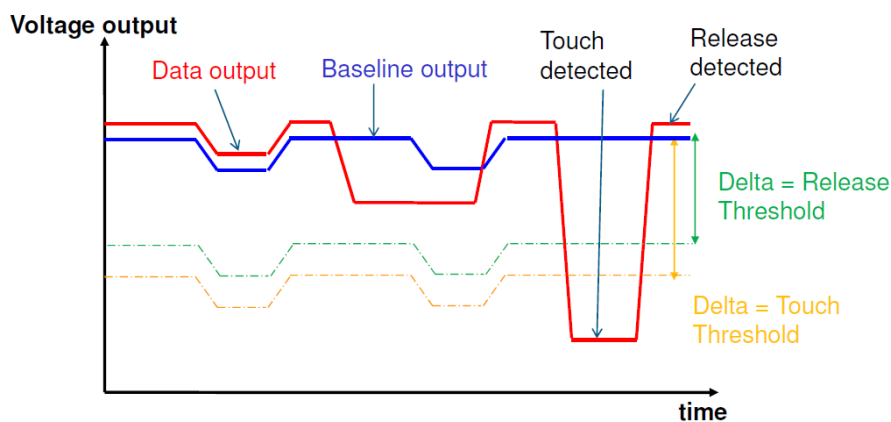

Figure 5. MPR121 Touch and Release Detection

6. Proximity Sensing

MPR121 can be used for near proximity sensing. By internally multiplexing all the sensing inputs so that they are connected together and all separated touch pads are "combined together" to create a single large electrode covering a larger sensing area. When enabled, this "13th" proximity detection channel will be included at the beginning of a normal electrode detection cycle. This 13th proximity detection has its own independent set of configuration registers. This system is described in application note AN3893.

Run Mode and Stop Mode

After completing **power on reset (POR)**, MPR121 is default in Stop Mode without any capacitance measurement. MPR121 can be set into Run Mode when bit D5~D0 in **Electrode Configuration Register (ECR, address 0x5E)** are not all zeros which indicates at least one of the 13 measurement channels is enabled. MPR121 can be set into Stop Mode by writing 2bXX000000 to ECR register.

In Run Mode, MPR121 uses a state machine which wakes up periodically to measure the electrodes, filter and analyze the data, and determine whether a touch pad has been touched or released. During the waiting period between measurements MPR121 draws negligible current, so the average current consumption is determined by the frequency and quantity of measurements channels enabled. MPR121 can be configured for a sampling interval between 1ms and 128ms. The user can make the tradeoff between noise rejection, touch response time, and power consumption. Refer to application note AN3890 on how to set up these configurations.

REGISTER DESCRIPTION

Table 1. Register Map

REGISTER	Fields								Register Address	Initial Value	Auto Increment Address
ELE0 - ELE7 Touch Status	E7TS	E6TS	E5TS	E4TS	E3TS	E2TS	E1TS	E0TS	0x00	0x00	
ELE8 - ELE11, ELEPROX Touch Status	OVCF			E12TS	E11TS	E10TS	E9TS	E8TS	0x01	0x00	
ELE0 - ELE7 OOR Status	E7OOR	E6OOR	E5OOR	E4OOR	E3OOR	E2OOR	E1OOR	E0OOR	0x02	0x00	
ELE8 - ELE11, ELEPROX OOR Status	ARFF	ACFF		E12OOR	E11OOR	E10OOR	E9OOR	E8OOR	0x03	0x00	
ELE0 Electrode Filtered Data LSB	E0FDL								0x04	0x00	
ELE0 Electrode Filtered Data MSB							E0FDH		0x05	0x00	
ELE1 Electrode Filtered Data LSB	E1FDL								0x06	0x00	
ELE1 Electrode Filtered Data MSB							E1FDH		0x07	0x00	
ELE2 Electrode Filtered Data LSB	E2FDL								0x08	0x00	
ELE2 Electrode Filtered Data MSB							E2FDH		0x09	0x00	
ELE3 Electrode Filtered Data LSB	E3FDL								0x0A	0x00	
ELE3 Electrode Filtered Data MSB							E3FDH		0x0B	0x00	
ELE4 Electrode Filtered Data LSB	E4FDL								0x0C	0x00	
ELE4 Electrode Filtered Data MSB							E4FDH		0x0D	0x00	
ELE5 Electrode Filtered Data LSB	E5FDL								0x0E	0x00	
ELE5 Electrode Filtered Data MSB							E5FDH		0x0F	0x00	
ELE6 Electrode Filtered Data LSB	E6FDL								0x10	0x00	
ELE6 Electrode Filtered Data MSB							E6FDH		0x11	0x00	
ELE7 Electrode Filtered Data LSB	E7FDL								0x12	0x00	
ELE7 Electrode Filtered Data MSB							E7FDH		0x13	0x00	
ELE8 Electrode Filtered Data LSB	E8FDL								0x14	0x00	
ELE8 Electrode Filtered Data MSB							E8FDH		0x15	0x00	
ELE9 Electrode Filtered Data LSB	E9FDL								0x16	0x00	
ELE9 Electrode Filtered Data MSB							E9FDH		0x17	0x00	Register Address + 1
ELE10 Electrode Filtered Data LSB	E10FDL								0x18	0x00	
ELE10 Electrode Filtered Data MSB							E10FDH		0x19	0x00	
ELE11 Electrode Filtered Data LSB	E11FDL								0x1A	0x00	
ELE11 Electrode Filtered Data MSB							E11FDH		0x1B	0x00	
ELEPROX Electrode Filtered Data LSB	E12FDL								0x1C	0x00	
ELEPROX Electrode Filtered Data MSB							E12FDH		0x1D	0x00	
ELE0 Baseline Value	E0BV								0x1E	0x00	
ELE1 Baseline Value	E1BV								0x1F	0x00	
ELE2 Baseline Value	E2BV								0x20	0x00	
ELE3 Baseline Value	E3BV								0x21	0x00	
ELE4 Baseline Value	E4BV								0x22	0x00	
ELE5 Baseline Value	E5BV								0x23	0x00	
ELE6 Baseline Value	E6BV								0x24	0x00	
ELE7 Baseline Value	E7BV								0x25	0x00	
ELE8 Baseline Value	E8BV								0x26	0x00	
ELE9 Baseline Value	E9BV								0x27	0x00	
ELE10 Baseline Value	E10BV								0x28	0x00	
ELE11 Baseline Value	E11BV								0x29	0x00	
ELEPROX Baseline Value	E12BV								0x2A	0x00	
MHD Rising			MHDR						0x2B	0x00	
NHD Rising			NHDR						0x2C	0x00	
NCL Rising	NCLR								0x2D	0x00	
FDL Rising	FDLR								0x2E	0x00	
MHD Falling			MHDF						0x2F	0x00	
NHD Falling			NHDF						0x30	0x00	

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Table 1. Register Map

REGISTER	Fields					Register Address	Initial Value	Auto Increment Address
NCL Falling	NCLF					0x31	0x00	
FDL Falling	FDLF					0x32	0x00	
NHD Touched			NHDT			0x33	0x00	
NCL Touched	NCLT					0x34	0x00	
FDL Touched	FDLT					0x35	0x00	
ELEPROX MHD Rising			MHDPROXR			0x36	0x00	
ELEPROX NHD Rising			NHDPROXR			0x37	0x00	
ELEPROX NCL Rising	NCLPROXR					0x38	0x00	
ELEPROX FDL Rising	FDLPROXR					0x39	0x00	
ELEPROX MHD Falling			MHDPROXF			0x3A	0x00	
ELEPROX NHD Falling			NHDPROXF			0x3B	0x00	
ELEPROX NCL Falling	NCLPROXF					0x3C	0x00	
ELEPROX FDL Falling	FDLPROXF					0x3D	0x00	
ELEPROX NHD Touched			NHDPROXT			0x3E	0x00	
ELEPROX NCL Touched	NCLPROXT					0x3F	0x00	
ELEPROX FDL Touched	FDLPROXT					0x40	0x00	
ELE0 Touch Threshold	E0TTH					0x41	0x00	
ELE0 Release Threshold	E0RTH					0x42	0x00	
ELE1 Touch Threshold	E1TTH					0x43	0x00	
ELE1 Release Threshold	E1RTH					0x44	0x00	
ELE2 Touch Threshold	E2TTH					0x45	0x00	
ELE2 Release Threshold	E2RTH					0x46	0x00	
ELE3 Touch Threshold	E3TTH					0x47	0x00	
ELE3 Release Threshold	E3RTH					0x48	0x00	
ELE4 Touch Threshold	E4TTH					0x49	0x00	Register Address + 1
ELE4 Release Threshold	E4RTH					0x4A	0x00	
ELE5 Touch Threshold	E5TTH					0x4B	0x00	
ELE5 Release Threshold	E5RTH					0x4C	0x00	
ELE6 Touch Threshold	E6TTH					0x4D	0x00	
ELE6 Release Threshold	E6RTH					0x4E	0x00	
ELE7 Touch Threshold	E7TTH					0x4F	0x00	
ELE7 Release Threshold	E7RTH					0x50	0x00	
ELE8 Touch Threshold	E8TTH					0x51	0x00	
ELE8 Release Threshold	E8RTH					0x52	0x00	
ELE9 Touch Threshold	E9TTH					0x53	0x00	
ELE9 Release Threshold	E9RTH					0x54	0x00	
ELE10 Touch Threshold	E10TTH					0x55	0x00	
ELE10 Release Threshold	E10RTH					0x56	0x00	
ELE11 Touch Threshold	E11TTH					0x57	0x00	
ELE11 Release Threshold	E11RTH					0x58	0x00	
ELEPROX Touch Threshold	E12TTH					0x59	0x00	
ELEPROX Release Threshold	E12RTH					0x5A	0x00	
Debounce Touch & Release		DR			DT	0x5B	0x00	
AFE Configuration 1	FFI		CDC			0x5C	0x10	
AFE Configuration 2	CDT		SFI		ESI	0x5D	0x24	
Electrode Configuration(ECR)	CL		ELEPROX		ELE	0x5E	0x00	
ELE0 Electrode Current			CDC0			0x5F	0x00	
ELE1 Electrode Current			CDC1			0x60	0x00	
ELE2 Electrode Current			CDC2			0x61	0x00	

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Table 1. Register Map

REGISTER	Fields						Register Address	Initial Value	Auto Increment Address
ELE3 Electrode Current			CDC3				0x62	0x00	
ELE4 Electrode Current			CDC4				0x63	0x00	
ELE5 Electrode Current			CDC5				0x64	0x00	
ELE6 Electrode Current			CDC6				0x65	0x00	
ELE7 Electrode Current			CDC7				0x66	0x00	
ELE8 Electrode Current			CDC8				0x67	0x00	
ELE9 Electrode Current			CDC9				0x68	0x00	
ELE10 Electrode Current			CDC10				0x69	0x00	
ELE11 Electrode Current			CDC11				0x6A	0x00	
ELEPROX Electrode Current			CDC12				0x6B	0x00	
ELE0, ELE1 Charge Time		CDT1			CDT0		0x6C	0x00	
ELE2, ELE3 Charge Time		CDT3			CDT2		0x6D	0x00	
ELE4, ELE5 Charge Time		CDT5			CDT4		0x6E	0x00	
ELE6, ELE7 Charge Time		CDT7			CDT6		0x6F	0x00	
ELE8, ELE9 Charge Time		CDT9			CDT8		0x70	0x00	Register Address + 1
ELE10, ELE11 Charge Time		CDT11			CDT10		0x71	0x00	
ELEPROX Charge Time					CDT12		0x72	0x00	
GPIO Control Register 0	CTL0						0x73	0x00	
GPIO Control Register 1	CTL1						0x74	0x00	
GPIO Data Register	DAT						0x75	0x00	
GPIO Direction Control Register	DIR						0x76	0x00	
GPIO Enable Register	EN						0x77	0x00	
GPIO Data Set Register	SET						0x78	0x00	
GPIO Data Clear Register	CLR						0x79	0x00	
GPIO Data Toggle Register	TOG						0x7A	0x00	
AUTO-CONFIG Control Register 0	AFES	RETRY		BVA	ARE	ACE	0x7B	0x00	
AUTO-CONFIG Control Register 1	SCTS				OORIE	ARFIE	ACFIE	0x7C	0x00	
AUTO-CONFIG USL Register	USL						0x7D	0x00	
AUTO-CONFIG LSL Register	LSL						0x7E	0x00	
AUTO-CONFIG Target Level Register	TL						0x7F	0x00	0x00
Soft Reset Register	SRST						0x80	0x00	-
Factory Reserved Region(0x81~0xFF)	-						-	-	-

Register Operation

1. General Rules

Note: After completing **power on reset (POR)** or soft reset by command, MPR121 all registers are in default reset initial value (see Table 1). All the registers are cleared, except AFE Configuration Registers 0x5C (Default 0x10) and 0x5D (Default 0x24).

MPR121 reset default mode is Stop Mode without any capacitance measurement. Set MPR121 into Run Mode by configuring **ECR register (0x5E)** so that least one of the 13 measurement channels is enabled. Set MPR121 into Stop Mode by writing 2bXX000000 to ECR register at any time. For all the registers, the current value can be read at any time.

Note: Registers write operation can only be done after MPR121 is set into Stop Mode, except the ECR and GPIO/LED related registers, which means changing the value of these registers while MPR121 is in Run Mode will not be effective.

Registers from address 0x00 to 0x2A are the output registers which are updated periodically when MPR121 is in Run Mode. While Baseline Value Registers 0x1D to 0x2A are the internal output baseline registers, these registers are also writeable to user, this is useful if customer setting targets as the initial baseline tracking start points is desired.

Registers from address 0x2B to 0x7F are control and configuration registers, which need to be correctly configured and initialized to start the capacitance measurement and touch detection.

2. Touch Status Registers (0x00~0x01)

ELE0 - ELE7 Touch Status (0x00)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	E7TS	E6TS	E5TS	E4TS	E3TS	E2TS	E1TS	E0TS
Write								

ELE8 – ELE12 Touch Status (0x01)

Read	OVCF	0	0	E12TS	E11TS	E10TS	E9TS	E8TS
Write	1							

These two registers indicate touch/release status of each electrode. ELE12 is the status for the "13th" **Electrode Proximity Detection (ELEPROX)**. The update rate of these status bits will be {ESI x SFI}.

ExTS: Touch or Release status bit of each respective channel (Read only).
> 1, the respective channel is currently deemed as touch.
> 0, the electrode is deemed as release.

Note: When a GPIO is enabled as input port and the pin is not configured as an electrode, the corresponding status bit shows the input level. This feature is for ELE4~ELE11 only. These GPIO status change will not cause any IRQ interrupt.

OVCF: Over Current Flag (Read and Write)
> 1, over current was detected on REXT pin.
> 0, normal condition

When over current detected, the OVCF is set and MPR121 goes to Stop Mode immediately. The ExTS bits in status registers, output registers 0x04~0x2A, and bit D5~D0 in ECR will be also cleared on over current condition. When the bit is "1", writing ECR register to enter Run mode will be discarded.

Write "1" to OVCF will clear this bit and MPR121 fault condition is cleared so that MPR121 can be configured into Run Mode again.

3. Electrode Data Register (0x04~0x1D)

Electrode Data Low Byte ExFDL and High Byte ExFDH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	ExFD7	ExFD6	ExFD5	ExFD4	ExFD3	ExFD2	ExFD1	ExFD0
Write								

Read	0	0	0	0	0	0	ExFD9	ExFD8
Write								

ExFDL, ExFDH: Each of the 13 channels has a low byte and a high byte registers to store a 10bit output electrode data, which is the 2nd level filter filtered data output. The data range is 0~1024 or 0x000~0x400 in Hex. Low byte ExFDL holds the lower 8 bits D0~D7, and high byte ExFDH holds the higher 2 bits D8 and D9.

These registers are read only and updated every {ESI x SFI}. A multi byte read operation to read both LSB and MSB is required to keep the data coherency (LSB and MSB matching).

A multi byte reading of 0x00 thru 0x2A returns results of a single moment (never mixed-up old and new).

4. Baseline Value Register (0x1E~0x2A)

Electrode Baseline Value

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	ExBV9	ExBV8	ExBV7	ExBV6	ExBV5	ExBV4	ExBV3	ExBV2
Write								

ExBV: The 3rd level filter is used as the baseline filter for touch detection with an output of a 10bit baseline vale. Baseline Value Register holds the high 8 bits of the internal 10bit baseline value for each of the 13 channels.

CL bits from ECR register (0x5E) specify the update operation of these registers. The update rate of these registers is {ESI x SFI}.

User can write it in Stop Mode and the write operation will clear lower 2 bits of the internal 10bits value.

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5. Baseline Filtering Control Register (0x2B~0x40)

Background baseline value tracking is operated by the internal 3rd level filter controlled by registers 0x2B to 0x40. All the 12 electrodes' baseline are controlled by the same set of registers 0x2B to 0x35, while the 13th channel ELEPROX is controlled by another independent set of registers 0x36 to 0x40.

Both above two sets have the same structure using 3 different scenarios called rising, falling, and touched. The rising situation is defined when electrode data > baseline value, the falling is defined when electrode data < baseline value, and the touched is when the electrode is in touched status.

For each scenario, the filtering characteristic is further defined by 4 parameters: the maximum half delta, noise half delta, noise count limit and filter delay count limit. There is no maximum half delta for touched scenario.

Maximum Half Delta (MHD): Determines the largest magnitude of variation to pass through the baseline filter. The range of the effective value is 1~63.

Noise Half Delta (NHD): Determines the incremental change when non-noise drift is detected. The range of the effective value is 1~63.

Noise Count Limit (NCL): Determines the number of samples consecutively greater than the Max Half Delta necessary before it can be determined that it is non-noise. The range of the effective value is 0~255.

Filter Delay Count Limit (FDL): Determines the rate of operation of the filter. A larger number makes it operate slower. The range of the effective value is 0~255.

The setting of the filter is depended on the actual application. For the details on how to set these registers, refer to application note AN3891.

6. Touch and Release Threshold (0x41~0x5A)

Touch Threshold ExTTH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read								
Write					ExTTH			

Release Threshold ExRTH

Read								
Write					ExRTH			

ExTTH, ExRTH: Each of the 13 channels has its own set of touch threshold and release threshold registers. The threshold is defined as a deviation value from the baseline value, so it remains constant even baseline value changes. Typically the touch threshold is a little bigger than the release threshold to touch debounce and hysteresis.

The range of the value is 0~255. For typical touch application, the value can be in range 0x05~0x30 for example. The setting of the threshold is depended on the actual application. For the operation details and how to set the threshold refer to application note AN3892 and MPR121 design guidelines.

7. Debounce Register (0x5B)

Touch and Release Debounce

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	0		DR		0		DT	
Write			DR				DT	

The register holds debounce setting affecting the final touch and release status change in 0x00 and 0x01. The status change will only take place after the number of consecutive touch or release detection meets the debounce number. If the number detected does not meet the debounce number, the status will not change.

DT: Debounce number for touch. The value range is 0~7.
DR: Debounce number for release. The value range is 0~7.

When an electrode data deems consecutive touch with the debounce number, the status becomes "touch". When an electrode data deems consecutive release with the debounce number, the status becomes "release". The status appears on Status Register with a delay of {ESI x SFI x DR (or DT)}.

8. AFE Configuration Register (0x5C, 0x5D)

AFE Configuration 1 Register (0x5C), default =0x10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	FFI		CDC					
Write								

This register holds the first level filter configuration, and the charge current global setting for all 13 channels. For each channel the global CDC will be used if the individual charge discharge current CDCx is zero. If there is none zero data in 0x5F~0x6B, then this individual CDCx value will be used for that respective channel instead of the global CDC value.

Field	Description
7:6 **FFI**	First Filter Iterations – The first filter iterations field selects the number of samples taken as input to the first level of filtering. 00 Encoding 0 – Sets samples taken to 6 (Default) 01 Encoding 1 – Sets samples taken to 10 10 Encoding 2 – Sets samples taken to 18 11 Encoding 3 – Sets samples taken to 34
5:0 **CDC**	Charge Discharge Current – The Charge Discharge Current field selects the supply current to be used when charging and discharging an electrode. Programmable in 1uA step. 000000 Encoding 0 – Disables Electrode Charging?? 000001 Encoding 1 – Sets the current to 1μA ~ 010000 Encoding 16 – Sets the current to 16μA (Default) ~ 111111 Encoding 63 – Sets the current to 63 μA

AFE Configuration 2 Register (0x5D), default =0x24

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	CDT			SFI		ESI		
Write								

This register holds global charge and discharge time setting, and the second level filter configuration. The CDT bits set the charge/discharge time global setting for all the 13 channels. For each channel the global CDT will be used if the individual charge discharge time CDTx is zero. If there is none zero data in 0x6C~0x72, then this individual CDTx value will be used for that respective channel instead of the global CDT value.

Field	Description
7:5 **CDT**	Charge Discharge Time – selects the amount of time an electrode charges. Programmable to $0.5 \, (2^{n-1})$ uS 000 Encoding 0 – Invalid 001 Encoding 1 – Time is set to 0.5 μs (Default) 010 Encoding 2 – Time is set to 1 μs ~ 111 Encoding 7 – Time is set to 32 μs
4:3 **SFI**	Second Filter Iterations – selects the number of samples taken for the second level filter. 00 Encoding 0 – Number of samples is set to 4 (Default) 01 Encoding 1 – Number of samples is set to 6 10 Encoding 2 – Number of samples is set to 10 11 Encoding 3 – Number of samples is set to 18
2:0 **ESI**	Electrode Sample Interval – selects the period between samples used for the second level of filtering. Programmable to 2^n ms. 000 Encoding 0 – Period set to 1 ms 001 Encoding 1 – Period set to 2 ms ~ 100 Encoding 4 – Period set to 16 ms (Default) ~ 111 Encoding 7 – Period set to 128 ms

9. Individual Charge Current Register (0x5F~0x6B)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	0		CDCx					
Write								

These registers hold the individual Charge/Discharge Current (CDCx) value for each channel if CDC global value is not used. The parameter setting is similar to the CDC. The power on reset default of these registers is all zeros.

Field	Description
5:0 CDCx	Individual Charge Discharge Current – The Individual Charge Discharge Current field selects the supply current to be used when charging and discharging a specific channel. Programmable in 1uA step. 000000 Encoding 0 – Global CDC is used if this channel is enabled (Default). 000001 Encoding 1 – Sets the current to 1µA, global CDC is not used ~ 010000 Encoding 16 – Sets the current to 16µA, global CDC is not used ~ 111111 Encoding 63 – Sets the current to 63µA, global CDC is not used

If the CDCx is zero, then the global value is used. If there is none zero data in 0x5F~0x6B, then the individual value will be used for this respective channel instead of the global CDC value.

If auto configuration is enabled and run once, the individual CDC will be automatically updated by MPR121 internally after auto configuration is finished.

10. Individual Charge Time Register (0x6C~0x72)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	CDTx'			0	CDTx		
Write								

These registers hold the individual Charge/Discharge Time (CDTx) value for each channel if CDT global value is not used. The parameter setting is similar to the CDT. The power on reset default of these registers is all zeros.

Field	Description
7:5 CDTx	Individual Charge Discharge Time – selects the amount of charge time for individual channels. Programmable to $0.5 (2^{n-1})$ uS 000 Encoding 0 – Global CDT is used if this channel is enabled (Default) 001 Encoding 1 – Time is set to 0.5µs, global CDT is not used 010 Encoding 2 – Time is set to 1µs, global CDT is not used ~ 111 Encoding 7 – Time is set to 32µs, global CDT is not used

If the CDTx is zero, then the global value is used. If there is none zero data in 0x6C~0x72, then the individual value will be used for this respective channel instead of the global CDT value.

If auto configuration and SCTS bit in Auto Configuration Register 1 (0x7B) are enabled and run once, the individual CDTx will be automatically updated by MPR121 internally after auto configuration is finished.

11. Electrode Configuration Register (ECR, 0x5E)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	CL[1:0]		ELEPROX[1:0]		ELE[3:0]			
Write								

This register selects measurement electrodes and proximity detection electrode configurations, and controls MPR121 in Run Mode or Stop Mode. MPR121 reset default is in Stop Mode without any capacitance measurement.

To start capacitance measurement and touch detection, set into Run Mode by selecting the sensing inputs to be enabled. MPR121 can be set into Stop Mode by writing 2bXX000000 to ECR at any time.

CL: Calibration Lock bit. The CL bits controls the Baseline Value Register update. Typically CL=2b10 is used so the baseline value can be initialized at the beginning stage with a value close to the immediate data instead of starting from zero. Since the 3rd level filter has a big time constant, starting from zero may cause a long time of no response with touch.

CL[1:0]	Description
00	Baseline tracking enable (Default). The baseline values updates every {ESI x SFI} period by MPR121 per baseline filter operation. The initial value is?????
01	Calibration lock. Baseline tracking disabled. Baseline values are unchanged by MPR121.
10	Baseline tracking and initialize enable. At the first {ESI x SFI}, MPR121 copy 5MSBs of the 2nd filter output to 10bit baseline value (5LSBs become zero). Subsequent update is per nominal baseline filter operation.
11	Baseline tracking and initialize enable. At the first {ESI x SFI}, MPR121 copy the 2nd filter output to 10bit baseline value. Subsequent update is per nominal baseline filter operation.

ELE[3:0]	Description
0000	Electrode touch detection disabled (Default)
0001	Run Mode with ELE0 measurement enabled.
0010	Run Mode with ELE0~1 measurement enabled.
0011	Run Mode with ELE0~2 measurement enabled.
0100	Run Mode with ELE0~3 measurement enabled.
0101	Run Mode with ELE0~4 measurement enabled.
0110	Run Mode with ELE0~5 measurement enabled.
0111	Run Mode with ELE0~6 measurement enabled.
1000	Run Mode with ELE0~7 measurement enabled.
1001	Run Mode with ELE0~8 measurement enabled.
1010	Run Mode with ELE0~9 measurement enabled.
1011	Run Mode with ELE0~10 measurement enabled.
11xx	Run Mode with ELE0~11 measurement enabled.

ELEPROX[1:0]	Description
00	Proximity detection disabled(Default)
01	Run Mode with ELE0~1 for proximity detection enabled.
10	Run Mode with ELE0~3 for proximity detection enabled.
11	Run Mode with ELE0~11for proximity detection enabled.

When both ELEPROX and ELE are none zero, proximity detection measures first then measures electrode(s). When both ELEPROX and ELE are cleared, MPR121 will be back to Stop Mode.

ELE: When ELECON ≠ 0, electrode touch detection with specific electrodes is enabled
ELEPROX: When ELEPROXCON≠ 0, proximity detection with specific electrodes combination is enabled

12. Auto Configuration Registers   (0x7B~0x7F)

In real application, the capacitance on each of the 13 channels can be various very differently depending on the electrode pattern, size, overlay and base material dielectric constant used for each channel. For example, the proximity channel ELEPROX may have a quite larger capacitance than the other individual electrode. The global CDC and CDT value may not fit all the channels in these cases that the charge is either not strong enough to detect weak capacitance change or too big that overflow the ADC detectable range.

To optimize the charge setting for each channel, the individual CDCx (I), CDTx (T) need to be properly set if the channel difference is large. There will be total 26 parameters need to be set if 13 channels are all used. This may consume a lot of time on trial and test with all possible combinations of different electrode pattern, size, overlay and base material dielectric constant, charge current value and charge time value used.

However, with auto-configuration, this task can be easily done by MPR121 automatically inside with binary search process on proper CDCx(I) and CDTx(T) combination so the charge level is as close to a target level as possible. Normally the target charge level (I x T) may be simply put at close to the input linear upper limit so the highest charge field can be produced to detect weak capacitance change. The upper limit and lower limit levels are also needed to provide the necessary searching boundaries. After auto configuration, the proper CDCx and CDTx for each channel are found and automatically filled.

The AUTO-CONFIG runs only once at first transition from Stop Mode to Run Mode. The AUTO-RECONFIG is supplements of AUTO-CONFIG. If electrode data goes out of valid range during normal measurement, AUTO-RECONFIG starts binary search for that electrode.

There are 5 registers in this group. Register 0x07D to 0x7F provided the configuration target settings. Registers 0x7B and 0x7C are the auto configuration control registers. Refer to application note AN3889 for details on how to set these registers.

Upper Side Limit Register (0x7D)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read					USL			
Write								

Lower Side Limit Register (0x7E)

Read					LSL			
Write								

Target Level Register (0x7F)

Read					TL			
Write								

Note similar to the baseline value, all the three parameters are in the 8bit format but internally treated as the 8MSB of 10bit data.

USL: Upper Side Limit. This value makes sure that the electrode data level is below the linear upper limit range VDD-0.7V. Typically the USL is set at the maximum linear limit.

$$USL = (VDD-0.7) / VDD \times 256$$

LSL: Lower Side Limit. This value results the lower limit for the electrode data. To make sure the touched electrode data still in the limit, the LSL should be low enough to prevent unnecessary out of range error. In a typical touch application, for example, the LSL can be set at 65% of the USL, that is

$$LSL = (VDD-0.7) / VDD \times 256 \times 0.65$$

TL: Target Level is the expected target electrode data level when untouched after auto configuration. MPR121 executes binary search on the proper setting of the charge current and/or charge time for each channel to hit the target level as close as possible. The TL shall be in between the Upper Side Limit (USL) and Lower Side Limit (LSL), and should be as high as possible to maximize the sensing charge field to get the maximum touch response.

Note the linear input range for ADC is limited from VDD-0.7 to 0.7V for each channel. To anticipate possible capacitance decrease range and VDD variation, for example, a typical setting for TL is 90% of the USL, that is

$$TL = USL \times 0.9 = (VDD-0.7) / VDD \times 256 \times 0.9$$

If a searching result is outside the range limited by USL and LSL, an Out Of Range (OOR) error will be reported at the end of auto configuration (refer to next section). Set the USL and TL as close to the linear upper input limit as possible will result the highest possible charge to detect weak capacitance change. **Note** in case where VDD is changing, the lowest VDD value shall be used to prevent OOR error.

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Auto Configuration Register 0 (0x7B)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	AFES		RETRY		BVA		ARE	ACE
Write								

ACE: 1: Enable AUTO-CONFIG, 0: Disable AUTO-CONFIG
ARE: 1: Enable AUTO-RECONFIG, 0: Disable AUTO-RECONFIG

BVA: Baseline Value Adjust Control specifies how to change baseline value for each channel upon finishing auto configuration and auto re-configuration.
      00: Baseline value is no change,
      01: Baseline value is cleared to zero,
      10: Baseline is set to the AUTO-CONFIG baseline value with 5MSBs loaded and the other lower bits cleared,
      11: Baseline is set to the AUTO-CONFIG baseline value

RETRY: MPR121 may retry AUTO-CONFIG or AUTO-RECONFIG after failed.
      00: no retry,
      01: 2 times,
      10: 4 times,
      11: 8 times.

AFES: This bit specifies AFE Samples during binary search. The AFES values should be as same as global AFES in ACR register, otherwise AUTO-CONFIG couldn't configure CDCx/CDTx correctly.
      00: 6 samples,
      01: 10 samples,
      10: 18 samples,
      11: 34 samples.

Auto Configuration Register 1 (0x7C)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	SCTS	0	0	0	0	OORIE	ARFIE	ACFIE
Write								

SCTS: 1: Skip Charge Time Search during binary search. User should specify charge time through global value CDT or individual value CDTx in respective registers. 0: Charge Time Search is executed during binary search.

ACFIE: 1: AUTO-CONFIG Fail Interrupt Enable, 0: AUTO-CONFIG Fail will not cause interrupt.
ARFIE: 1: AUTO-RECONFIG Fail Interrupt Enable, 0: AUTO-RECONFIG fail will not cause interrupt.
OORIE: 1: Out of Range Interrupt Enable, 0: Out of Range error will not cause Interrupt.

13. Out Of Range Status Registers (0x02, 0x03)

MPR121 checks electrode data after AUTO-CONFIG/AUTO-RECONFIG operation and also in normal measurement. When electrode data goes out of a range, corresponding OORx bits in the OOR0 and OOR1 Registers become "1" to indicate failed electrode. One possible example of triggering OOR error may be caused by shorting one of the measurement channels to ground. The valid range can be programmed through USL Register and LSL Register. Those bits are cleared when passed AUTO-CONFIG, AUTO-RECONFIG or range check. These two register is read only, user can't change the contents.

OUT OF RANGE Register 0 (0x02)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Read	OOR7	OOR6	OOR5	OOR4	OOR3	OOR2	OOR1	OOR0
Write								

OUT OF RANGE Register 1 (0x03)

Read	ACFF	ARFF	0	OOR12	OOR11	OOR10	OOR9	OOR8
Write								

OORx: 1: OOR error detected on respective channel, 0: No OOR error.

ACFF: AUTO-CONFIG Fail Flag. When AUTO-CONFIG failed, this bit set.
ARFF: AUTO-RECONFIG Fail Flag. When AUTO-RECONFIG failed this bit set.

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14. GPIO Registers (0x73~0x7A)

These registers control GPIO function. D7~D0 bits corresponds to GPIO7 ~ GPIO0 on pins ELE11/LED7 ~ ELE4/LED0 respectively. The GPIO control registers can write always regardless Stop and Run mode. The configuration of the LED driver and GPIO system is described with more detail in application note AN3894.

When the ports are not used for electrode sensing, they can be used for GPIO pins to be set as input or output, and can be used to drive LED.

Note: The number of touch sensing electrodes, and therefore the number of GPIO ports left available is configured by the Electrode Configuration register (0x5E) and GPIO Enable Register (0x77), but electrode configuration has higher priority than GPIO feature. When a pin is enabled as GPIO but is also selected as electrode by Electrode Configuration Register, the GPIO function is disabled immediately and it becomes an electrode during Run Mode.

During the Stop Mode just after power on reset, all electrodes and GPIO ports are in high impedance as all the GPIO ports and are default disabled and the electrodes are not enabled.

GPIO Registers (0x73~0x7A)

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Control 0	**0x73**	CTL0[7]	CTL0[6]	CTL0[5]	CTL0[4]	CTL0[3]	CTL0[2]	CTL0[1]	CTL0[0]
GPIO Control 1	**0x74**	CTL1[7]	CTL1[6]	CTL1[5]	CTL1[4]	CTL1[3]	CTL1[2]	CTL1[1]	CTL1[0]
GPIO Data	**0x75**	DAT[7]	DAT[6]	DAT[5]	DAT[4]	DAT[3]	DAT[2]	DAT[1]	DAT[0]
GPIO Direction	**0x76**	DIR[7]	DIR[6]	DIR[5]	DIR[4]	DIR[3]	DIR[2]	DIR[1]	DIR[0]
GPIO Enable	**0x77**	EN[7]	EN[6]	EN[5]	EN[4]	EN[3]	EN[2]	EN[1]	EN[0]
GPIO Data Set	**0x78**	SET[7]	SET[6]	SET[5]	SET[4]	SET[3]	SET[2]	SET[1]	SET[0]
GPIO Data Clear	**0x79**	CLR[7]	CLR[6]	CLR[5]	CLR[4]	CLR[3]	CLR[2]	CLR[1]	CLR[0]
GPIO Data Toggle	**0x7A**	TOG[7]	TOG[6]	TOG[5]	TOG[4]	TOG[3]	TOG[2]	TOG[1]	TOG[0]

EN, DIR, CTL0, CTL1: GPIO Enable and Input/Output Configuration Bits

When an EN bit sets, the corresponding GPIO pin is enabled and the function is configured by CTL0, CTL1 and DIR bits.

When the port is used as input, it can be configured as normal logic input with high impedance (CTL0CTL1=2b00) or input with additional internal pull-down (CTL0CTL1=2b10) or pull-up (CTL0CTL1=2b11), note the former may result unstable logic input state if opened without fixed logic level input.

For output configuration, it can be push/pull (CTL0CTL1=2b00) or open drain.

EN	DIR	CTL0:CTL1	DESCRIPTION
0	X	XX	GPIO function is disabled. Port is high impedance state if not enabled for electrode either.
1	0	00	GPIO port becomes input port.
1	0	10	GPIO port becomes input port with internal pull-down.
1	0	11	GPIO port becomes input port with internal pull-up.
1	0	01	Not defined yet (as same as CTL0:CTL1 = 00).
1	1	00	GPIO port becomes CMOS output port.
1	1	11	GPIO port becomes open drain output port with only high side MOS.
1	1	10	GPIO port becomes open drain output port with only low side MOS.
1	1	01	Not defined yet (as same as CTL0:CTL1 = 00).

DAT: GPIO Data bits

When a GPIO is enabled as output, the GPIO port outputs the corresponding DAT bit level from GPIO Data Register (0x075). The output level toggle holds on during any electrode charging and AD conversion and the level transition will be occurred after the AD conversion. Reading this register returns the content of the GPIO Data Register (not a level of the port).

When a GPIO is configured as input, reading this register returns latched input level of the corresponding port (not contents of the GPIO Data Register). A write changes content of the register, but not affect to the input function.

SET, CLR, TOG: Manipulate GPIO Data Register Content

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Write a bit with "1" to the GPIO Data Set Register, GPIO Data Clear Register, and GPIO Data Toggle Register will set/clear/toggle contents of the corresponding DAT bit in Data Register. Write "0" has no meaning. Using of those registers allows any individual port(s) to be able individually set, cleared, or toggled without affecting other ports. Reading those register returns as same as GPIO Data Register reading.

15. Software Reset Register (0x80)

Write 0x80 with 0x63 asserts soft reset. The soft reset doesn't affect I^2C module, but all others reset as same as POR.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

Table 2. Absolute Maximum Ratings - Voltage (with respect to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +3.6	V
Supply Voltage	V_{REG}	-0.3 to +2.75	V
Input Voltage SCL, SDA, $\overline{IRQ}$	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operating Temperature Range	T_O	-40 to +85	°C
GPIO Source Current per Pin	i_{GPIO}	12	mA
GPIO Sink Current per Pin	i_{GPIO}	1.2	mA
Storage Temperature Range	T_S	-40 to +125	°C

ESD AND LATCH-UP PROTECTION CHARACTERISTICS

Normal handling precautions should be used to avoid exposure to static discharge.

Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD and Latch-up Test Conditions

Rating	Symbol	Value	Unit
Human Body Model (HBM)	V_{ESD}	±2000	V
Machine Model (MM)	V_{ESD}	±200	V
Charge Device Model (CDM)	V_{ESD}	±500	V
Latch-up current at T_A = 85°C	I_{LATCH}	±100	mA

DC CHARACTERISTICS

This section includes information about power supply requirements and I/O pin characteristics.

Table 4. DC Characteristics

(Typical Operating Circuit, V_{DD} = V_{REG} = 1.8 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Supply Voltage	V_{DD}		2.0	3.3	3.6	V
Low Supply Voltage	V_{REG}		1.71	1.8	2.75	V
Average Supply Current	I_{DD}	Run1 Mode @ 1 ms sample interval		393		µA
Average Supply Current	I_{DD}	Run1 Mode @ 2 ms sample interval		199		µA
Average Supply Current	I_{DD}	Run1 Mode @ 4 ms sample interval		102		µA
Average Supply Current	I_{DD}	Run1 Mode @ 8 ms sample interval		54		µA
Average Supply Current	I_{DD}	Run1 Mode @ 16 ms sample interval		29		µA
Average Supply Current	I_{DD}	Run1 Mode @ 32 ms sample interval		17		µA
Average Supply Current	I_{DD}	Run1 Mode @ 64 ms sample interval		11		µA
Average Supply Current	I_{DD}	Run1 Mode @ 128 ms sample interval		8		µA
Measurement Supply Current	I_{DD}	Peak of measurement duty cycle		1		mA
Idle Supply Current	I_{DD}	Stop Mode		3		µA
Input Leakage Current ELE_	I_{IH}, I_{IL}			0.025		µA
Input Capacitance ELE_					15	pF
Input High Voltage SDA, SCL	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage SDA, SCL	V_{IL}				0.3 x V_{DD}	V
Input Leakage Current SDA, SCL	I_{IH}, I_{IL}			0.025	1	µA
Input Capacitance SDA, SCL					7	pF
Output Low Voltage SDA, $\overline{IRQ}$	V_{OL}	I_{OL} = 6mA			0.5V	V
Output High Voltage ELE4 - ELE11 (GPIO mode)	V_{OHGPIO}	V_{DD} = 2.7 V to 3.6 V: I_{OHGPIO} = -10 mA V_{DD} = 2.3 V to 2.7 V: I_{OHGPIO} = -6 mA V_{DD} = 1.8 V to 2.3 V: I_{OHGPIO} = -3 mA	V_{DD} - 0.5			V
Output Low Voltage ELE4 - ELE11 (GPIO mode)	V_{OLGPIO}	I_{OLGPIO} = 1 mA			0.5	V
Power On Reset	V_{TLH}	V_{DD} rising	1.08	1.35	1.62	V
	V_{THL}	V_{DD} falling	0.88	1.15	1.42	V

AC CHARACTERISTICS

Table 5. AC CHARACTERISTICS

(Typical Operating Circuit, V_{DD} and V_{REG} = 1.8 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
8 MHz Internal Oscillator	f_H		7.44	8	8.56	MHz
1 kHz Internal Oscillator	f_L		0.65	1	1.35	kHz

I²C AC CHARACTERISTICS

Table 6. I²C AC Characteristics
(Typical Operating Circuit, V_{DD} and V_{REG} = 1.8 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$				0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R			$20+0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F			$20+0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F.TX}$			$20+0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}			25		ns
Capacitive Load for Each Bus Line	C_b				400	pF

SERIAL COMMUNICATION

Introduction

The MPR121 uses an I^{2}C Serial Interface. The MPR121 operates as a slave that sends and receives data through an I^{2}C 2-wire interface. The interface uses a Serial Data Line (SDA) and a Serial Clock Line (SCL) to achieve bi-directional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MPR121, and it generates the SCL clock that synchronizes the data transfer.

The MPR121 SDA line operates as both an input and an open-drain output. A pull-up resistor, typically 4.7 kΩ, is required on SDA. The MPR121 SCL line operates only as an input. A pull-up resistor, typically 4.7 kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

The I^{2}C timing parameter is shown as below.
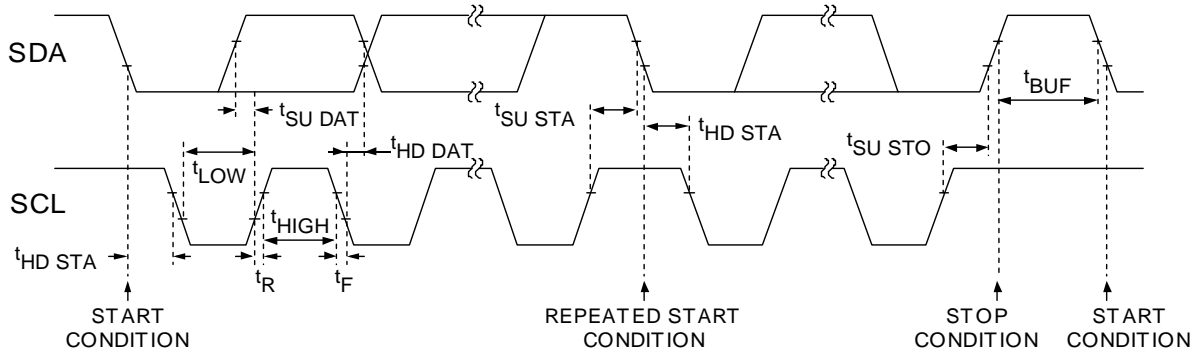
Figure 6. Serial Interface Timing Details

Start and Stop Conditions

Each transmission consists of a START (**S**) condition signaled by a master, followed by the MPR121's 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP (**P**) condition (Figure 7). Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (**S**) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (**P**) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.
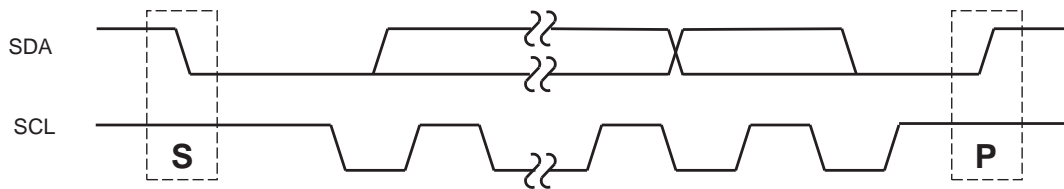
Figure 7. Start and Stop conditions

Bit Transfer

One data bit is transferred during each clock pulse (Figure 8). The data on SDA must remain stable while SCL is high.
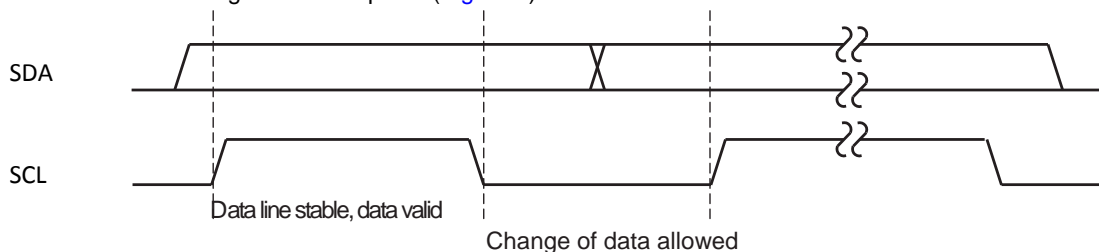
Figure 8. Bit Transfer

Operation with Multiple Masters

The application should use repeated starts to address the MPR121 to avoid bus confusion between I^{2}C masters. On an I^{2}C bus, once a master issues a start/repeated start condition, that master owns the bus until a stop condition occurs. If a master that does not own the bus attempts to take control of that bus, then improper addressing may occur. An address may always be rewritten to fix this problem. Follow I^{2}C protocol for multiple master configurations.

MPR121 Slave Address and R/W bit

MPR121 use a 7-bit format slave address which is pin configurable by ADDR pin connection. The MPR121 slave addresses can be configured as shown in Table 7.

Table 7.

ADDR Pin Connection	I^{2}C Address
VDD	0x5A
VSS	0x5B
SDA	0x5C
SCL	0x5D

The MPR121 monitors the bus continuously, waiting for a START condition followed by its slave address. The bit following the 7-bit slave address (the 8th bit) is the R/W bit, which is low for a write command and high for a read command (Figure 9). When a MPR121 recognizes its slave address, it acknowledges and is then ready for continued communication.
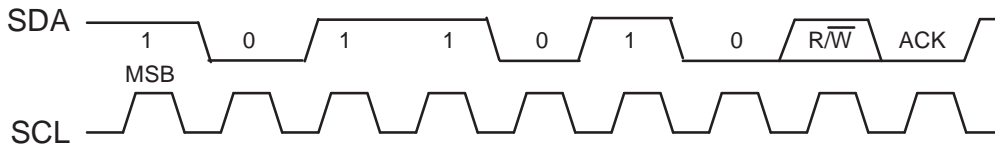
Figure 9. Slave Address

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 11) which the recipient uses to handshake receipt of each byte of data. Thus each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MPR121, the MPR121 generates the acknowledge bit, since the MPR121 is the recipient. When the MPR121 is transmitting to the master, the master generates the acknowledge bit, since the master is the recipient.
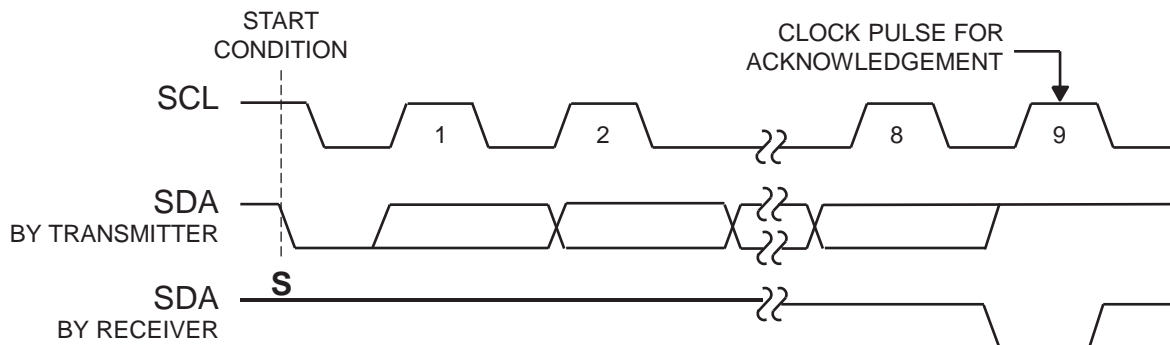
Figure 10. Acknowledge

Write Format

A write to the MPR121 comprises the transmission of the MPR121's slave address with the R/$\overline{W}$ bit set to 0, followed by at least one byte of information. The first byte of information is the command byte. The command byte determines which register of the MPR121 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the command byte is just stored in the register pointer and the MPR121 takes no further action (Figure 11) beyond storing the command byte.
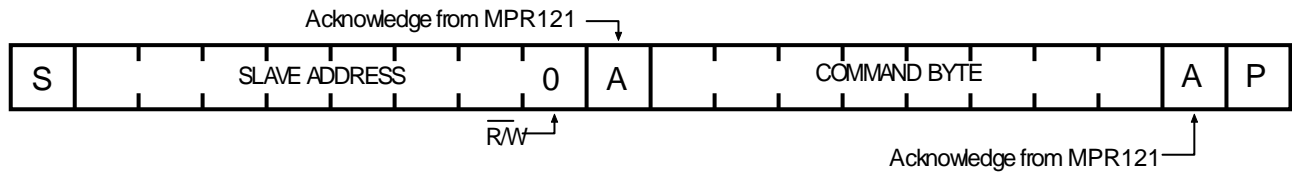
Figure 11. Write format with command byte only

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MPR121 selected by the command byte (Figure 12). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MPR121 internal registers because the command byte address generally auto-increments (see Table 1) for the address auto-increment change.
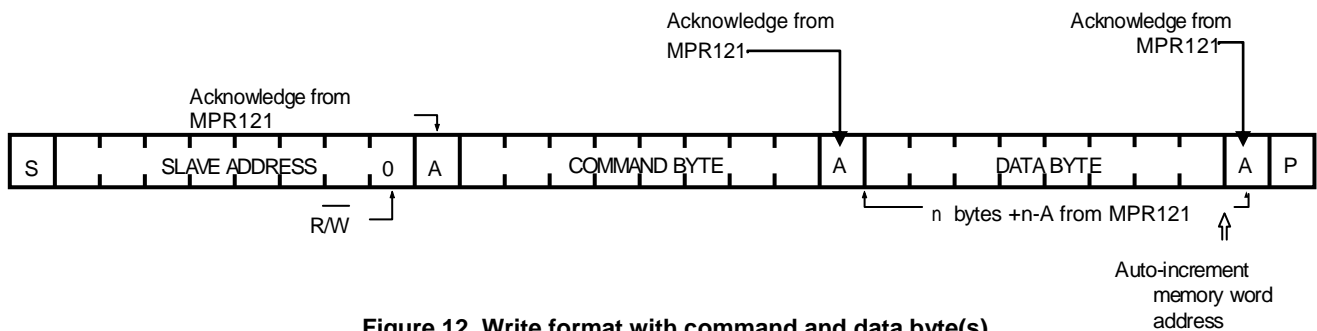
Figure 12. Write format with command and data byte(s)

Read Format

MPR121 is read using MPR121's internally register pointer, the same way the stored register address is used as address pointer for a write. The pointer generally auto-increments after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring MPR121's register address by performing a write command byte (Figure 13) followed by a repeated start (**Sr**). The master can now read 'n' consecutive bytes from MPR121, with first data byte being read from the register addressed by the initialized register address, and ending the read be a not-acknowledge (**NA**) before a STOP (**P**).
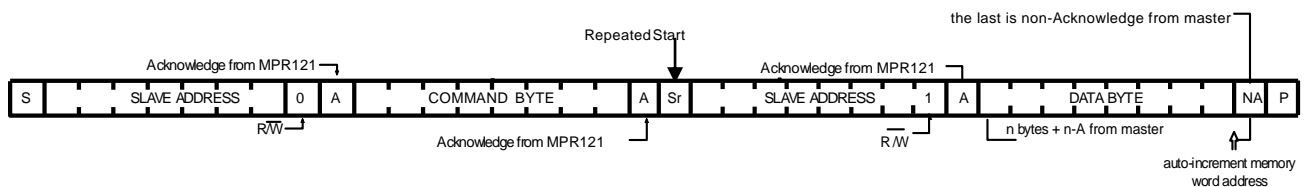
**Figure 13. Read format with command adn and data
and data byte(s)**

PACKAGE DIMENSIONS
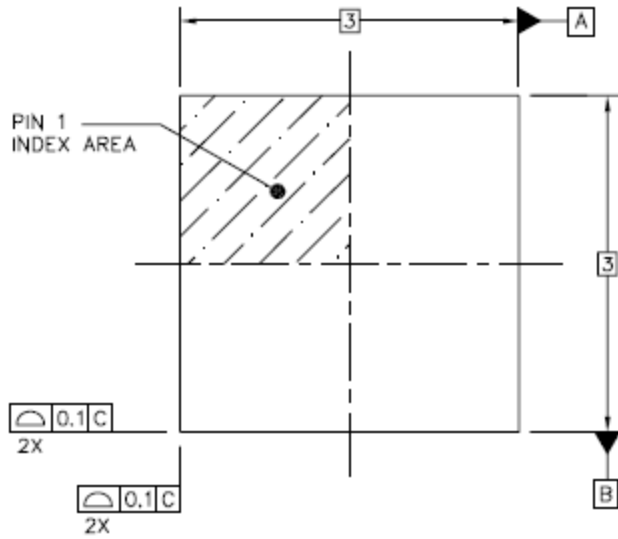
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. THIS IS NON JEDEC REGISTERED PACKAGE.

4. COPLANARITY APPLIES TO LEADS AND ALL OTHR BOTTOM SURFACE METALLIZATION.

5. MIN. METAL GAP SHOULD BE 0.2MM.
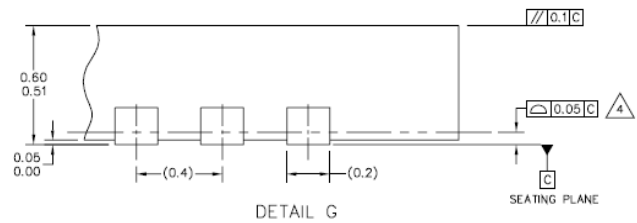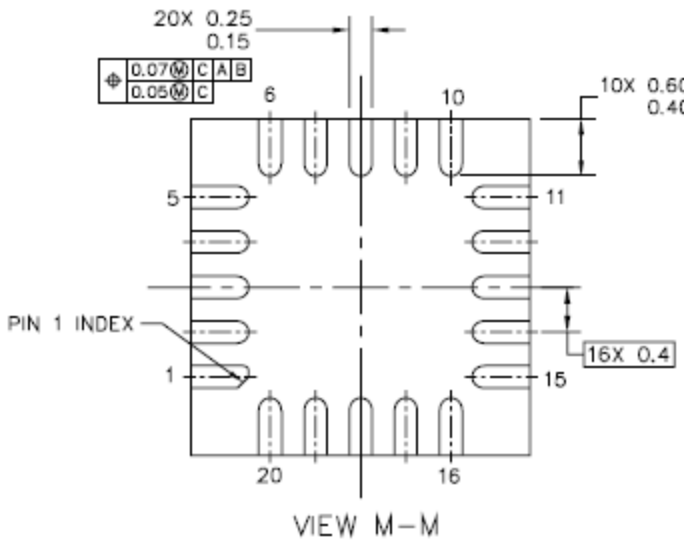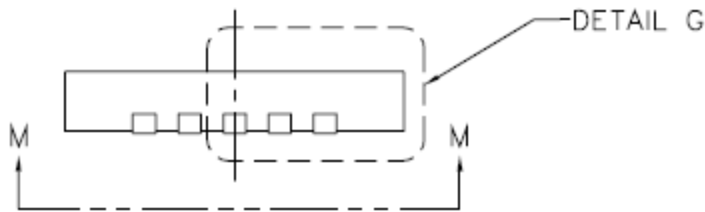
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