AN4123
Application note

STEVAL-ISV015V1 up to 2.5 W solar USB charger

By Domenico Ragonese

Introduction

The STEVAL-ISV015V1 is a demonstration board mounting the SPV1040 device (solar energy harvester) as input stage and the LD39050PUR device (low noise and low quiescent current voltage regulator) as output stage. It targets any portable application powered by USB supply and merges the capability of the SPV1040 device to maximize the power extraction from solar modules with the high precision voltage regulation of the LD39050 device. It is shown in *Figure 1*.

Figure 1. STEVAL-ISV015V1 demonstration board

The board has been designed to harvest power from PV panels and to supply loads requiring up to 2.5 W (5 V, 500 mA) through a mini-USB (B type) connector. Between the two stages, a 440 mF super capacitor stores the harvested energy even when load is not connected or, if connected, it needs less power than that available from the source.
The application components at the input stage have been selected to optimize the energy harvesting from polycrystalline PV panels composed of 2, 3 and 4 PV cells in series and able to supply up to 900 mA. The trimmer VR3 is connected between the PV panel and the MPP-SET pin of the SPV1040 device and allows the maximum power extraction from the selected PV panel to be fine tuned. Setting the VR3 = 1 kΩ is recommended to cover most application cases.
So, other PV panels can also be used but it may be necessary to replace some of the application components in order to make the system work in the most efficient way.
The PV panel and main application components can be replaced, but the following guidelines must be carefully considered:

- The PV panel can be selected as long as V_{OC} < 5.5 V and I_{SC} < 1.65 A
- The inductor L1 can be replaced by considering that it affects the maximum peak current and that an input overcurrent limit (1.65 A) does not have to be triggered
- The maximum output current can be limited by inserting the current sensing resistor RS1 (0 Ω by default)

For further details on component selection, please refer to Section 6 “External component selection” of the AN3319 application note. For details on the SPV1040 device and the LD39050 device features, please refer to the related datasheets.

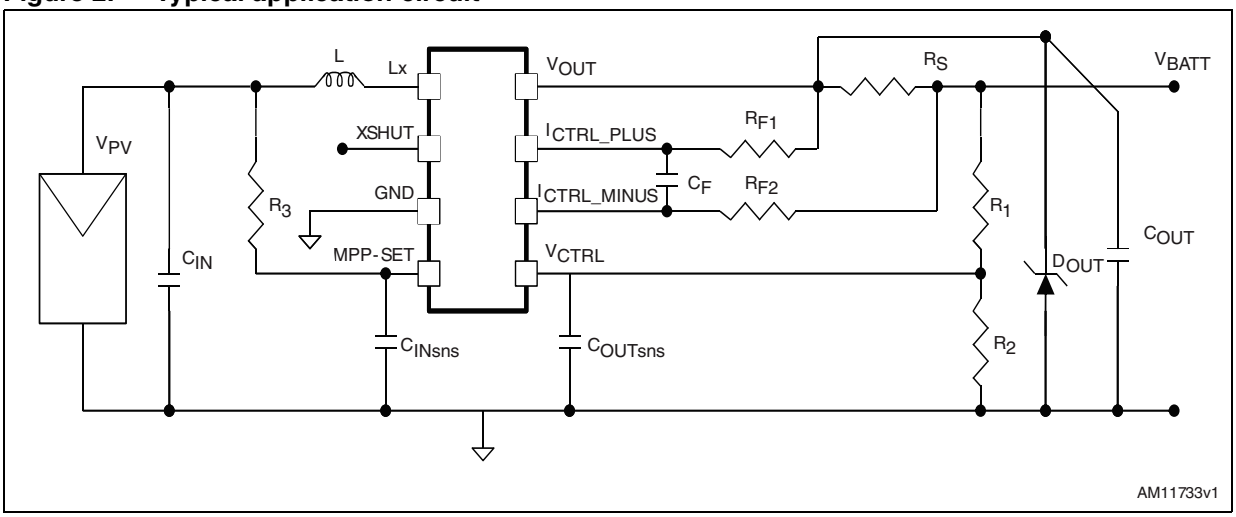
Contents

1 SPV1040 operating description

The SPV1040 device is a high efficiency, low power and low voltage DC-DC converter that provides a single output voltage up to 5.2 V. The combination of the SPV1040 device and the LD39050 device provides an optimal solution to supply devices requiring a regulated voltage.

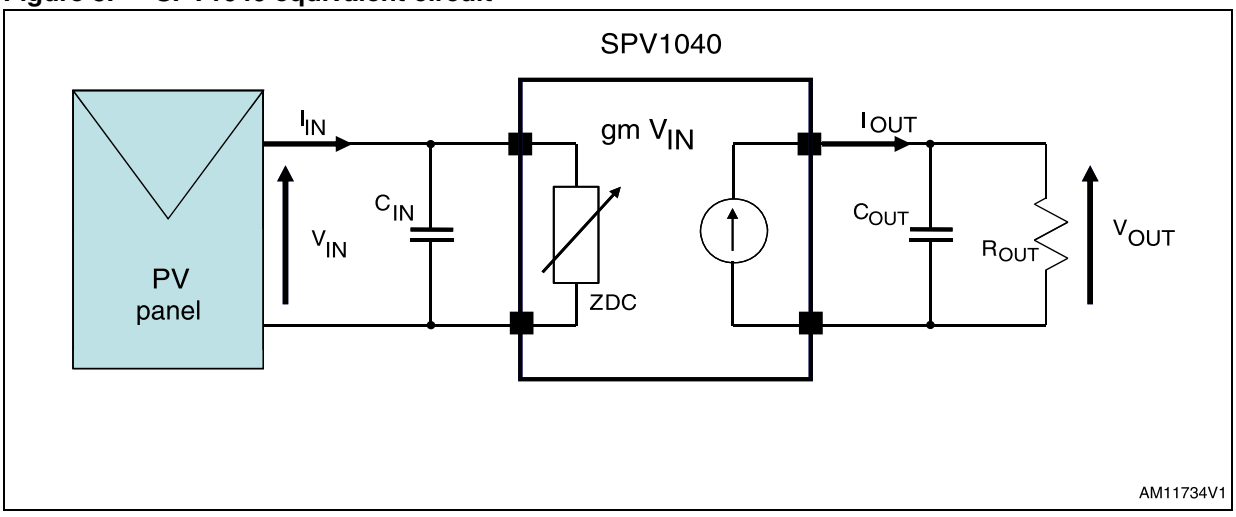
The SPV1040 device is a 100 kHz fixed frequency PWM step-up converter able to maximize the energy harvested by few solar cells thanks to the embedded MPPT algorithm which maximizes the power generated from the panel by continuously tracking its output voltage and current. The converter guarantees the overall application safety and its own safety by stopping the PWM switching in the case of overvoltage, overcurrent or overtemperature condition. The IC integrates a 120 mΩ N-channel MOSFET power switch and a 140 mΩ P-channel MOSFET synchronous rectifier.

Figure 2. Typical application circuit



The SPV1040 device acts as an impedance adapter between the PV module and the output load. In fact, the equivalent circuit can be shown as in *Figure 3*.

Figure 3. SPV1040 equivalent circuit



The MPPT algorithm sets up the DC working point properly by guaranteeing $Z_{IN} = Z_M$ (assuming Z_M the impedance of the supply source). In this way, the power extracted from the supply source ($P_{IN} = V_{IN} \times I_{IN}$) is maximum ($P_M = V_M \times I_M$).

The voltage current curve shows all the available working points of the PV panel at a given solar irradiation. The voltage power curve is derived from the voltage current curve by plotting the product V x I for each voltage generated. For further details on the MPPT algorithm, please refer to the SPV1040 device datasheet.

Figure 4. MPPT working principle

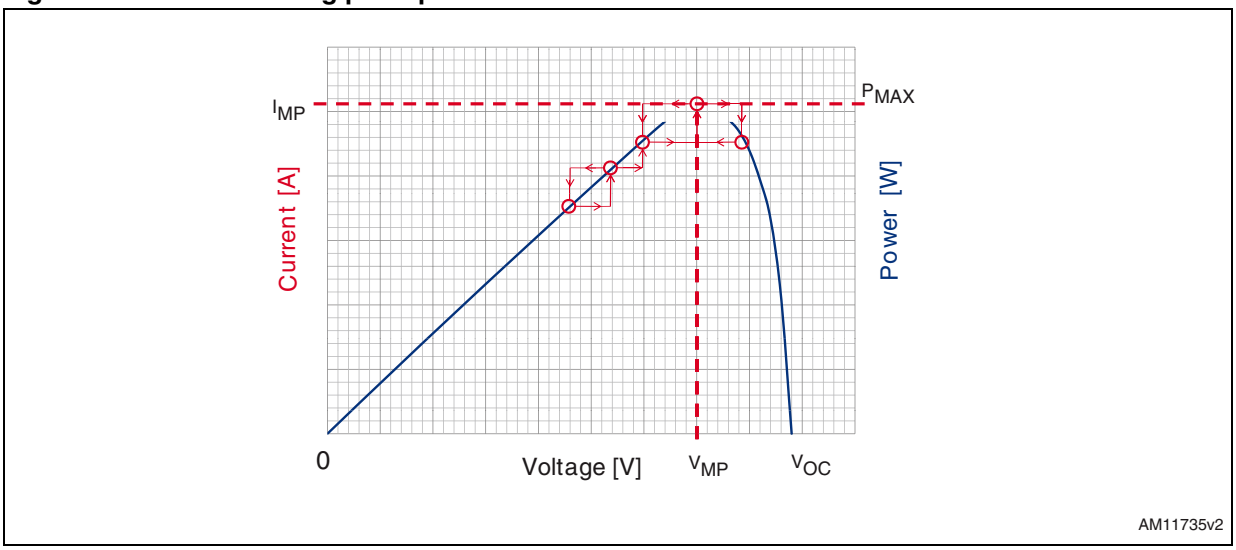
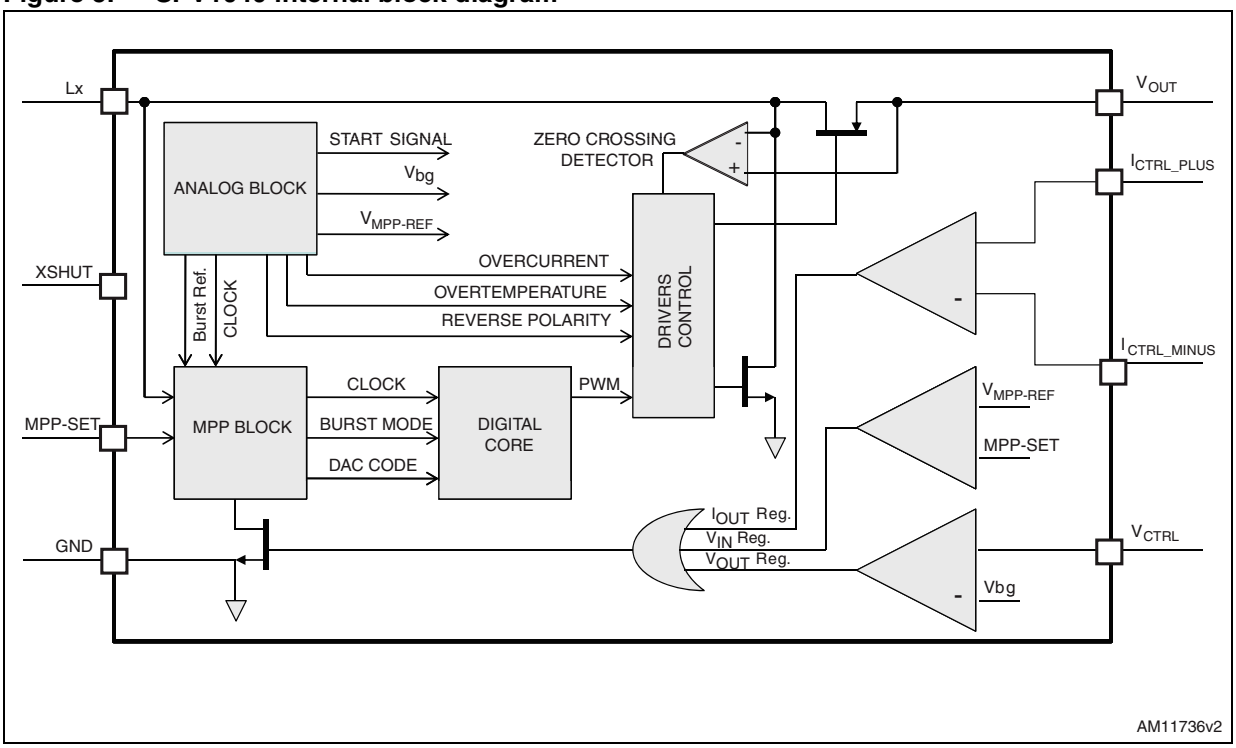


Figure 5. SPV1040 internal block diagram



The duty cycle set by the MPPT algorithm can be overwritten if one of the following conditions is triggered:

- Input overcurrent protection (OVC): inductor peak current ≥ 1.65 A
- Overtemperature protection (OVT): internal temperature ≥ 155 °C
- Output voltage regulation: V_{CTRL} triggers the 1.25 V internal reference
- Output current limitation: RS1 x (I_{CTRL_PLUS} - I_{CTRL_MINUS}) ≥ 50 mV
- MPP-SET voltage $V_{MPP-SET}$ ≤ 300 mV at the startup and $V_{MPP-SET}$ ≤ 450 mV in running mode.

Application components must be carefully selected to avoid any undesired triggering of the above thresholds.

2 LD39050 operating description

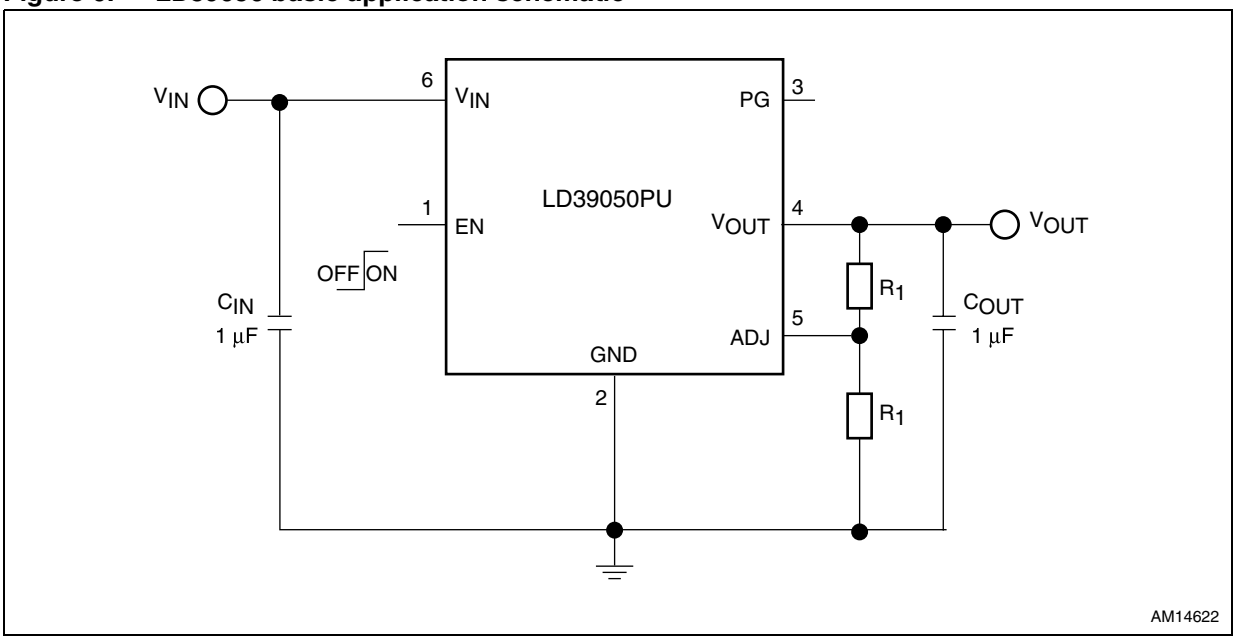
The LD39050 device is an ultra low dropout linear regulator with low quiescent current and low noise features that make it suitable for low power battery powered applications. It provides up to 500 mA with a low 200 mV dropout. The input voltage range is from 1.5 V up to 5.5 V. For this application the device is used in its adjustable output version, with a reference voltage of 0.8 V.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

The power supply rejection is 65 dB at low frequencies and starts to roll off at 10 kHz. An Enable logic control function puts the LD39050 device in shutdown mode allowing a total current consumption lower than 1 µA.

An internal thermal feedback loop disables the output voltage if the die temperature rises to approximately 160 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device.

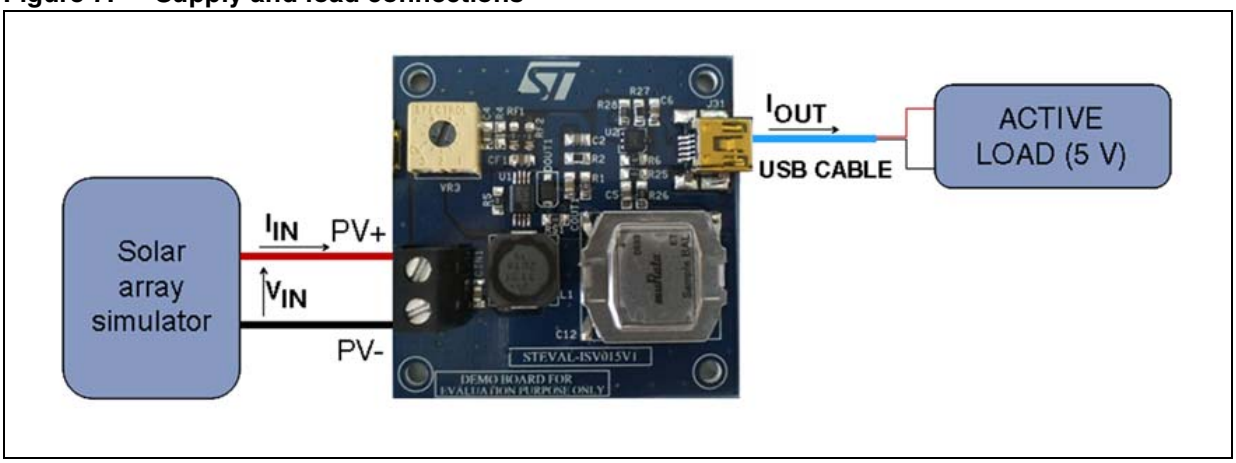
Figure 6. LD39050 basic application schematic



3 Reference design description

The setup environment used for the measurement campaign is shown in *Figure 7*.

Figure 7. Supply and load connections



An electric “solar array simulator” (SAS, SAS-FL05/01 from CBL Electronics) has been used to simulate polycrystalline PV modules with 2, 3 and 4 PV cells in series and with different sizes to supply currents from 100 mA up to 900 mA (by 100 mA steps). *Figure 8* to *Figure 13* show the I-V and P-V curves generated by the SAS, obtained using a PV module analyzer ISM490 from ISOTECH (only 100 mA and 900 mA cases are reported).

Figure 8. 2 cells in series, 100 mA

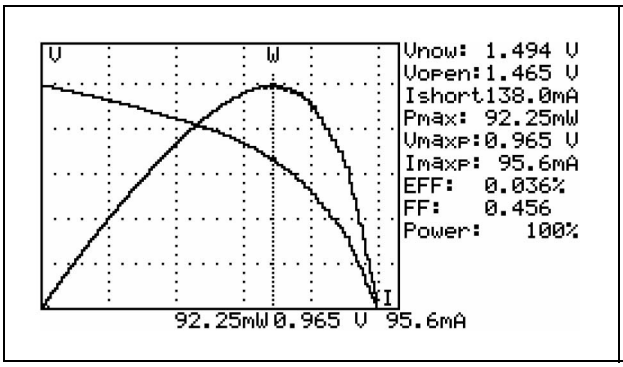


Figure 9. 3 cells in series, 100 mA

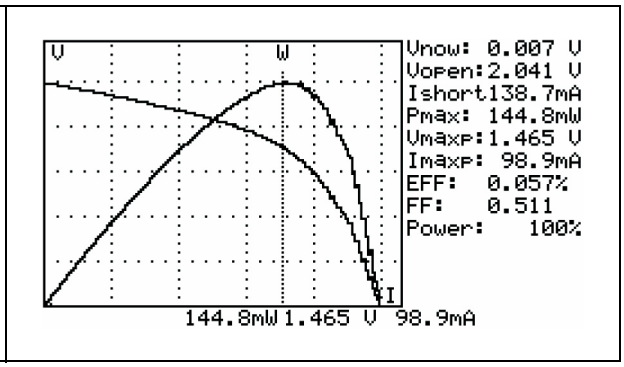


Figure 10. 4 cells in series, 100 mA

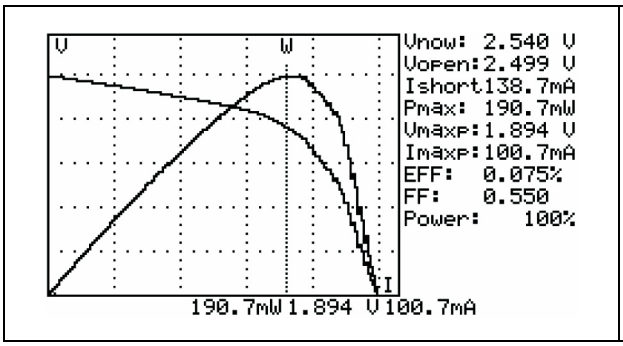


Figure 11. 2 cells in series, 900 mA

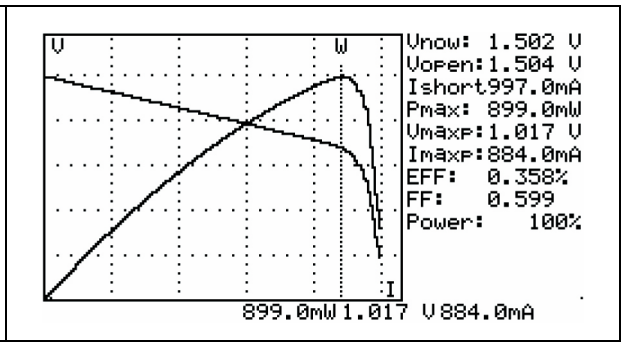


Figure 12. 3 cells in series, 900 mA

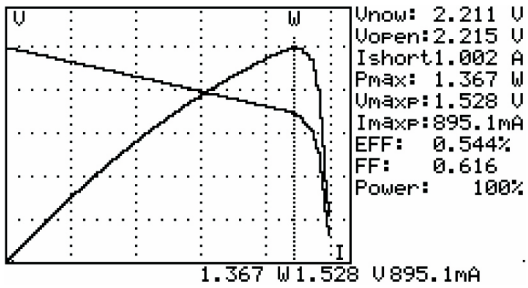


Figure 13. 4 cells in series, 900 mA

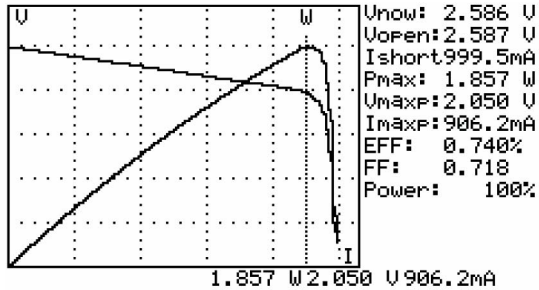
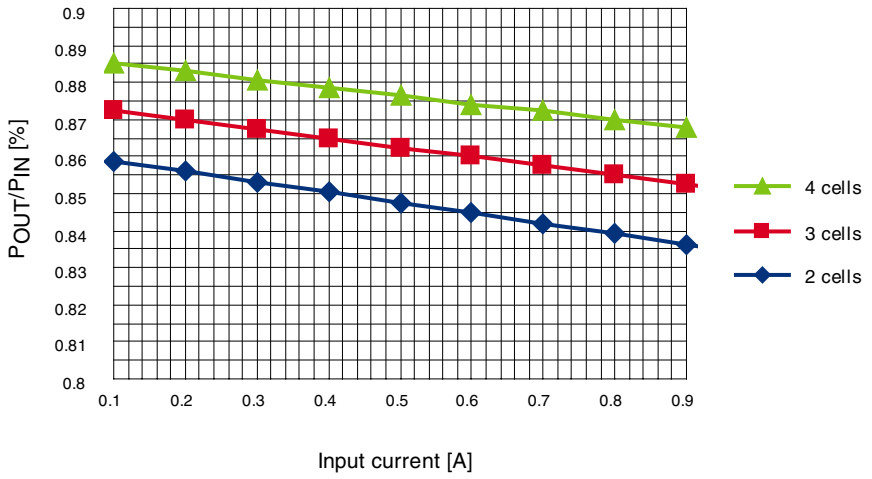


Figure 14 shows the system efficiency (P_{OUT}/P_{IN}) when the load is an active load configured in “constant voltage mode” set to 5 V:

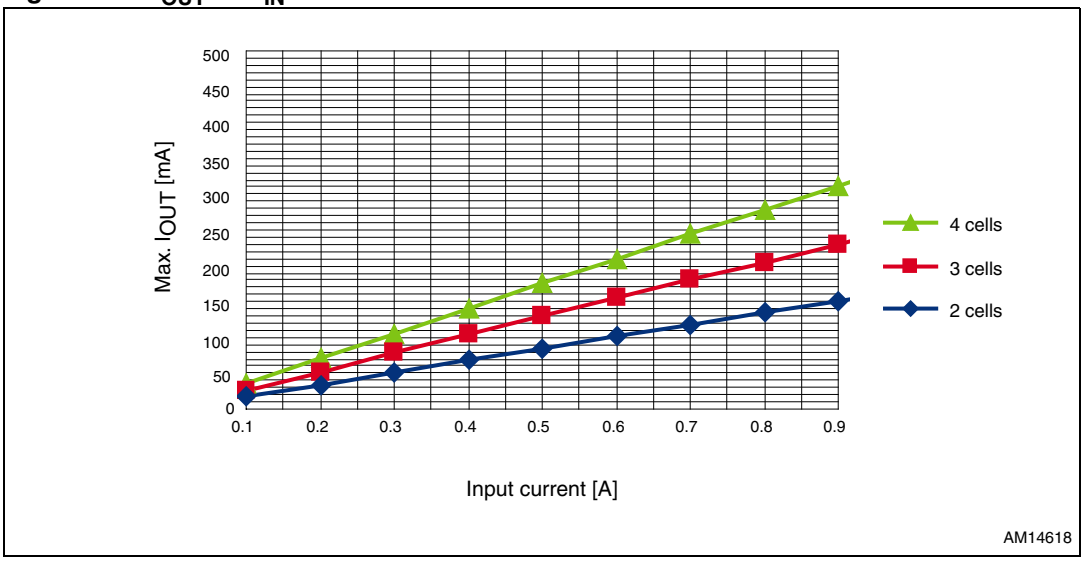
Figure 14. System efficiency



The power supplied by the PV panel depends on the actual irradiation, so that if the load should require more power than available, the output voltage (5 V) is sustained by the supercapacitor according to the amount of charge previously stored. When charge is no longer available in the supercapacitor, the output voltage drops.

Figure 15 shows the maximum available output current versus the input current when PV module with 2, 3 or 4 cells in series is used.

Figure 15. I_{OUT} vs. I_{IN}



Obviously, in case of low irradiation or lower maximum power extractable from the panel, the maximum output current drawn by the load must be properly reduced in order to avoid any undesired output voltage drop. *Figure 16* to *Figure 18* show the same data but highlighting the maximum output current versus the input power provided by the PV panel.

Figure 16. Max. I_{OUT} vs. P_{IN} (2 cells in series)

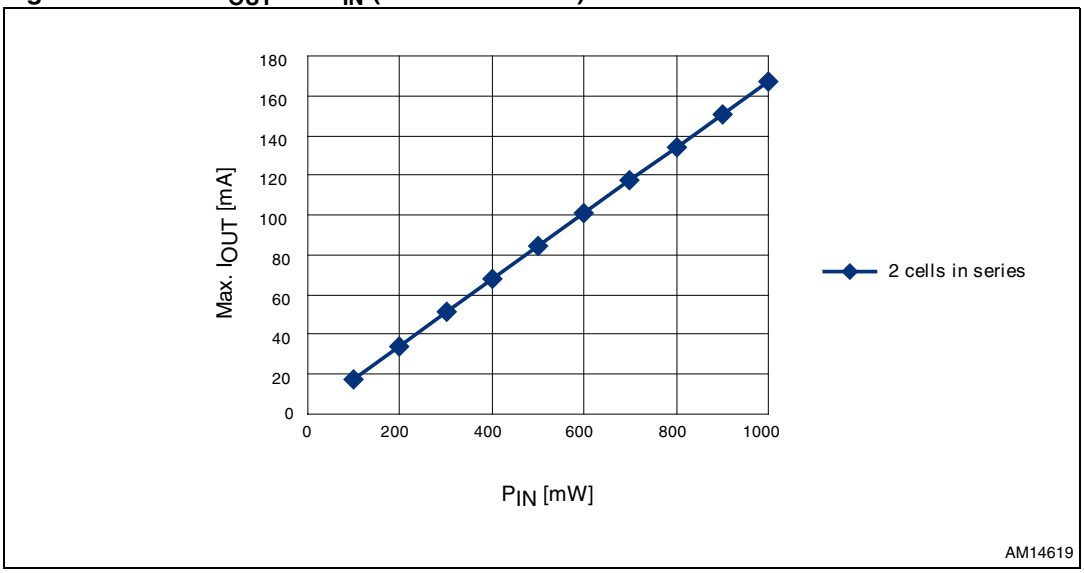


Figure 17. Max. I_{OUT} vs. P_{IN} (3 cells in series)

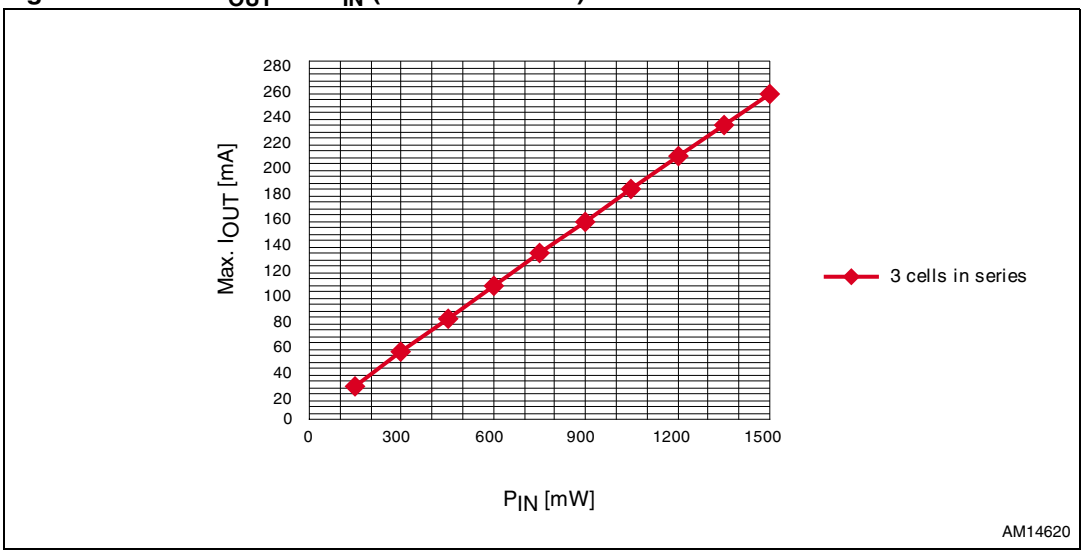
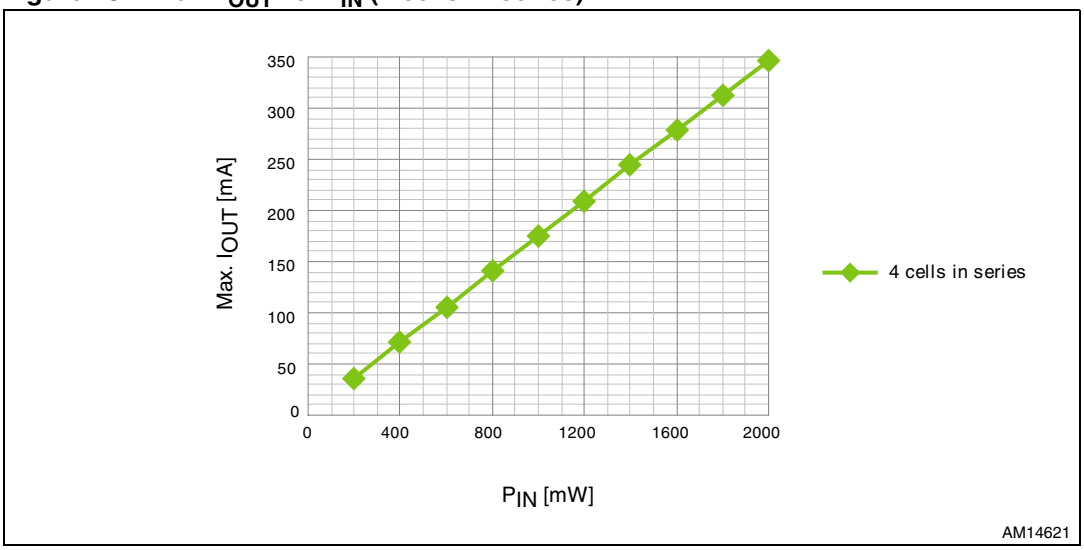


Figure 18. Max. I_{OUT} vs. P_{IN} (4 cells in series)



4 Schematic and bill of material

The schematic, bill of material and Gerber files can be downloaded at: http://ims.st.com/referencedesign/photovoltaic.php

Figure 19. Schematic

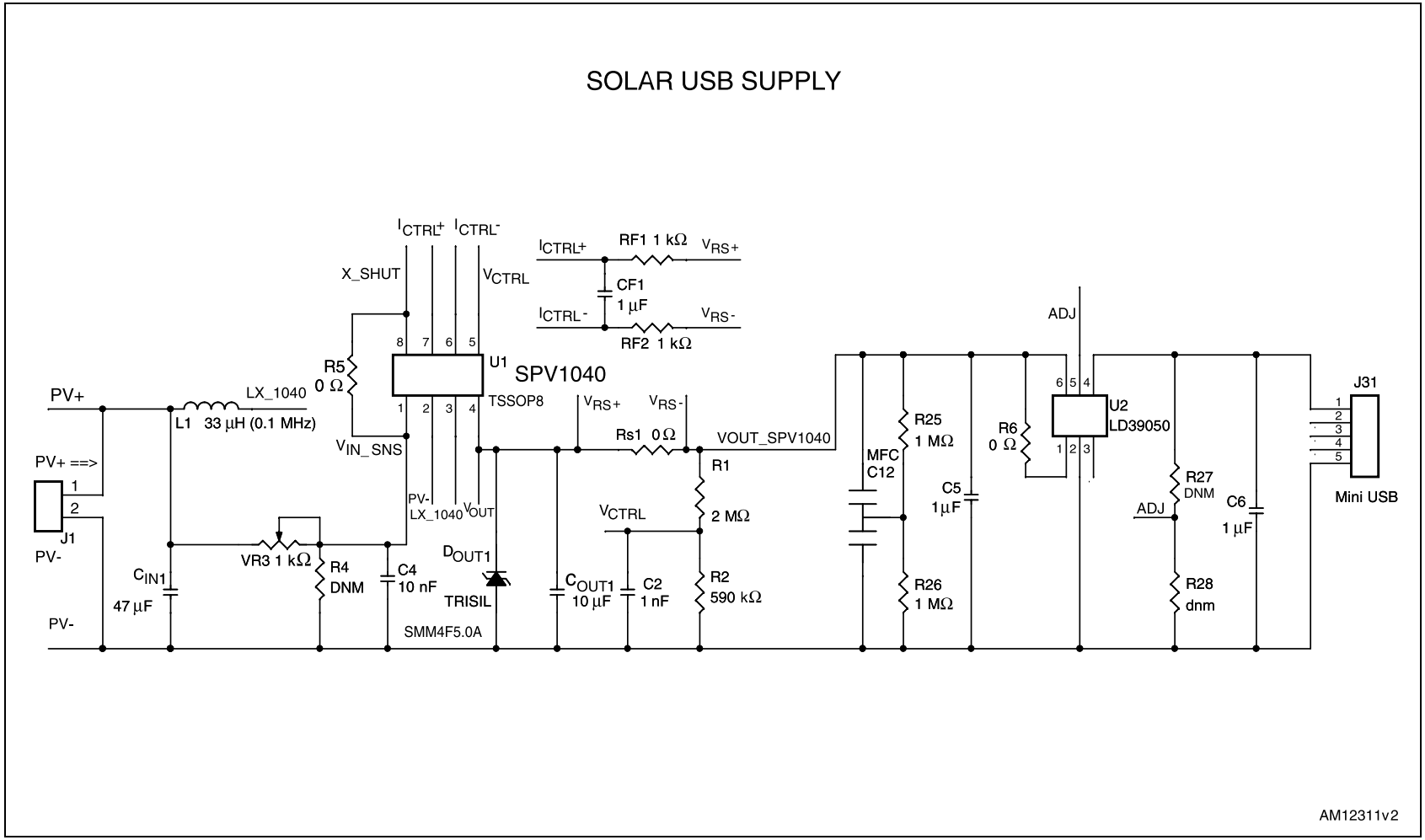


Table 1 reports the list of components of the STEVAL-ISV015V1 device.

Table 1. Bill of material

Item	Qty.	Reference	Part / value	Tolerance (%)	Voltage current	WATT	Technology information	Package	Manufacturer	Manufacturer code
1	1	J1	2-pin screw connector					TH-5 mm	PHOENIX CONTACT	1935161
2	1	C_{IN1}	47 µF		6.3 V			0805	KEMET	C0805C476M9PAC7800
3	1	C2	1 nF		50 V			0805	KEMET	C0805C102K5RAC
4	1	C4	10 nF		50 V			0805	KEMET	C0805C103K5RAC
5	1	C_{OUT1}	10 µF		16 V			0805	KEMET	C0805C106K4PAC7800
6	1	VR3	(0-1 kΩ)			500 mW		63M	VISHAY	63M-102
7	0	R4	DNM					0805		
7	1	L1	33 µH		I_{SAT} > 2 A, I_{RMS} 1.8 A				Coilcraft EPCOS	MSS1038-333 B82464G4
8	1	RS1	0 Ω		50 mV at I_{OUT_MAX}	125 mW		0805	VISHAY	CRCW08050000Z0EA
9	1	R1	2 MΩ			125 mW		0805	VISHAY	CRCW08052M00FKEA
10	1	R2	590 kΩ			125 mW		0805	Panasonic	ERA6AEB5903V
11	2	R5, R6	0 Ω			125 mW		0805	VISHAY	CRCW08050000Z0EA
13	1	U1	SPV1040					TSSOP8	STMicroelectronics	SPV1040T
14	1	D_{OUT1}	SMM4F5.0		V_{BR} = 5 V, V_{CL} = 9 V			ST MITE FLAT	STMicroelectronics	SMM4F5.0
15	2	RF1, RF2	1 kΩ			125 mW		0805	VISHAY	CRCW08051K00FKEA
17	3	CF1, C5, C6	1 µF		10 V			0805	Murata Manufacturing, Co., Ltd.	GRM21BR71C105KA01L
20	1	U2	LD39050					MLPD 3 x 3	STMicroelectronics	LD39050
21	1	J31	Mini-USB-B					Mini-USB-B	MOLEX®	548190578

Table 1. Bill of material (continued)

Item	Qty.	Reference	Part / value	Tolerance (%)	Voltage current	WATT	Technology information	Package	Manufacturer	Manufacturer code
22	1	C12	MFC						Murata Manufacturing, Co., Ltd.	MFC
23	2	R25, R26	1 MΩ			125 mW		0805	Multicomp	MC0805S8F1004T5E
25	1	R27	53.6 kΩ			125 mW		0805	Panasonic	ERA6AEB5362V
26	1	R28	10.2 kΩ			125 mW		0805	VISHAY	MC0805S8F1004T5E

Layout

PCB silkscreen

Figure 20. Silkscreen view

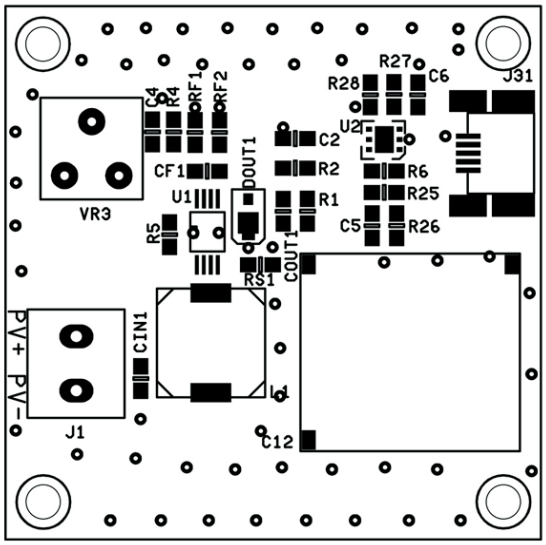


Figure 21. Top view

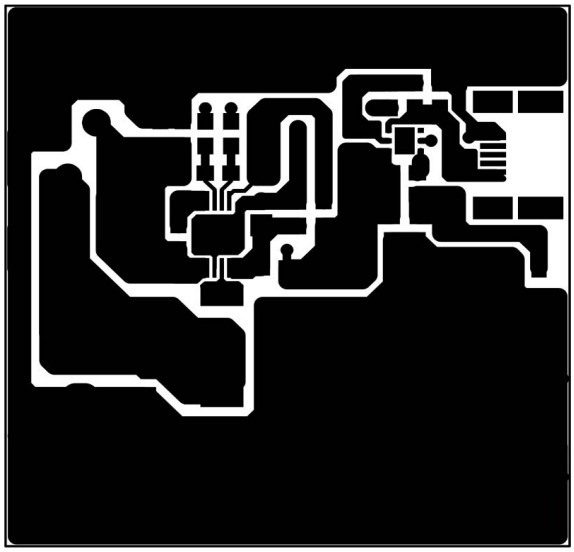
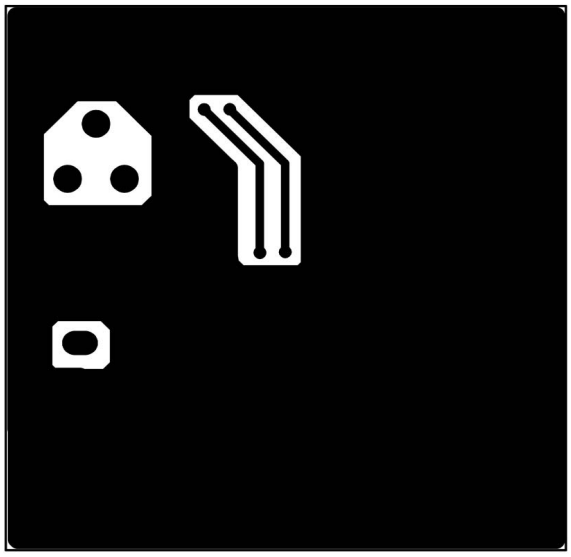


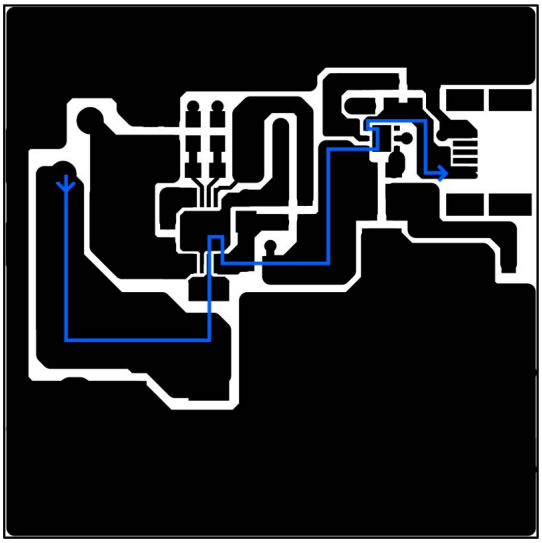
Figure 22. Bottom view



Special care must be taken in the layout of the input and output stages both for optimizing the losses on the high current paths and for the placement of critical application components.

The high current path is highlighted by the blue line in *Figure 23*:

Figure 23. High current path



For the SPV1040 device, the output current sensing resistor (RS1) and output capacitor (C_{OUT1}) must be placed as close as possible to its V_{OUT} pin. The output current sense circuit (RF1, RF2 and CF1) must be designed as symmetrical as possible, in order to guarantee the noise immunity on the voltage drop measurement across RS1.

For the LD39050 device, both input and output capacitors (C5 and C6, respectively) must be connected within 0.5" to V_{IN} and V_{OUT} pins. The PC board copper area soldered to the exposed pad acts as a heatsink, therefore, the wider it is the better the heat exchange toward the surrounding ambient is. Feed-through vias to inner and/or bottom copper layers are also needed to improve the overall thermal performance of the device.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
17-Jul-2012	1	Initial release.