

FEATURES

- Offset voltage: 400 μ V typical**
- Low offset voltage drift: 6 μ V/ $^{\circ}$ C maximum (AD8692/AD8694)**
- Very low input bias currents: 1 pA maximum**
- Low noise: 8 nV/ $\sqrt{\text{Hz}}$**
- Low distortion: 0.0006%**
- Wide bandwidth: 10 MHz**
- Unity-gain stable**
- Single-supply operation: 2.7 V to 6 V**
- Qualified for automotive applications**

APPLICATIONS

- Photodiode amplification**
- Battery-powered instrumentation**
- Medical instruments**
- Multipole filters**
- Sensors**
- Portable audio devices**

GENERAL DESCRIPTION

The AD8691, AD8692, and AD8694 are low cost, single, dual, and quad rail-to-rail output, single-supply amplifiers featuring low offset and input voltages, low current noise, and wide signal bandwidth. The combination of low offset, low noise, very low input bias currents, and high speed make these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from this combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion of these devices.

Applications for these amplifiers include power amplifier (PA) controls, laser diode control loops, portable and loop-powered instrumentation, audio amplification for portable devices, and ASIC input and output amplifiers.

The small SC70 and TSOT package options for the AD8691 allow it to be placed next to sensors, thereby reducing external noise pickup.

The AD8691, AD8692, and AD8694 are specified over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$. The AD8691 single is available in 5-lead SC70 and 5-lead TSOT packages. The AD8692 dual is available in 8-lead MSOP and narrow SOIC surface-mount packages. The AD8694 quad is available in 14-lead TSSOP and narrow 14-lead SOIC packages.

See the Ordering Guide section for automotive grades.

PIN CONFIGURATIONS

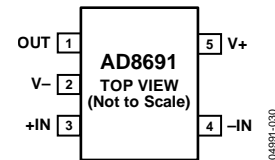


Figure 1. 5-Lead TSOT

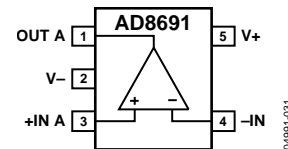


Figure 2. 5-Lead SC70

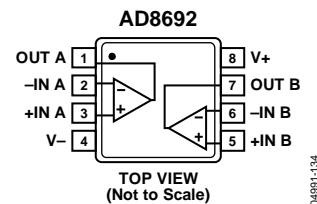


Figure 3. 8-Lead SOIC and 8-Lead MSOP

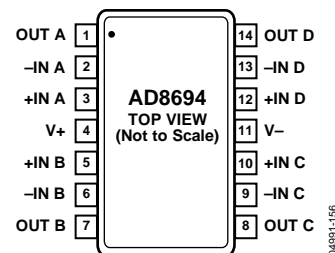


Figure 4. 14-Lead SOIC and 14-Lead TSSOP

Rev. F

Document Feedback

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REVISION HISTORY

9/13—Rev. E to Rev. F

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| Changes to Figure 3 and Figure 4..... | 1 |
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| Changes to Ordering Guide | 14 |

8/11—Rev. D to Rev. E

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11/10—Rev. C to Rev. D

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| Changes to Ordering Guide | 14 |
| Added Automotive Products Section | 14 |

5/07—Rev. B to Rev. C

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| Changes to Large Signal Voltage Gain Values in Table 1 | 3 |
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3/05—Rev. A to Rev. B

| | |
|--------------------|-----------|
| Added AD8694 | Universal |
|--------------------|-----------|

1/05—Rev. 0 to Rev. A

| | |
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| Changes to Features | 1 |
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| Changes to Figure 9..... | 6 |
| Updated Outline Dimensions | 11 |
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10/04—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 2.7\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|--------------------------|--|------|----------|------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.4 | 2.0 | mV |
| Input Bias Current | I_B | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.2 | 1 | pA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.1 | 0.5 | pA |
| Input Voltage Range | | | -0.3 | | +1.6 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 68 | 90 | | dB |
| Large Signal Voltage Gain | A_{VO} | $R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }2.2\text{ V}$ $R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }2.2\text{ V}$ | 90 | 250 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 2 | 12 | $\mu\text{V}/^\circ\text{C}$ |
| | | | | 1.3 | 6 | $\mu\text{V}/^\circ\text{C}$ |
| INPUT CAPACITANCE | | | | | | |
| Common-Mode Input Capacitance | C_{CM} | | | 5 | | pF |
| Differential Input Capacitance | C_{DM} | | | 2.5 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 2.64 | 2.66 | | V |
| Output Voltage Low | V_{OL} | $I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 25 | 40 | mV |
| Short-Circuit Current | I_{SC} | | | ± 20 | | mA |
| Closed-Loop Output Impedance | Z_{OUT} | $f = 1\text{ MHz}$, $A_v = 1$ | | 12 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S = 2.7\text{ V to }5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 80 | 95 | | dB |
| Supply Current/Amplifier | I_{SY} | $V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 75 | 95 | | dB |
| | | | | 0.85 | 0.95 | mA |
| | | | | | 1.2 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 2\text{ k}\Omega$ | | 5 | | V/ μs |
| Settling Time | t_s | To 0.01% | | 1 | | μs |
| Gain Bandwidth Product | GBP | | | 10 | | MHz |
| Phase Margin | ϕ_m | | | 60 | | Degrees |
| Total Harmonic Distortion + Noise | THD + N | $G = 1$, $R_L = 600\ \Omega$, $f = 1\text{ kHz}$, $V_O = 250\text{ mV p-p}$ | | 0.003 | | % |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{n\text{ p-p}}$ | $f = 0.1\text{ Hz to }10\text{ Hz}$ | | 1.6 | 3.0 | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 8 | 12 | nV/ $\sqrt{\text{Hz}}$ |
| | e_n | $f = 10\text{ kHz}$ | | 6.5 | | nV/ $\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.05 | | pA/ $\sqrt{\text{Hz}}$ |

$V_S = 5.0\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|--------------------------|--|------|----------|------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $V_{CM} = -0.3\text{ V to }+3.9\text{ V}$ $V_{CM} = -0.1\text{ V to }+3.9\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.4 | 2.0 | mV |
| Input Bias Current | I_B | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.2 | 1 | pA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.1 | 0.5 | pA |
| Input Voltage Range | | | -0.3 | | +3.9 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = -0.3\text{ V to }+3.9\text{ V}$ $V_{CM} = -0.1\text{ V to }+3.9\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 70 | 95 | | dB |
| Large Signal Voltage Gain | A_{VO} | $V_O = 0.5\text{ V to }4.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{CM} = 0\text{ V}$ $V_O = 0.5\text{ V to }4.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{CM} = 0\text{ V}$ | 250 | 2000 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | | | $\mu\text{V}/^\circ\text{C}$ |
| | | | | 2 | 12 | $\mu\text{V}/^\circ\text{C}$ |
| | | | | 1.3 | 6 | $\mu\text{V}/^\circ\text{C}$ |
| INPUT CAPACITANCE | | | | | | |
| Common-Mode Input Capacitance | C_{CM} | | | 5 | | pF |
| Differential Input Capacitance | C_{DM} | | | 2.5 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C to }+125^\circ\text{C}$ | 4.96 | 4.98 | | V |
| | | | 4.7 | 4.78 | | V |
| | | | 4.6 | | | V |
| Output Voltage Low | V_{OL} | $I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C to }+125^\circ\text{C}$ $-40^\circ\text{C to }+125^\circ\text{C}$ | | 20 | 40 | mV |
| | | | | 165 | 210 | mV |
| | | | | 185 | 240 | mV |
| | | | | | 290 | mV |
| | | | | | 370 | mV |
| Short-Circuit Current | I_{SC} | | | ± 80 | | mA |
| Closed-Loop Output Impedance | Z_{OUT} | $f = 1\text{ MHz}$, $A_V = 1$ | | 10 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S = 2.7\text{ V to }5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 80 | 95 | | dB |
| | | | 75 | 95 | | dB |
| Supply Current/Amplifier | I_{SY} | $V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | 0.95 | 1.05 | mA |
| | | | | | 1.3 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 2\text{ k}\Omega$ | | 5 | | V/ μs |
| Settling Time | t_S | To 0.01% | | 1 | | μs |
| Full Power Bandwidth | BW_P | <1% distortion | | 360 | | kHz |
| Gain Bandwidth Product | GBP | | | 10 | | MHz |
| Phase Margin | ϕ_m | | | 65 | | Degrees |
| Total Harmonic Distortion + Noise | THD + N | $G = 1$, $R_L = 600\ \Omega$, $f = 1\text{ kHz}$, $V_O = 1\text{ V p-p}$ | | 0.0006 | | % |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{n\text{ p-p}}$ | $f = 0.1\text{ Hz to }10\text{ Hz}$ | | 1.6 | 3.0 | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 8 | 12 | nV/ $\sqrt{\text{Hz}}$ |
| | e_n | $f = 10\text{ kHz}$ | | 6.5 | | nV/ $\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.05 | | pA/ $\sqrt{\text{Hz}}$ |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|--------------------------------------|--|
| Supply Voltage | 6 V |
| Input Voltage | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ |
| Differential Input Voltage | $\pm 6\text{ V}$ |
| Output Short-Circuit Duration to GND | Observe derating curves |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Operating Temperature Range | -40°C to $+125^\circ\text{C}$ |
| Junction Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, the device soldered in the circuit board for surface-mount packages.

Table 4. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|-----------------------|---------------|---------------|---------------------------|
| 8-Lead MSOP (RM-8) | 210 | 45 | $^\circ\text{C}/\text{W}$ |
| 8-Lead SOIC (R-8) | 158 | 43 | $^\circ\text{C}/\text{W}$ |
| 5-Lead TSOT (UJ-5) | 207 | 61 | $^\circ\text{C}/\text{W}$ |
| 5-Lead SC70 (KS-5) | 376 | 126 | $^\circ\text{C}/\text{W}$ |
| 14-Lead TSSOP (RU-14) | 180 | 35 | $^\circ\text{C}/\text{W}$ |
| 14-Lead SOIC (R-14) | 120 | 36 | $^\circ\text{C}/\text{W}$ |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = +5\text{ V}$ or $\pm 2.5\text{ V}$, unless otherwise noted.

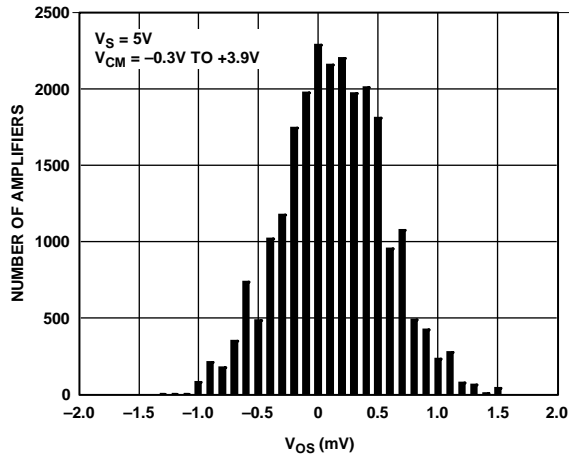


Figure 5. Input Offset Voltage Distribution

04991-003

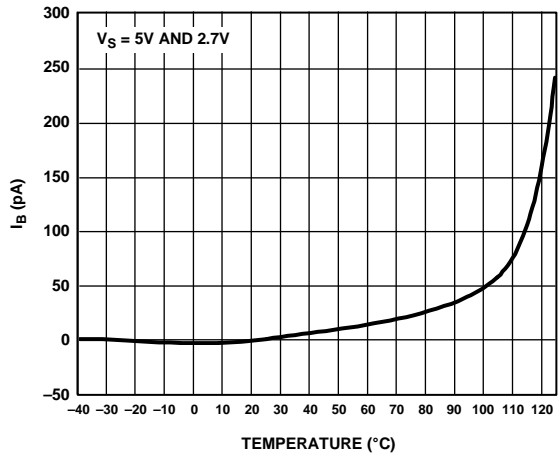


Figure 8. Input Bias Current vs. Temperature

04991-006

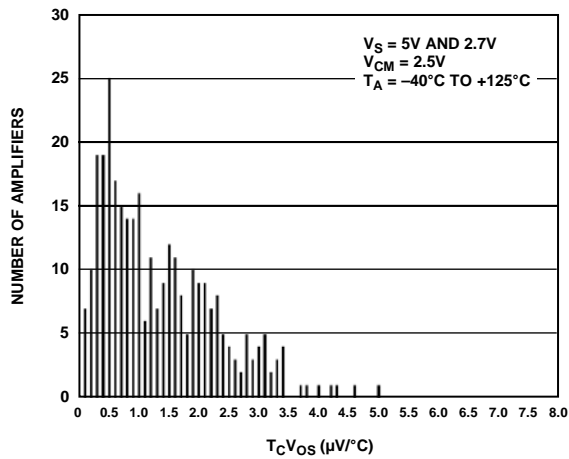


Figure 6. AD8692/AD8694 Input Offset Voltage Drift Distribution

04991-004

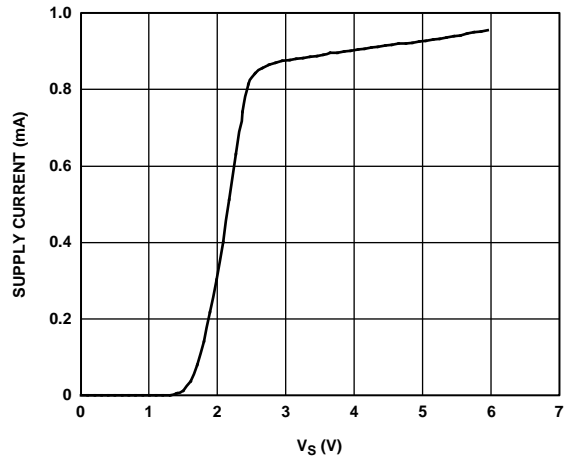


Figure 9. Supply Current vs. Supply Voltage

04991-007

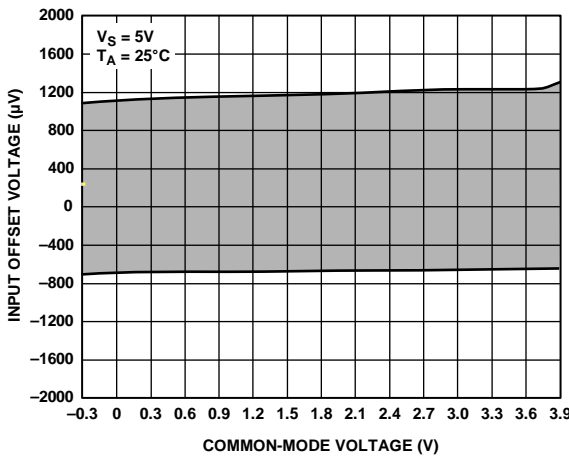


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

04991-005

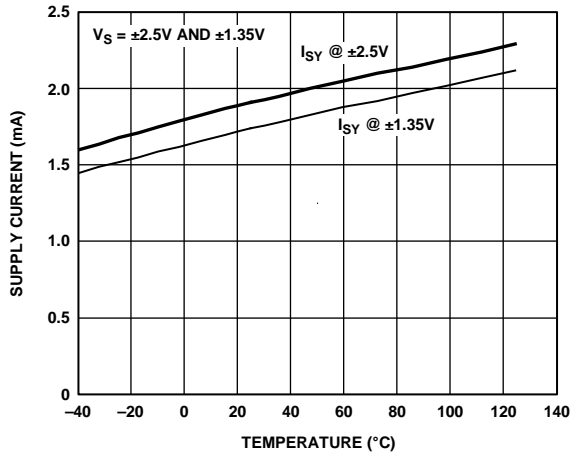


Figure 10. Supply Current vs. Temperature

04991-008

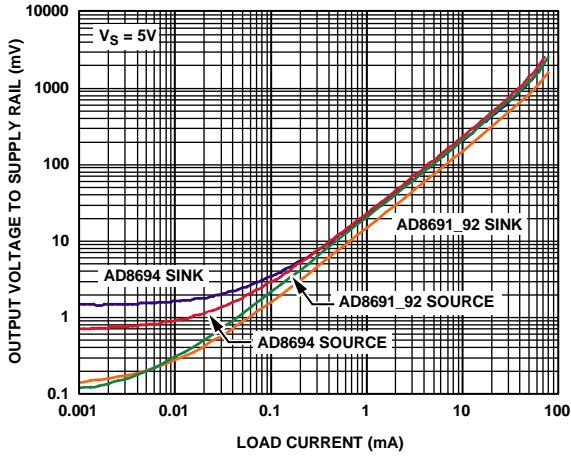


Figure 11. Output Voltage to Supply Rail vs. Load Current

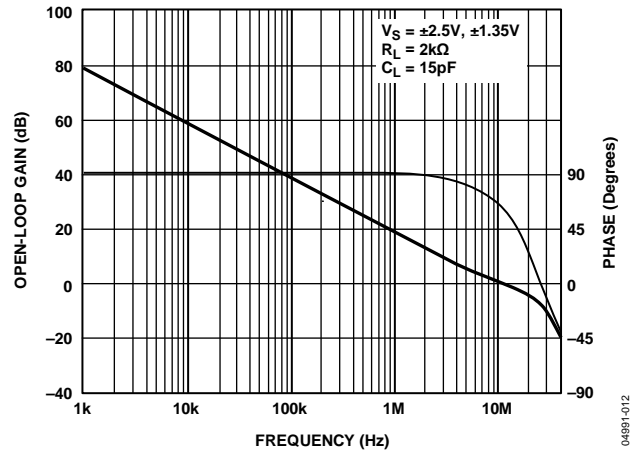


Figure 14. Open-Loop Gain and Phase vs. Frequency

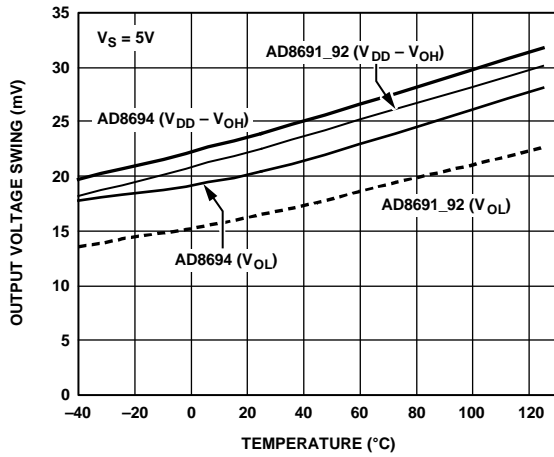


Figure 12. Output Voltage Swing vs. Temperature ($I_L = 1 \text{ mA}$)

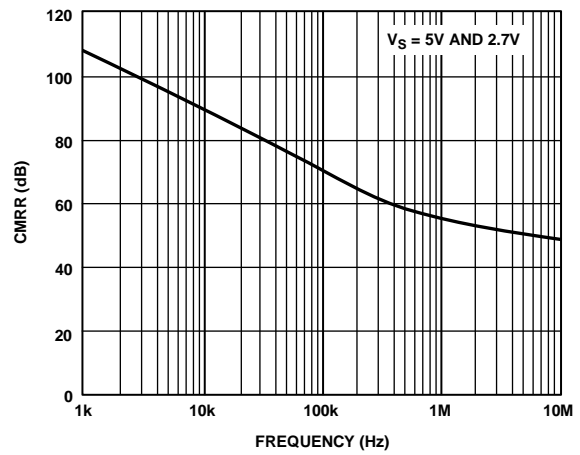


Figure 15. CMRR vs. Frequency

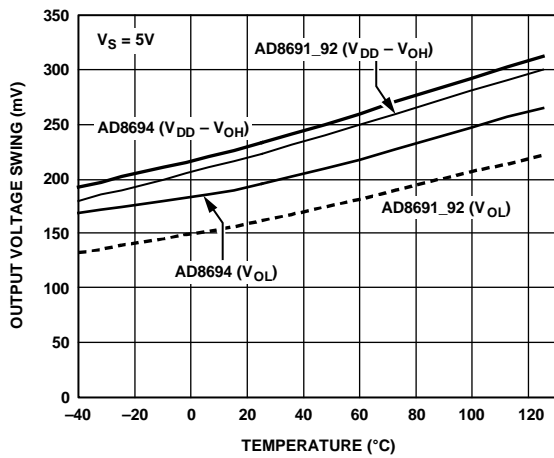


Figure 13. Output Voltage Swing vs. Temperature ($I_L = 10 \text{ mA}$)

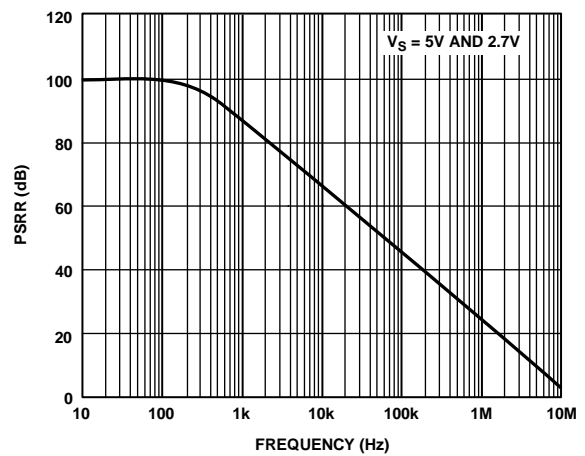


Figure 16. PSRR vs. Frequency

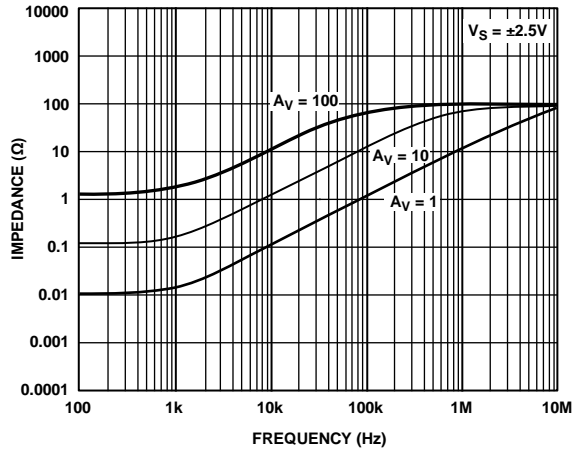


Figure 17. Closed-Loop Output Impedance vs. Frequency

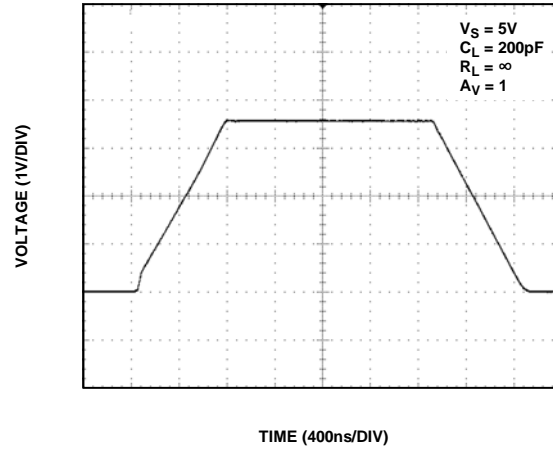


Figure 20. Large Signal Transient Response

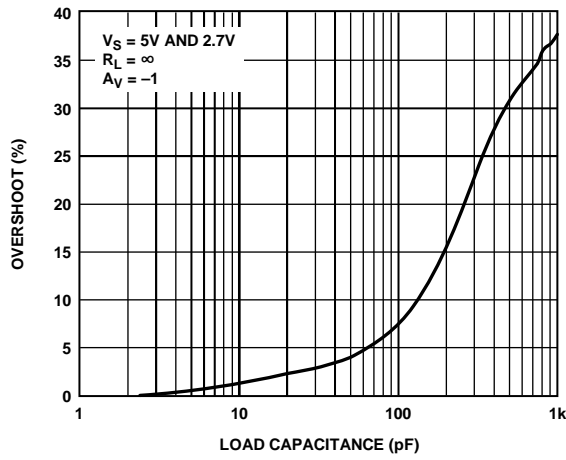


Figure 18. Small Signal Overshoot vs. Load Capacitance

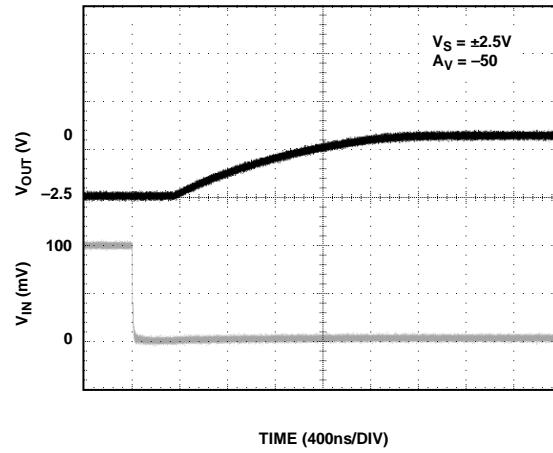


Figure 21. Positive Overload Recovery

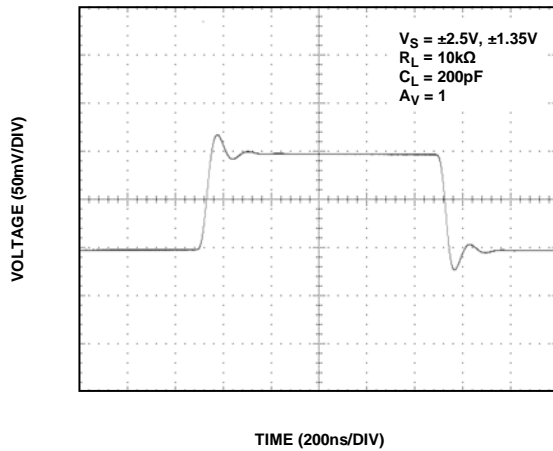


Figure 19. Small Signal Transient Response

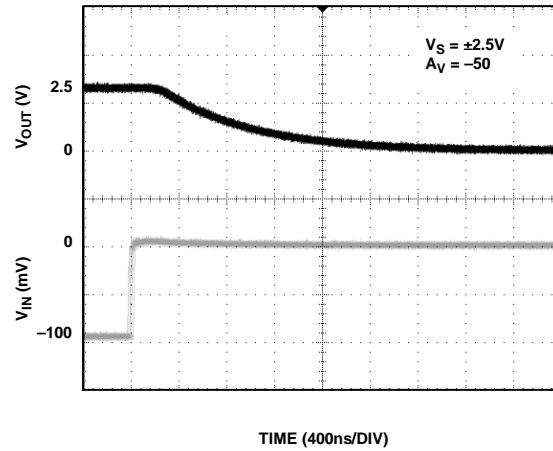


Figure 22. Negative Overload Recovery

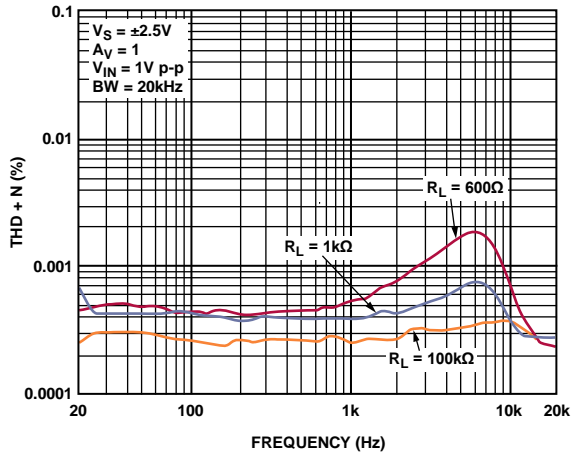


Figure 23. THD + N vs. Frequency

04891-021

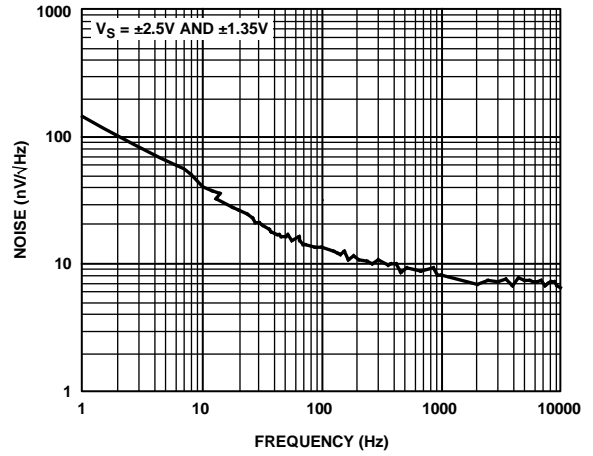


Figure 25. Voltage Noise Density

04891-023

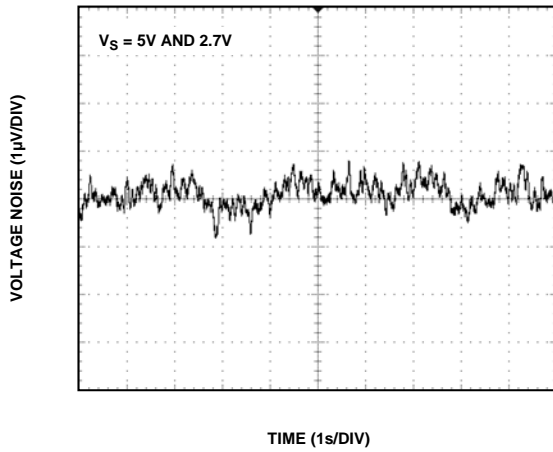


Figure 24. 0.1 Hz to 10 Hz Input Voltage Noise

04891-022

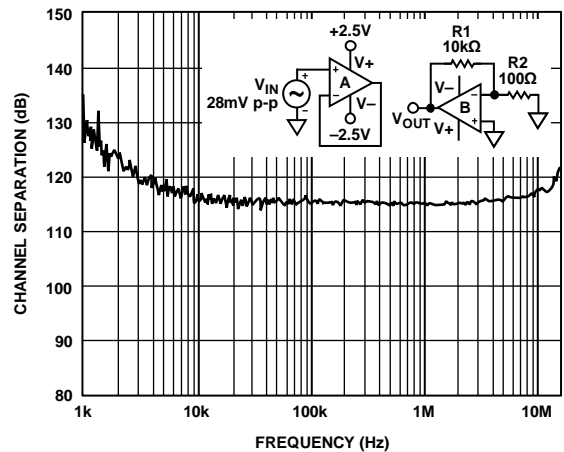


Figure 26. AD8692/AD8694 Channel Separation

04891-024

$V_S = +2.7\text{ V}$ or $\pm 1.35\text{ V}$, unless otherwise noted.

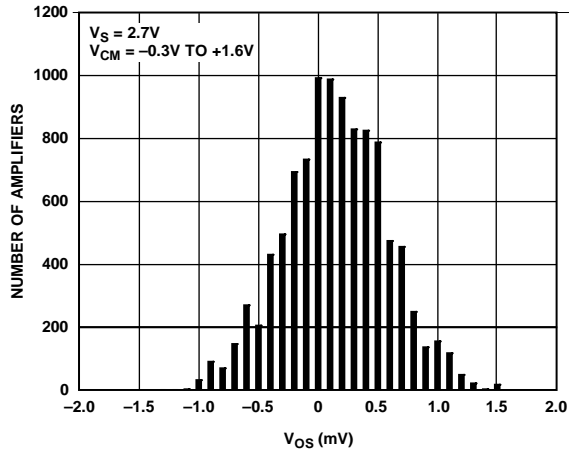


Figure 27. Input Offset Voltage Distribution

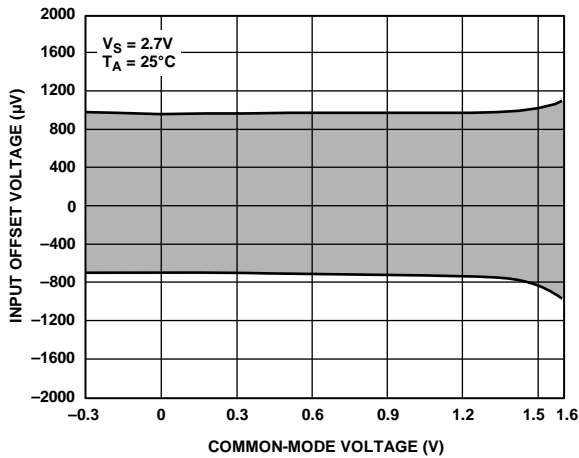


Figure 28. Input Offset Voltage vs. Common-Mode Voltage

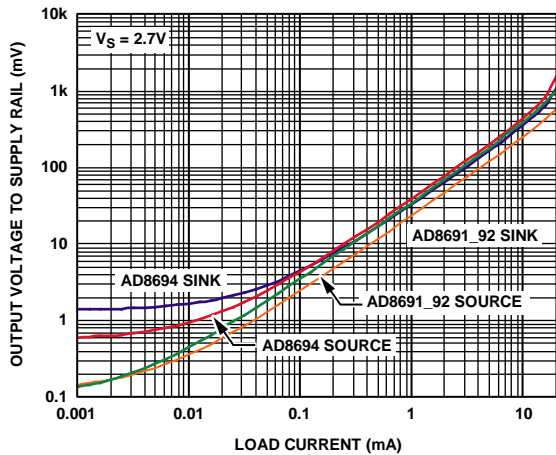


Figure 29. Output Voltage to Supply Rail vs. Load Current

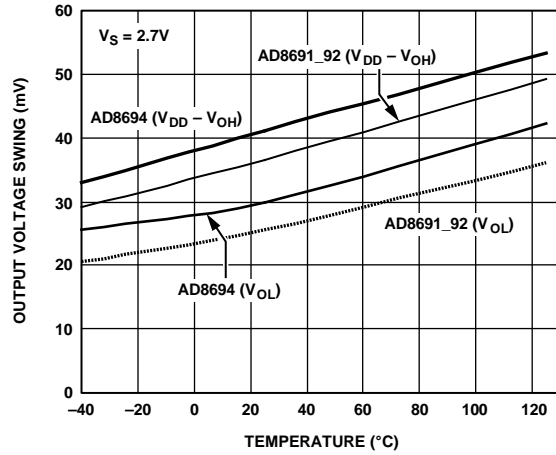


Figure 30. Output Voltage Swing vs. Temperature ($I_L = 1\text{ mA}$)

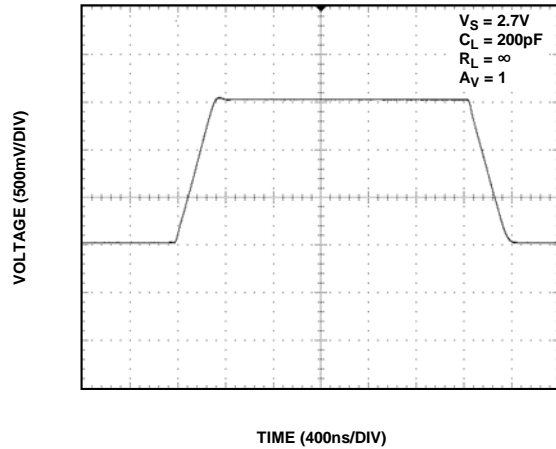


Figure 31. Large Signal Transient Response

04991-025

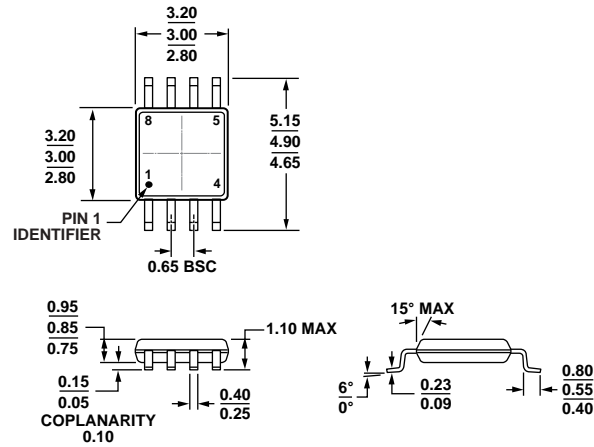
04991-028

04991-026

04991-023

04991-027

OUTLINE DIMENSIONS

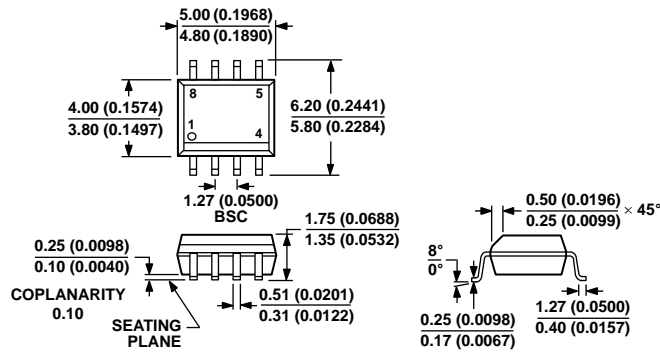


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 32. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2008-B



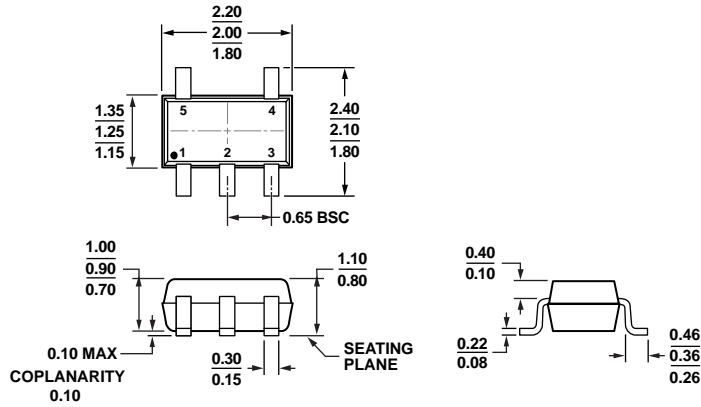
COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 33. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A

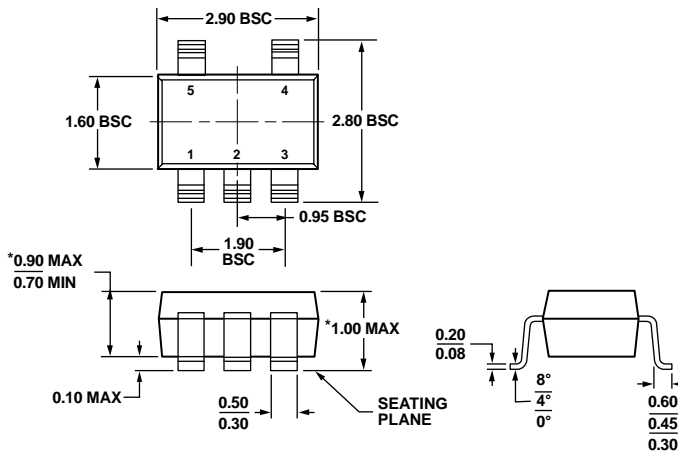


COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 34. 5-Lead Thin Shrink Small Outline Package [SC70] (KS-5)

Dimensions shown in millimeters

072809-A

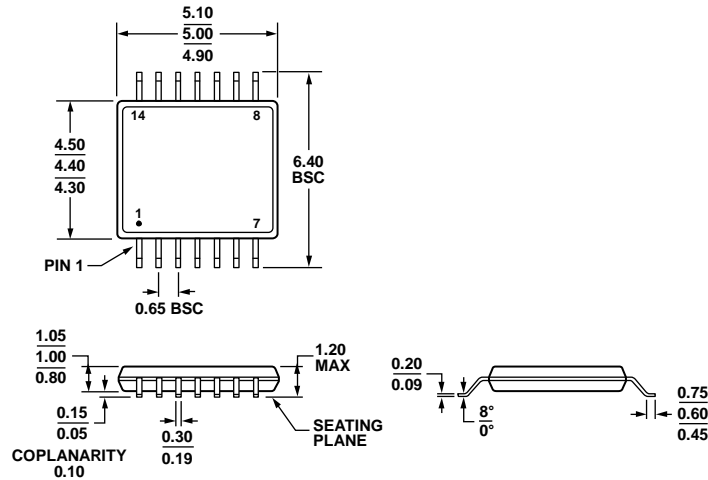


*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 35. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)

Dimensions shown in millimeters

100708-A

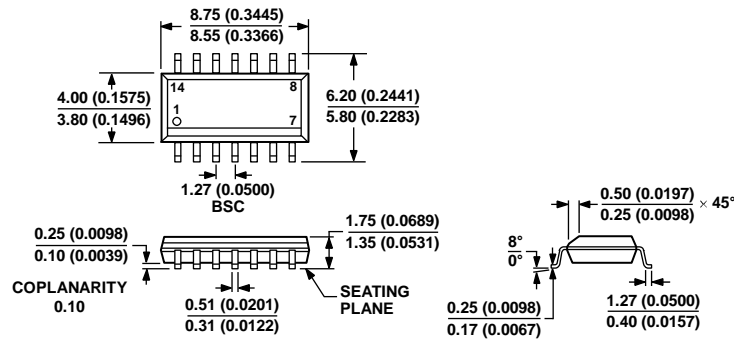


COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 36. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061908-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 37. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

061606-A

ORDERING GUIDE

| Model ^{1, 2} | Temperature Range | Package Description | Package Option | Branding |
|-----------------------|-------------------|---------------------|----------------|----------|
| AD8691AUJZ-R2 | -40°C to +125°C | 5-Lead TSOT | UJ-5 | ACA |
| AD8691AUJZ-REEL | -40°C to +125°C | 5-Lead TSOT | UJ-5 | ACA |
| AD8691AUJZ-REEL7 | -40°C to +125°C | 5-Lead TSOT | UJ-5 | ACA |
| AD8691AKSZ-R2 | -40°C to +125°C | 5-Lead SC70 | KS-5 | ACA |
| AD8691AKSZ-REEL | -40°C to +125°C | 5-Lead SC70 | KS-5 | ACA |
| AD8691AKSZ-REEL7 | -40°C to +125°C | 5-Lead SC70 | KS-5 | ACA |
| AD8691WAUJZ-R7 | -40°C to +125°C | 5-Lead TSOT | UJ-5 | ACA |
| AD8691WAUJZ-RL | -40°C to +125°C | 5-Lead TSOT | UJ-5 | ACA |
| AD8692ARMZ-R7 | -40°C to +125°C | 8-Lead MSOP | RM-8 | APA |
| AD8692ARMZ-REEL | -40°C to +125°C | 8-Lead MSOP | RM-8 | APA |
| AD8692ARZ | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8692ARZ-REEL | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8692ARZ-REEL7 | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8692WARMZ-REEL | -40°C to +125°C | 8-Lead MSOP | RM-8 | APA |
| AD8694ARUZ | -40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| AD8694ARUZ-REEL | -40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| AD8694WARUZ | -40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| AD8694WARUZ-REEL | -40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| AD8694ARZ | -40°C to +125°C | 14-Lead SOIC_N | R-14 | |
| AD8694ARZ-REEL | -40°C to +125°C | 14-Lead SOIC_N | R-14 | |
| AD8694ARZ-REEL7 | -40°C to +125°C | 14-Lead SOIC_N | R-14 | |
| AD8694WAC-P3 | -40°C to +125°C | Die | | |
| AD8694WAC-P7 | -40°C to +125°C | Die | | |

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The [AD8691W](#)/[AD8692W](#)/[AD8694W](#) models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

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