high performance needs great design.

Datasheet: AS5048A/AS5048B Magnetic Rotary Encoder

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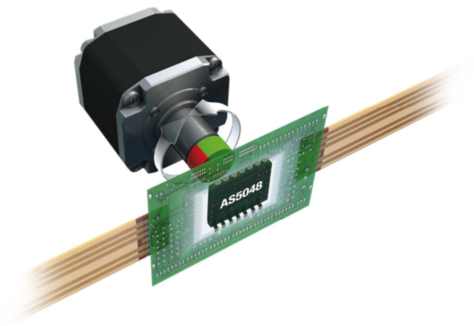
AS5048A/AS5048B

Datasheet

Magnetic Rotary Encoder

14-bit Angular Position Sensor



General Description

The AS5048 is an easy to use 360° angle position sensor with a 14-bit high resolution output. The maximum system accuracy is 0.05° assuming linearization and averaging is done by the external microcontroller.
The IC measures the absolute position of the magnet's rotation angle and consists of Hall sensors, analog digital converter and digital signal processing. The zero position can be programmed via SPI or I²C command. Therefore no programmer is needed anymore. This simplifies the assembly of the complete system because the zero position of the magnet does not need to be mechanically aligned. This helps developers to shorten their developing time. The sensor tolerates misalignment, air gap variations, temperature variations and as well external magnetic fields. This robustness and wide temperature range (-40°C up to +150°C) of the AS5048 makes the IC ideal for rotation angle sensing in harsh industrial and medical environments. Several AS5048 ICs can be connected in daisy chain for serial data read out. The absolute position information of the magnet is directly accessible over a PWM output and can be read out over a standard SPI or a high speed I²C interface. AS5048A has a SPI interface, AS5048B I2C interface. Both devices offer a PWM output. An internal voltage regulator allows the AS5048 to operate at either 3.3 V or 5 V supplies.

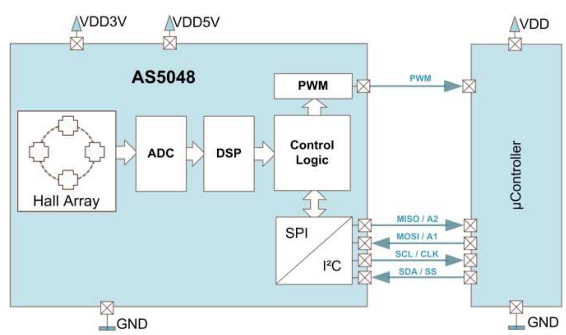
Key Features & Benefits

- 360° contactless angle position sensor
- Standard SPI or high speed I²C interface
- Pulse width modulated output (PWM)
- Simple programmable zero position via SPI or I²C command
- No programmer needed
- 14-bit full scale resolution
  0.0219°/LSB
- Angle accuracy 0.05°after system linearization and averaging
- Daisy chain capability
- Tolerant to air gap variations
  magnetic field input range: 30mT – 70mT
- -40°C to +150°C ambient temperature range
- 3.3V / 5V compliant
- 14-pin TSSOP package (5x6.4mm)

Applications

- Robotic joint position detection
- Industrial motor position control
- Medical robots and fitness equipment

Block Diagram



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1 Pin Configuration

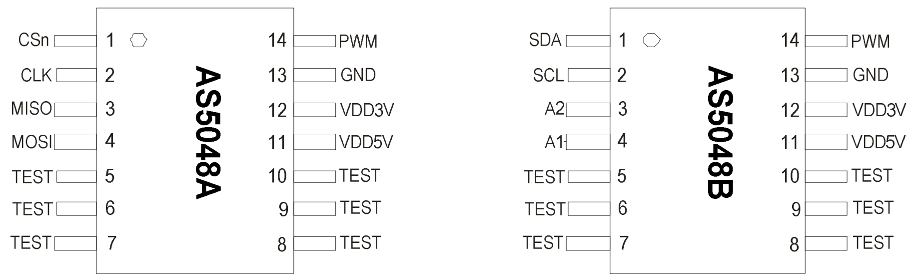


Figure 1: Pin configuration TSSOP14

1.1 Pin Description

Pin	AS5048A	Type	Description	AS5048B	Type	Description
1	CSn	DI_ST	SPI chip select - active low	SDA	DIO_OD	Data pin I2C interface
2	CLK	DI_ST	SPI clock input	SCL	DI_ST	I2C clock input
3	MISO	DIO_ST	SPI master in/slave out	A2	DI_ST	I2C address selection pin 3
4	MOSI	DI_ST	SPI master out/slave in	A1	DI_ST	I2C address selection pin 4
5	TEST	AIO	Test pin, see Note	Same as AS5048A		
6	TEST	AIO	Test pin, see Note			
7	TEST	AIO	Test pin, see Note			
8	TEST	AIO	Test pin, see Note			
9	TEST	AIO	Test pin, see Note			
10	TEST	AIO	Test pin, see Note			
11	VDD5V	S	Positive Supply Voltage, 3.0 to 5.5 V			
12	VDD3V	S	3.3V Regulator output; internally regulated from VDD. Connect to VDD for 3V supply voltage. 10µF capacitor to GND required in 5V operation mode			
13	GND	S	Negative Supply Voltage (GND)			
14	PWM	DO	Pulse Width Modulation output			

Table 1: Pin description TSSOP14

PIN Types:			
	S	...	supply pad
	AIO	...	analog I/O
	DI_ST	...	digital input with schmitt trigger
	DO	...	digital output – push-pull
	DIO _ST	...	digital I/O with schmitt trigger in the input path
	DIO _OD	...	digital I/O with open drain output

Note: Pin 5, 6, 7, 8, 9, 10 should be grounded to GND.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage at VDD pin	VDD5V	-0.3	7	V	
DC voltage at VDD3V pin	VDD3V	-0.3	5	V	
DC voltage at GND pin	GND	-0.3	0.3	V	
Input pin voltage	V_in		VDD+0.3	V	
Input current (latchup immunity)	I_scr	-100	100	mA	Norm: Jedec 78
Electrostatic discharge	ESD		+/-2	kV	Norm: MIL 883 E method 3015
Total power dissipation (all supplies and outputs)	P_t		150	mW	
Storage temperature	T_strg	-55	150	°C	
Package body temperature	T_body		260	°C	The reflow peak soldering temperature (body temperature)specified is in accordance with IPC/JEDEC J-STD-020 “Moisture Solid State Surface Mount Devices”. The lead finish from Pb-free leaded packages is matte tin (100% Sn)
Humidity non-condensing	H	5	85	%	
Moisture Sensitive Level	MSL	3			Represents a maximum floor life time of 168h

Table 2 Absolute Maximum Ratings

2.2 Operating Conditions

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Parameter	Symbol	Min	Max	Unit	Note
Positive supply voltage	VDD5V	4.5	5.5	V	5V Operation via LDO
	VDD3V	3	3.6	V	LDO output voltage
Positive core supply voltage	VDDCORE	3	3.6	V	
Negative supply voltage	GND	0	0	V	
Ambient temperature	T_amb	-40	150	°C	Only for 5V operation. T_amb_max for 3V is 125°C
Supply Current	I_sup		15	mA	

Table 3: Operating Condition

2.3 DC/AC Characteristics for digital inputs and outputs

Parameter	Symbol	Min	Typ	Max	Unit	Note
CMOS digital input with schmitt trigger: CSn, CLK, MOSI						
High level input voltage	V_IH	0.7 * VDD5V			V	
Low level input voltage	V_IL			0.3 * VDD5V	V	
Input leakage current	I_LEAK			1	µA	
CMOS output: PWM, MISO						
High level output voltage	V_OH	VDD5V-0.5			V	
Low level output voltage	V_OL			GND+0.4	V	
Capacitive load	C_L			50	pF	
Output current	I_OUT			4	mA	

Table 4:DC/AC characteristics

2.4 Electrical System Specifications

VDD5V = 5V, $T_{Ambient}$ = -40 to +150°C unless noted otherwise

Parameter	Symbol	Min	Typ	Max	Unit	Note
Magnetic input field	Bz	30	50	70	mT	
Output sampling rate	f_{sample}	10.2	11.25	12.4	kHz	
Output Resolution	RES		14		Bit	
Sensor output noise	Noise			0.06	Deg	2.73LSB@14bit, rms value
System propagation delay	t_{prop}	90.7	100	110.2	µs	
PWM frequency	f_{PWM}	0.907	1	1.102	kHz	
Non-linearity optimum placement of magnet	INL_{OPT}			±0.4	Deg	Assuming 8 mm diameter of magnet
Non-linearity @displacement of magnet	INL_{DIS}			±0.7	Deg	Assuming 8 mm diameter of magnet and 500 um displacement in x and y
Non-linearity @displacement of magnet and temperature -40 -150 degC	$INL_{DIS+TEMP}$			±1.2	Deg	Assuming 8 mm diameter of magnet and 500 um displacement in x and y
Startup Time	$t_{startup}$			10	ms	

Table 5 System specification

2.5 Global Timing Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Internal Master Clock	F_{OSC}	4.05	4.5	4.95	MHz	±10%
	T_{OSC}		$1/F_{OSC}$		Hz	

Table 6 Global timing conditions

3 Functional Description

The AS5048 is a magnetic Hall sensor system manufactured in a CMOS process. A lateral Hall sensor array is used to measure the magnetic field components perpendicular to the surface of the chip. The AS5048 is uses self-calibration methods to eliminate signal offset and sensitivity drifts.

The integrated Hall sensors are placed around the center of the device and deliver a voltage representation of the magnetic flux Bz.

Through Sigma-Delta Analog-to-Digital Converter (ADC) and Digital Signal-Processing (DSP) algorithms, the AS5048 provides accurate high-resolution absolute angular position information. This is accomplished by a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs that indicate movements of the magnet towards or away from the device's surface, in the z-axis.

A small diametrically magnetized (two-pole) standard magnet provides the angular position information. Depending on the system requirements different magnet diameters are possible. Additional flexibility is given by the wide range of the magnetic input range. The AS5048 can be combined with NeFeB, SmCo and alternative magnet materials e.g. hard ferrites. The AS5048 provides a 14-bit binary code representing the angular position of the magnet. The type of output is pre-programmed as SPI version A or I2C version B. Simultaneously a PWM output signal is available in 12 bit format.

A simple programming of the zero position is possible over the interface. No additional programmer is needed. The AS5048 uses one time programmable (OTP) fuses for permanent programming of the user settings. The verification is possible over a simple digital readout of the OTP content.

4 Operation

4.1 Supply Voltage Configuration

The AS5048 operates at 5V ±10%, using an internal Low-Dropout (LDO) voltage regulator. In addition a 3.3V operation is possible. The **VDD3V** output is intended for internal use only. **It must not be loaded with an external load.**

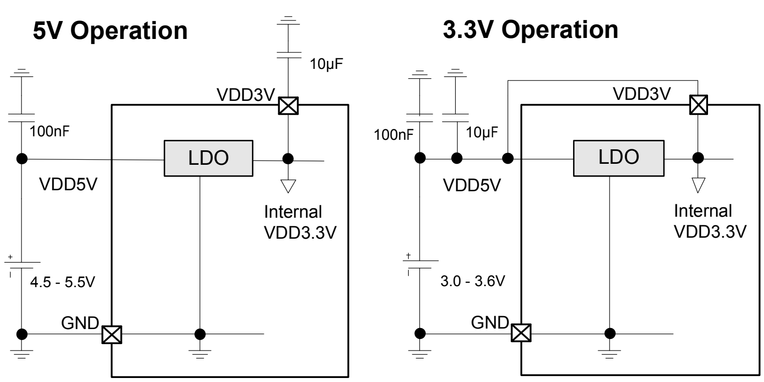


Figure 2: Connections for 5V and 3.3V supply voltages

Note: The pin **VDD3V** must always be buffered by a 10 µF capacitor in 5V operation. It must not be left floating, as this may cause unstable internal supply voltages which may lead to larger output jitter of the measured angle.

In 3V operation the **VDD3V** must be shorted to **VDD5V.** The ambient temperature Tamb is limited to 125 degC in this mode.

4.2 SPI Interface

The 16 bit SPI Interface enables read / write access to the register blocks and is compatible to a standard micro controller interface. The SPI is active as soon as **CSn** is pulled low. The AS5048A then reads the digital value on the **MOSI**(master out slave in) input with every falling edge of **CLK** and writes on its **MISO** (master in slave out) output with the rising edge. After 16 clock cycles **CSn** has to be set back to a high status in order to reset some parts of the interface core.

4.2.1 SPI Interface Signals (4-Wire Mode, Wire_mode = 1)

The AS5048A only supports slave operation mode. Therefore **CLK** for the communication as well as the **CSn** signal has to be provided by the test equipment. The following picture shows a basic interconnection diagram with one master and an AS5048A device and a principle schematic of the interface core.

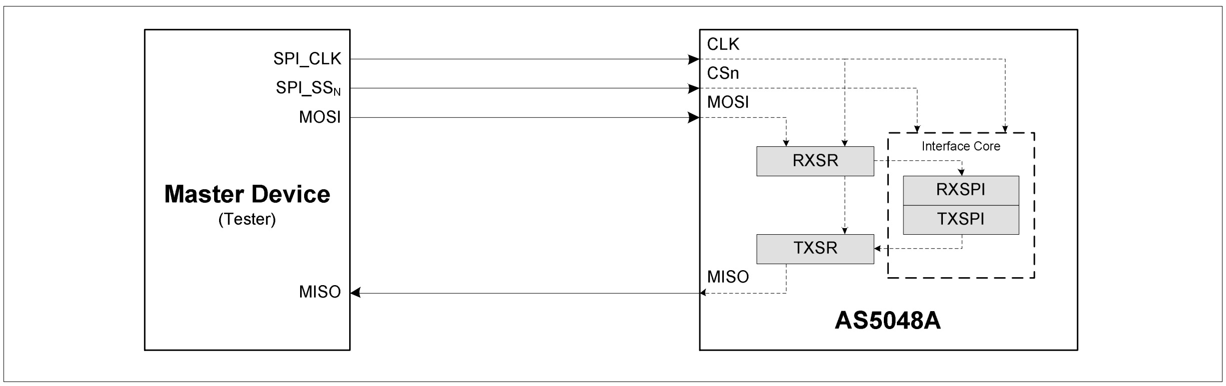


Figure 3 SPI Connection AS5048A with uC

Because the interface has to decode the sent command before it can react and provide data the response of the chip to a specific command applied at a time T can be accessed in the next transmission cycle ending at T + TCOM.
The data are sent and read with **MSB first**. Every time the chip is accessed it is sending and receiving data.

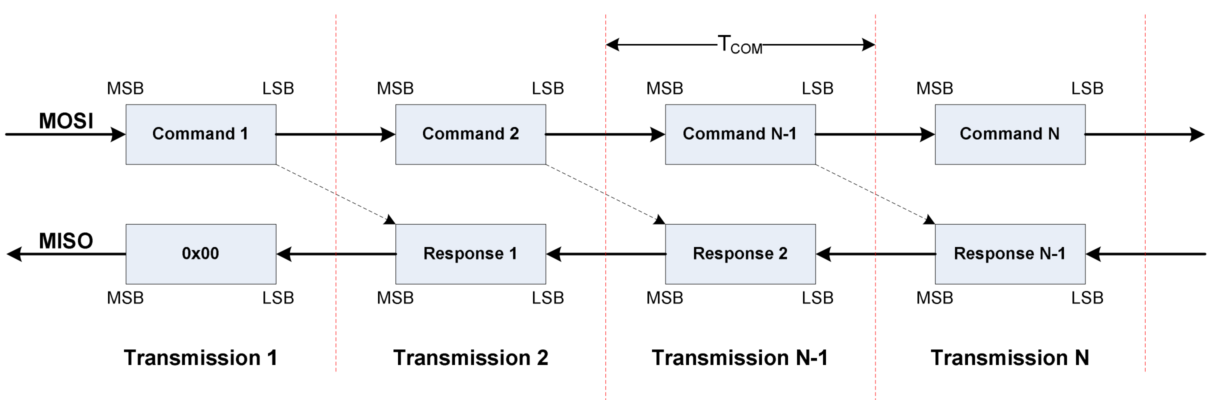


Figure 4 SPI Command/Response Data Flow

4.2.2 SPI Timing

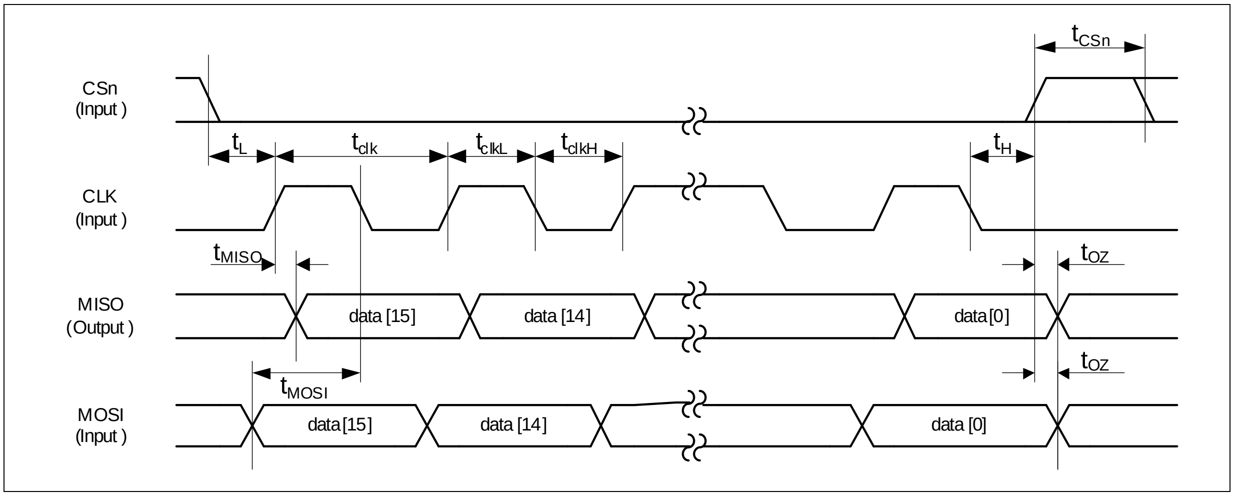


Figure 5 SPI Timing Diagram

Parameter	Description	Min	Max	Unit
t_L	Time between CSn falling edge and CLK rising edge	10 (2)		ns
t_L	Time between CSn falling edge and CLK rising edge	350 (1)		ns
T_{CLK}	Serial clock period	100		ns
t_{CLKL}	Low period of serial clock	50		ns
t_{CLKH}	High period of serial clock	50		ns
t_H	Time between last falling edge of CLK and rising edge of CSn	t_{CLK} / 2		ns
T_{CSnH}	High time of CSn between two transmissions	10 (2)		ns
T_{CSnH}	High time of CSn between two transmissions	350 (1)		ns
t_{MOSI}	Data input valid to clock edge	20		ns
t_{MISO}	CLK edge to data output valid		20	ns

Table 7 SPI Timing Characteristics

Notes:

(1) Synchronization with the internal clock → 2 * $t_{CLK\_SYS} + 10\text{ ns}$ (e.g. at 8 MHz → 253 ns)

(2) No synchronization needed because the internal clock is inactive

4.2.3 SPI Connection to the Host UC

Single Slave Mode

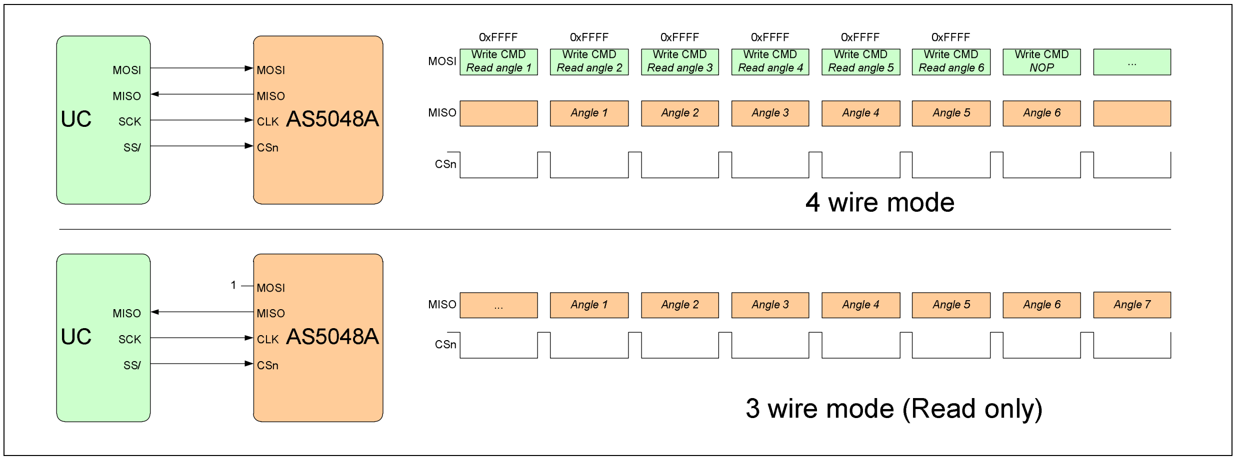


Figure 6 Single Slave Mode

3 Wire Mode (read only):

Multiple Slave, n+3 Wire (Separate ChipSelect)

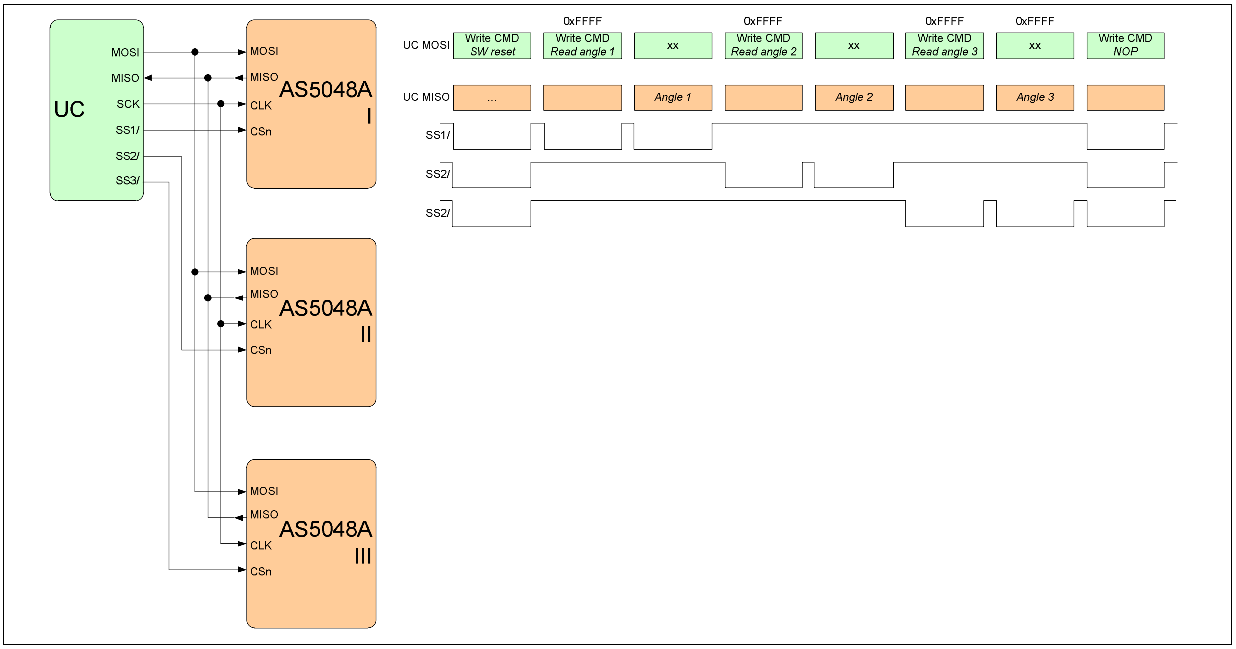


Figure 7 Multiple Slave, n+3 Wire (Separate ChipSelect)

Daisy Chain, 4 Wire

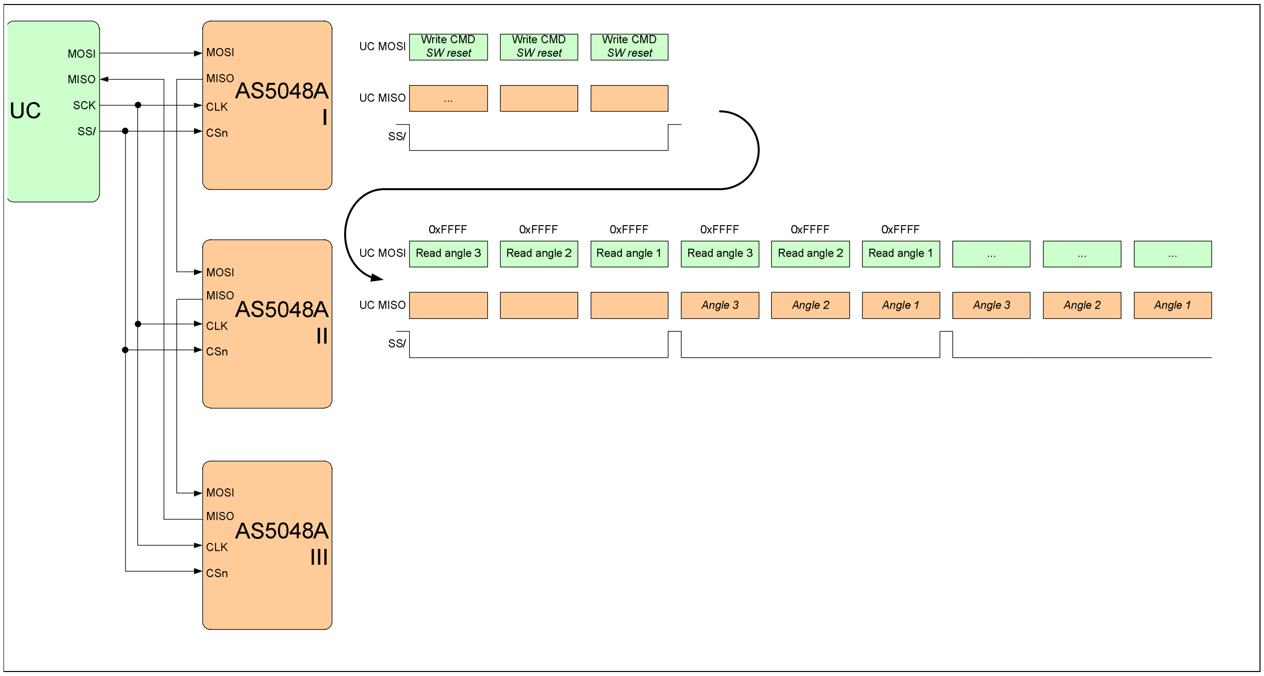


Figure 8 Daisy Chain, 4 Wire

4.2.4 SPI Communication Command Package

Every command sent to the AS5048A is represented with the following layout.

Command Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	RWn	Address<13:0>													
Bit Definition & Description																
PAR	Parity bit (EVEN)															
RWn	Indicates read(1) or write(0) command															
Address	14 bit address code															

Table 8 SPI Command Package

4.2.5 Read Package (Value Read from AS5048A)

The read frame always contains two alarm bits, the parity and error flags and the addressed data of the previous read command.

Read Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	EF	Data<13:0>													
Bit Definition & Description																
PAR			Parity bit (EVEN)													
EF			Error flag indicating a transmission error in a previous host transmission													
Data			14 bit addressed data													

Table 9 SPI read package

4.2.6 Write Data Package (Value Written to AS5048A)

The write frame is compatible to the read frame and contains two additional bits, parity flag and R flag.

If the previous command was a write command a second package has to be transmitted.

Data Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	R	Data <13:0>													
Bit Definition & Description																
PAR			Parity bit (EVEN)													
R			Has to be 0													
Data			14 bit data to write to former selected address													

Table 10 SPI write data package

4.2.7 Register Map SPI

	Address hex	Name	Access Type	Bit Nr.	Symbol	Default	Description
Control and Error Registers	x0000	SPI NOP	R	13	NOP	0	No operation dummy information
				:			
				0			
	x0001	Clear Error Flag	R	13	not used	n.a.	Error Register. All errors are cleared by access
				:			
				3			
				2	Parity Error	0	
				1	Command Invalid		
				0	Framing Error		
	x0003	Programming Control	R/W	13	not used	0	Programming control register. Programming must be enabled before burning the fuse(s). After programming is a verification mandatory. See programming procedure.
				:			
				7			
				6	Verify		
				5	not used		
				4			
				3	Burn		
				2	reserved		
				1			
				0	Programming Enable		
Programmable Customer settings	x0016	OTP Register Zero Position Hi	R/W + Program	13	not used	0	Zero Position value high byte
				:			
				8			
				7	Zero Position <13>	0	
				:	:	:	
				0	Zero Position <6>	0	
	x0017	OTP Register Zero Position Low 6 LSBs	R/W + Program	13	not used	0	Zero Position remaining 6 lower LSB's
				:			
				6			
				5	Zero Position <5>	0	
				:	:	:	
				0	Zero Position <0>	0	
Readout Registers	x3FFD	Diagnostics + Automatic Gain Control (AGC)	R	13	not used	n.a.	Diagnostics flags
				12			
				11	Comp High	0	
				10	Comp Low	0	
				9	COF	0	
				8	OCF	1	
				7	AGC value<7>	1	Automatic Gain Control value. 0 decimal represents high magnetic field 255 decimal represents low magnetic field
				:	:	:	
				0	AGC value<0>	0	
	x3FFE	Magnitude	R	13	Magnitude<13>	0	Magnitude information after ATAN calculation
				:	:	:	
				0	Magnitude<0>	0	
	x3FFF	Angle	R	13	Angle <13>	0	Angle information after ATAN calculation and zero position adder
				:	:	:	
				0	Angle<0>	0	

Table 11 SPI register map

4.2.8 SPI Interface Commands

READ Command

For a single *READ* command two transmission sequences are necessary. The first package written to the AS5048 contains the *READ* command **(MSB-1 high)** and the address the chip has to access, the second package transmitted to the AS5048 device can be *any command* the chip has to process next. The content of the desired register is available in the *MISO* register of the *master device* at the end of the second transmission cycle.

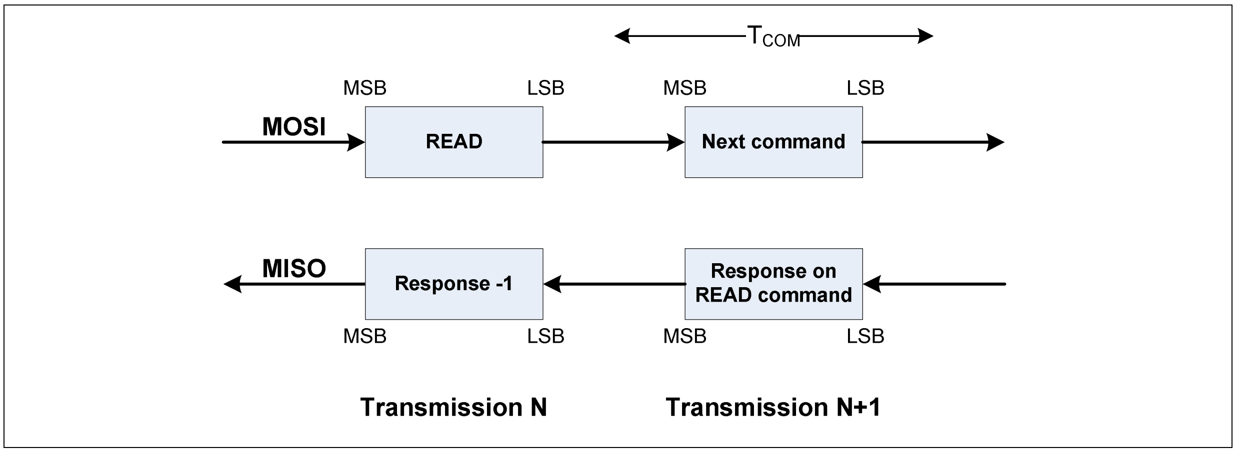


Figure 9 READ Command

WRITE Command

A single *WRITE* command takes two transmission cycles. With a NOP command after the WRITE command you can verify the sent data with three transmission cycles because the data will be send back during the following command.

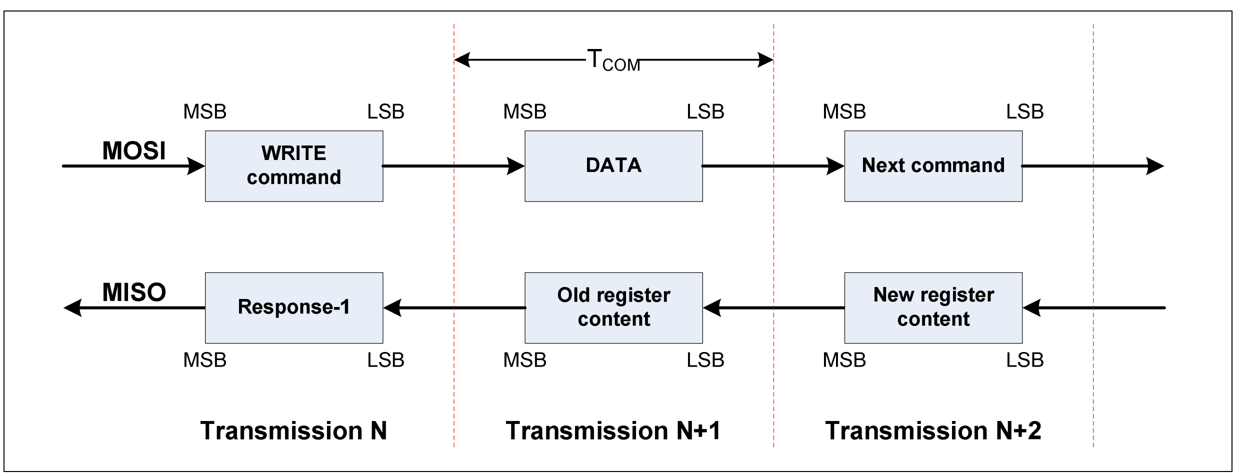


Figure 10 WRITE Command

CLEAR ERROR FLAG Command

The *CLEAR ERROR FLAG* command is implemented as *READ* command. This command clears the *ERROR FLAG* which is contained in every *READ* frame. Before the *ERROR FLAG* is cleared the error register content comes back with the information which error type was occurred. On the next new *READ* register the *ERROR FLAG* is cleared

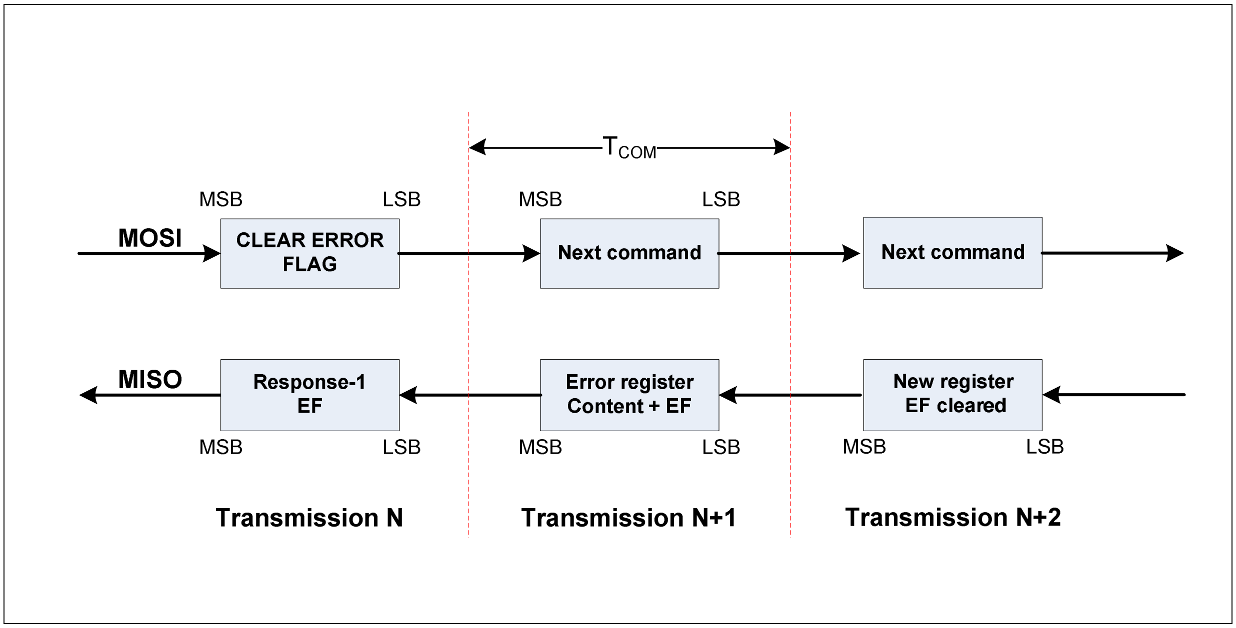


Figure 11 CLEAR ERROR FLAG Command

The package necessary to perform a *CLEAR ERROR FLAG* is built up as follows.

CLEAR ERROR FLAG Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 12 Clear Error Flag Command

Possible conditions which force the ERROR FLAG to be set:

- wrong parity
- wrong number of clocks (no full transmission cycle or too many clocks)

Note: If the error flag is set to high because of a communication problem the flag remains set until it will be cleared by the *CLERAR ERROR FLAG* command.

NOP Command

The *NOP* command represents a dummy write to the AS5048.

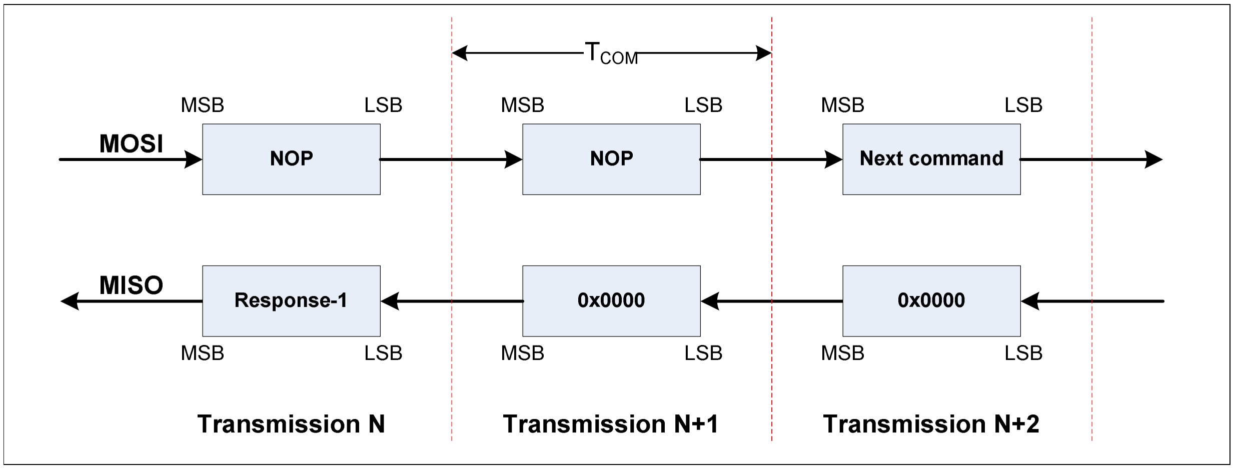


Figure 12 NOP Command

The NOP command frame looks like follows.

NOP Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 13 NOP Command

The chip's response on this command is 0x0000 – if no error happens.

4.3 I²C interface

The AS5048B supports 2-wire high-speed I²C protocol in device mode. The host MCU (master) has to initiate the data transfers. The 7-bit device address of the slave depends on the state of the OTP I2C register 21 (0x15) bit 0...4 + 2 I2C address selection pin 3 and 4.

Supported modes:

- Random/Sequential Read
- Byte/Page Write
- Standard : 0 to 100kHz clock frequency (slave mode)
- Fast Mode : 0 to 400kHz clock frequency (slave mode)
- High Speed: 0 to 3.4MHz clock frequency (slave mode)

The SDA signal is bidirectional and is used to read and write the serial data. The SCL signal is the clock generated by the host MCU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 3.4MHz, data are triggered on the rising edge of SCL.

4.3.1 I²C Electrical Specification

			FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{IL}	LOW-Level Input Voltage		-0.5	0.3V_{DD}	-0.5	0.3VDD	-0.5	0.3V_{DD}	V
V_{IH}	HIGH-Level Input Voltage		0.7V_{DD}	V_{DD} + 0.5 (1)	0.7V_{DD}	VDD + 0.5 (1)	0.7VDD	V_{DD} + 0.5 (1)	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs	V_{DD}< 2V	0.1V_{DD}	--	0.1V_{DD}	--	0.1VDD	--	V
V_{OL}	LOW-Level Output Voltage (open-drain or open-collector) at 3mA Sink Current	V_{DD} < 2V	--	0.2V_{DD}	--	0.2VDD	--	0.2V_{DD}	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4V	20		--	--	--	--	mA
I_{CS}	Pull-up current of SCLH current source		--	--	3	12	3	12	mA
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		--	50 (2)	--	10	--	10	ns
I_i	Input Current at each I/O Pin	Input Voltage between	-10	+10 (3)	--	10	--	10	µA
C_B	Total Capacitive Load for each Bus Line		--	550	--	100	--	400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)		--	10	--	10	--	10	pF

Table 14 I²C Electical Specification

(1) Maximum V_{IH} = V_{DDmax} +0.5V or 5.5V
(2) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
(3) I/O pins of Fast-mode and Fast-mode Plus devices must not obstruct the SDA and SCL lines if VDD is switched off.

4.3.2 I²C Timing

			FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF (5)		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{SCLK}	SCL clock Frequency		--	1000	--	3400	--	1700	kHz
t_{BUF}	Bus Free Time; time between STOP and START Condition		500	--	500	--	500	--	ns
$t_{HD;STA}$	Hold Time; (Repeated) START Condition (1)		260	--	160	--	160	--	ns
t_{LOW}	LOW Period of SCL Clock		500	--	160	--	320	--	ns
t_{HIGH}	HIGH Period of SCL Clock		260	--	60	--	120	--	ns
$t_{SU;STA}$	Setup Time for a Repeated START condition		260	--	160	--	160	--	ns
$t_{HD;DAT}$	Data Hold Time (2)		0	450	0	70	0	150	ns
$t_{SU;DAT}$	Data Setup Time (3)		50	--	10	--	10	--	ns
t_R	Rise Time of SDA and SCL Signals		20+0.1 C_b	120	--	--	--	--	ns
t_F	Fall time of SDA and SCL signals		20+0.1 C_b	120 (4)	--	--	--	--	ns
t_{rCL}	Rise time of SCLH signal	Ext. pull-up source of 3mA	--	--	10	40	20	80	ns
t_{rCL1}	Rise time of SCLH signal after repeated START condition and after an acknowledge bit	Ext. pull-up source of 3mA	--	--	10	80	20	160	ns
t_{fCL}	Output rise time of SCLH signal	Ext. pull-up source of 3mA	--	--	10	40	20	80	ns
t_{rDA}	Output rise time of SDAH signal		--	--	10	80	20	160	ns
t_{fDA}	Output rise time of SDAH signal		--	--	10	80	20	160	ns
$t_{SU;STO}$	Setup Time for STOP Condition		260	--	160	--	160	--	ns
V_{nL}	Noise margin at LOW level		0.1V_{DDp}	--	0.1V_{DDp}	--	0.1V_{DDp}	--	V
V_{nH}	Noise margin at HIGH level		0.2V_{DDp}	--	0.2V_{DDp}	--	0.2V_{DDp}	--	V

Table 15 I²C Timing

(1) after this time the first clock is generated
(2) A device must internally provide a minimum hold time (120ns / max 250ns for Fast-mode Plus, 80ns / max 150ns for High-speed mode) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
(3) A fast-mode device can be used in standard-mode system, but the requirement $t_{SU;DAT}$ = 250ns must then e met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does strech the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{Rmax} + $T_{SU;DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
(4) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing
(5) For capacitive bus loads between 100pF and 400pF, the timing parameters must be linearly interpolated

4.3.3 Register Table

The following registers / functions are accessible over the serial I^{2}C interface.

	Address dec	Name	Access Type	Bit Nr.	Symbol	Default	Description
Control OTP	3	Programming Control	R/W	7	not used	0	Programming control register. Programming must be enabled before burning the fuse(s). After programming is an verification mandatory. See programming procedure.
				6	Verify		
				5	not used		
				4			
				3	Burn		
				2	reserved		
				1			
				0	Programming Enable		
Programmable Customer settings	21	I^{2}C slave address	R/W + Program	7	not used	n.a.	I^{2}C slave address slave address consist of 5 programable bits (MSBs) and the hardware setting of Pins A1 and A2 I^{2}C address <4> is by default not programmed and due to the inversion defined as '1'
				:			
				5			
				4	I^{2}C address<4>	internally inverted	
				:	:	:	
				0	I^{2}C address<0>	0	
	22	OTP Register Zero Position Hi	R/W + Program	7	Zero Position <13>	0	Zero Position value high byte
				:	:	:	
				0	Zero Position <6>	0	
	23	OTP Register Zero Position Low 6 LSBs	R/W + Program	7	not used	n.a.	Zero Position remaining 6 lower LSB's
				6			
				5	Zero Position <5>	0	
				:	:	:	
				0	Zero Position <0>	0	
Readout Registers	250	Automatic Gain Control	R	7	AGC value<7>	1	Automatic Gain Control value. 0 decimal represents high magnetic field 255 decimal represents low magnetic field
				:	:	:	
				0	AGC value<0>	0	
	251	Diagnostics	R	7	not used	n.a.	Diagnostic flags
				:			
				4			
				3	Comp High	0	
				2	Comp Low	0	
				1	COF	0	
				0	OCF	1	
	252	Magnitude	R	7	Magnitude<13>	0	Magnitude information afer ATAN calculation
				:	:	:	
				0	Magnitude<6>	0	
	253		R	7	not used	n.a.	
				6			
				5	Magnitude<5>	0	
				:	:	:	
				0	Magnitude<0>	0	
	254	Angle	R	7	Angle<13>	0	Angle Value afer ATAN calculation and zero position adder
				:	:	:	
				0	Angle<6>	0	
	255		R	7	not used	n.a.	
				6			
				5	Angle<5>	0	
				:	:	:	
				0	Angle<0>	0	

Table 16 Register Map I2C

4.3.4 I²C Slave address

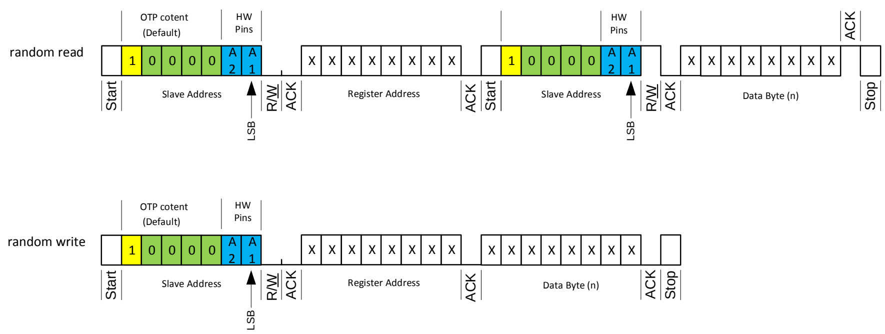


Figure 13 Slave address construction

The slave address consists of the hardware setting on pins A1, A2 and upper MSBs programmable by the user. The MSB of the slave address (yellow) is internally inverted. This means that by default the resulting data is '1'. A read of the I²C slave address register 21 will return a '0' at the MSB.

4.4 PWM interface

The AS5048 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. The PWM frequency is internally trimmed to an accuracy of ±10% over full temperature range. This tolerance can be cancelled by measuring the complete duty cycle.

The PWM signal consists of different sections:

- Init:
  12 clocks -> PWM = 'high'
- Error_n:
  4 clocks -> PWM = 'not(system_error)'
- Data:
  4095 clocks -> PWM = 'angle_zero' / 'low' (in case of error)
- Exit:
  8 clocks -> PWM = 'low'

In case of an error the data section is set to zero.

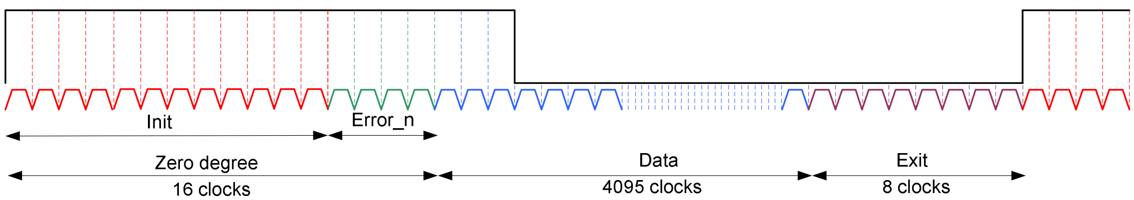


Figure 14 PWM Format

Parameter	Symbol	Value	Unit
PWM – Period	T_PWM	4119	T_PWM_BIT
PWM – Bit Time	T_PWM_BIT	1	T_OSC
PWM Resolution	N_PWM	4096	bit

Table 17 PWM Period and resolution

5 Package Drawings and Markings

Package type: TSSOP14

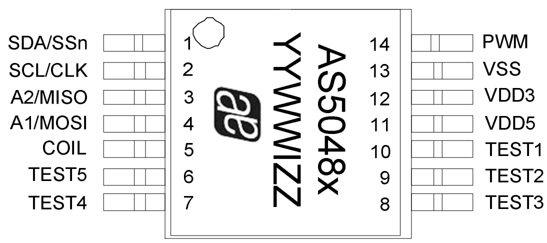


Figure 15 Package Marking

5.1.1 Assembly Lot Code

The assembly lot code for standard "**YYWWIZZ**" is composed as follows:

X **-** Interface type: A=SPI / B=I²C

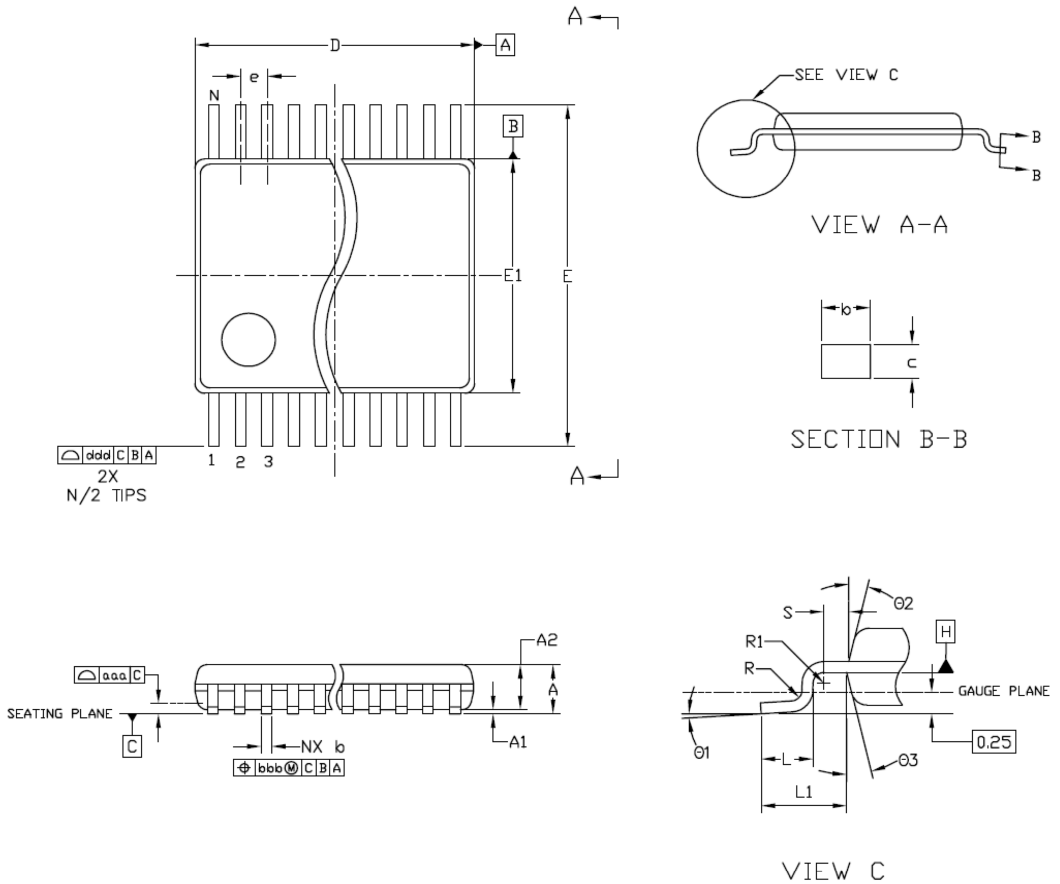
YY - Year

WW - Week

I - Plant identification letter

ZZ - Letters for free traceability

14-Lead Thin Shrink Small Outline Package TSSOP-14



REF.	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E	–	6.40 BSC	–
E1	4.30	4.40	4.50
e	–	0.65 BSC	–
L	0.45	0.60	0.75
L1	–	1.00 REF	–
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
Θ1	0°	–	8°
Θ2	–	12 REF	–
Θ3	–	12 REF	–
aaa	–	0.10	–
bbb	–	0.10	–
ccc	–	0.05	–
ddd	–	0.20	–
N		14	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.

6 Application Information

6.1 Programming of the AS5048

6.1.1 Programming of the zero position

The absolute angle position can be permanent programmed over the interface. This could be useful for random placement of the magnet on the rotation axis. A readout at the mechanical zero position can be performed and written back into the IC. With permanent programming the position is non-reversible stored in the IC. This programming can be performed only once.

To simplify the calculation of the zero position it is only needed to write the value in the IC which was read out before from the angle register.

6.1.2 Programming sequence with verification

To program the zero position is needed to perform following sequence:

1. Read angle information
2. Set the Programming Enable bit in the OTP control register
3. Write previous read angle position into OTP zero position register
4. Read back for verification the zero position register data
5. Set the Burn bit to start the automatic programming procedure
6. Read angle information (equals to 0)
7. Set the Verify bit to load the OTP data again into the internal registers with modified threshold comparator levels
8. Read angle information (equals to 0)

The programming can either be performed in 5V operation using the internal LDO, or in 3V operation but using a minimum supply voltage of 3.3V. In case of 3V operation, also a 10uF capacitor is required on the VDD3 pin.

6.2 Diagnostic functions of the AS5048

The AS5048 provides diagnostics functions of the IC and also diagnostic functions of the magnetic input field

Following diagnostic flags are available:

See Table 11 register address x3FFD (AS5048A) or Table 16 register address 251 dec (AS5048B)

OCF (**O**ffset **C**ompensation **F**inished), logic high indicates the finished Offset Compensation Algorithm. After power up the flag remains always to logic high.

COF (**C**ordic **O**ver**f**low), logic high indicates an out of range error in the CORDIC part. When this bit is set, the angle and magnitude data is invalid. The absolute output maintains the last valid angular value.

COMP low, indicates a weak magnetic field. It is recommended to monitor in addition the magnitude value.

COMP high, indicated a high magnetic field. It is recommended to monitor the magnitude value.

6.3 Choosing the Proper Magnet

The AS5048 works with a variety of different magnets in size and shape. A typical magnet could be 6-8 mm in diameter and ≥2.5mm in height The magnetic field strength perpendicular to the die surface has to be in the range of ±30mT…±70mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic flux B_Z at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±30mT…±70mT.

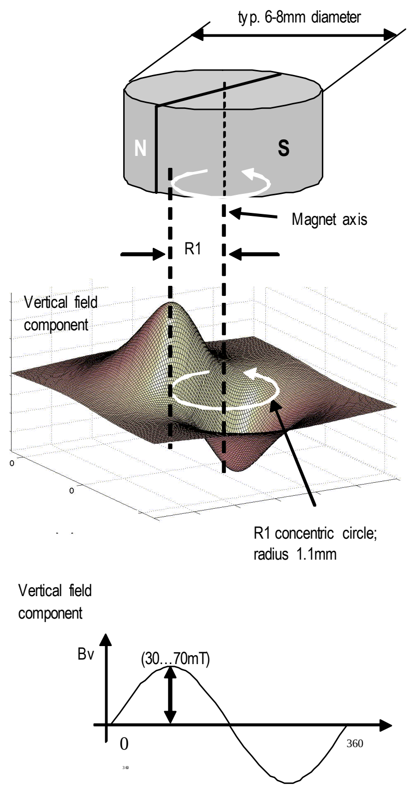


Figure 16: Typical magnet and magnetic flux distribution

6.4 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below:

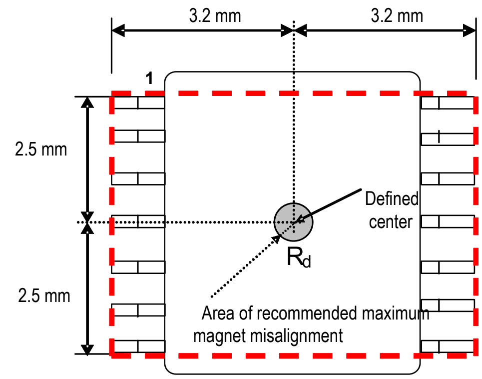


Figure 17: Defined chip center and magnet displacement radius

6.5 Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25 mm (larger magnets allow more displacement e.g. 0.5 mm) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits The typical distance "z" between the magnet and the package surface is 0.5mm to 2.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by indication flags.

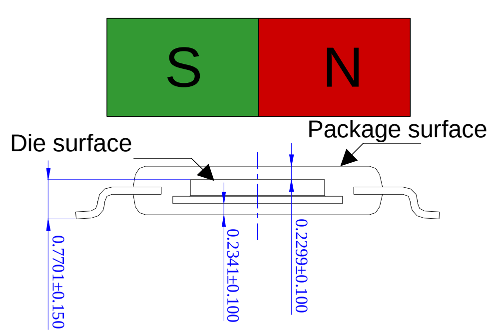


Figure 18: Vertical placement of the magnet

7 Ordering Information

Model	Description	Delivery Form	Package
AS5048A-HTSP	14 –Bit Programmable Magnetic Rotary Encoder with SPI-Interface	Tape&Reel	TSSOP 14
AS5048B-HTSP	14 –Bit Programmable Magnetic Rotary Encoder with I2C-Interface	Tape&Reel	TSSOP 14

Table 18: Ordering Information

8 Revision History

Revision	Date	Owner	Description
1.0	10-April-2012	mub	Initial revision
1.1	16-April-2012	mub	Minor correction text
1.2	09-May-2012	mub	Default pin configuration added. Minor text corrections
1.3	20-June-2012	mub	I2C Slave address explanation. Minor corrections.

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