Bias Voltage and Current Sense Circuits for Avalanche Photodiodes

Feeding and Reading the APD

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INTRODUCTION

Avalanche photodiodes (APDs) are widely utilized in laser based fiberoptic systems to convert optical data into electrical form. The APD is usually packaged with a signal conditioning amplifier in a small module. An APD receiver module and attendant circuitry appears in Figure 1. The APD module (figure right) contains the APD and a transimpedance (e.g., current-to-voltage) amplifier. An optical port permits interfacing fiberoptic cable to the APD's photosensitive portion. The module's compact construction facilitates a direct, low loss connection between the APD and the amplifier, necessary because of the extremely high speed data rates involved.

The receiver module needs support circuitry. The APD requires a relatively high voltage bias (figure left) to operate, typically 20V to 90V. This voltage is set by the bias supply's programming port. This programming voltage may also include corrections for the APD's temperature dependent response. Additionally, it is desirable to monitor the APD's average current (figure center), which indicates optical signal strength. This information can be combined with feedback techniques to maintain optical signal strength at an optimal level. The feedback loop's operating characteristics can also determine if deleterious degradation of optical components has occurred, permitting corrective measures to be taken. APD current is typically between 100nA and 1mA, a dynamic range of 10,000:1. This measurement, which should be taken with an accuracy inside 1%, normally must occur in the APD's "high side," complicating circuit design. This restriction applies because the APD's anode is committed to the receiver amplifier's summing point.

The APD module, an expensive and electrically delicate device, must be protected from damage under all conditions. The support circuitry must never produce spurious outputs which could destroy the APD module. Particular attention must be devoted to the bias supply's dynamic response under programming and power-up/down conditions. Finally, it is desirable to power the support circuitry from a single 5V rail.

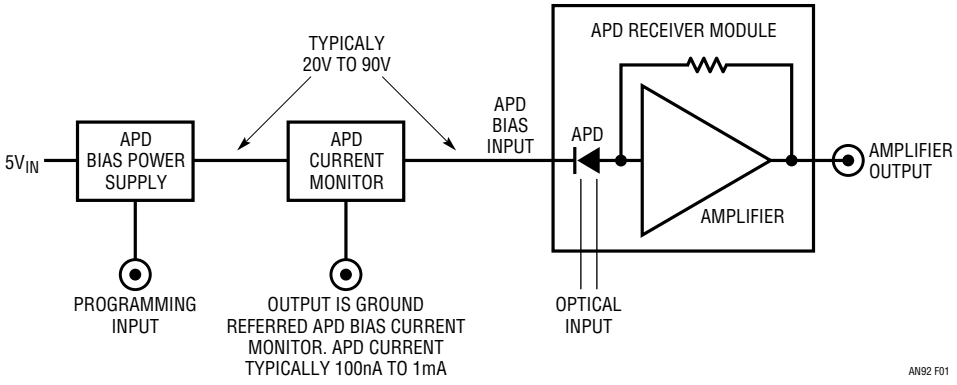


Figure 1. Avalanche Photodiode (APD) Module (Figure Right) Contains APD, Amplifier and Optical Port. Power Supply (Figure Left) Provides APD Bias Voltage. APD Current Monitor (Figure Center) Operates at High Common Mode Voltage, Complicating Signal Conditioning

The bias voltage and current measurement requirements described above constitute a significant design challenge and are addressed in the following text.

Simple Current Monitor Circuits (with Problems)

Figure 2's straightforward approaches attempt to address the current monitor problem. Figure 2a uses an instrumentation amplifier powered by a separate 35V rail to measure across the 1kΩ current shunt. Figure 2b is similar but derives its power supply from the APD bias line. Although both approaches function, they do not meet APD current sensing requirements. APD bias voltages can range to 90V, exceeding the amplifier's supply and common mode voltage limits. Additionally, the measurement's wide dynamic range requires the single rail powered amplifier to swing within 100μV of zero, which is impractical. Finally, it is desirable for the amplifiers to operate from a single, low voltage rail.

Figure 3's circuit divides down the high common mode current shunt voltage, theoretically permitting the 5V powered amplifier to extract the current measurement over a 20V to 90V APD bias range. In practice, this arrangement introduces prohibitive errors, primarily because the desired signal is also divided down. The current measurement information is buried in the divider resistor's tolerance, even with 0.01% components. The desired 1% accuracy over a 100mA to 1nA range cannot be achieved. Finally, although the amplifier operates from a single 5V supply, it cannot swing all the way to zero.

It is clear from the preceding circuits that common circuit approaches will not meet APD signal conditioning requirements. More sophisticated techniques are necessary.

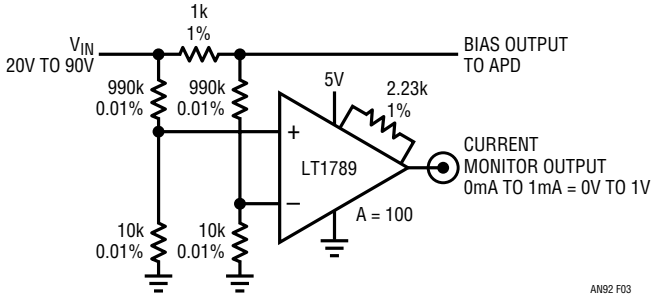
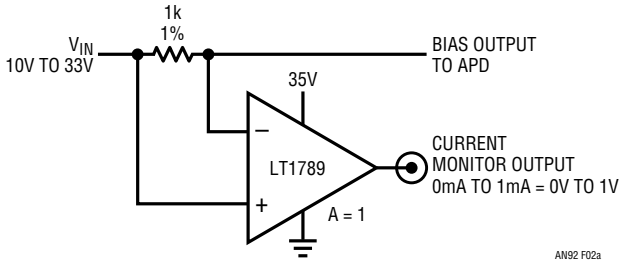


Figure 3. Dividing Down High Common Mode Voltage Introduces Huge Errors, Even with Precision Components. Desired 1% Accuracy Over 100nA to 1mA Current Monitor Range Is Buried by Resistor Mismatch, Even with 0.01% Resistors. Single Rail Powered Amplfier Cannot Swing Close Enough to Zero. Approach Is Impractical

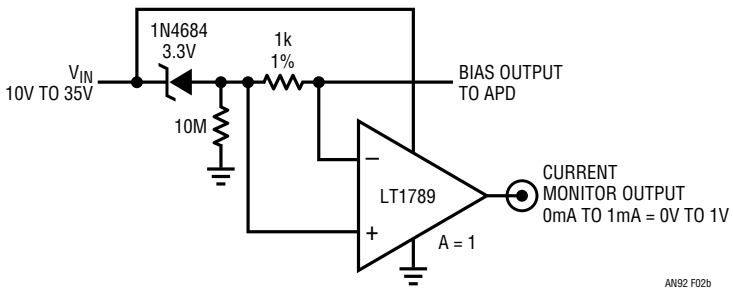
Carrier Based Current Monitor

Figure 4 utilizes AC carrier modulation techniques to meet APD current monitor requirements. It features 0.4% accuracy over the sensed current range, runs from a 5V supply and has the high noise rejection characteristics of carrier based "lock in" measurements.

The LTC1043 switch array is clocked by its internal oscillator. Oscillator frequency, set by the capacitor at Pin 16, is about 150Hz. S1 clocking biases Q1 via level shifter Q2. Q1 chops the DC voltage across the 1kΩ current shunt, modulating it into a differential square wave signal which



(2a)



(2b)

Figure 2. Instrumentation Amplifiers Extract Current Measurement from Modest Common Mode Voltages. Figure 2a Requires Separate Amplifier Power and Bias Supply Connections; Figure 2b Derives Both Connections from Single Point. Zener Level Shift Accomodates Amplifier Input Common Mode Range. Circuits Cannot Operate from Single, Low Voltage Rail, Swing Close to Zero or Accomodate High Bias Voltages

feeds A1 through 0.2µF AC coupling capacitors. A1's single-ended output biases demodulator S2, which presents a DC output to buffer amplifier A2. A2's output is the circuit output.

Switch S3 clocks a negative output charge pump which supplies the amplifier's V^- pins, permitting output swing to (and below) zero volts. The 100k resistors at Q1 minimize its on-resistance error contribution and prevent destructive potentials from reaching A1 (and the 5V rail) if either 0.2µF capacitor fails. A2's gain of 1.1 corrects for the slight attenuation introduced by A1's input resistors. In practice, it may be desirable to derive the APD bias voltage regulator's feedback signal from the indicated point, eliminating the 1kΩ shunt resistor's voltage drop.[1] Verifying accuracy involves loading the APD bias line with 100nA to 1mA and noting output agreement.[2]

DC Coupled Current Monitor

Figure 5's DC coupled current monitor eliminates the previous circuit's trim but pulls more current from the APD bias supply. A1 floats, powered by the APD bias rail. The 15V zener diode and current source Q2 ensure A1 never is exposed to destructive voltages. The 1kΩ current shunt's voltage drop sets A1's positive input potential. A1 balances its inputs by feedback controlling its negative input via Q1. As such, Q1's source voltage equals A1's

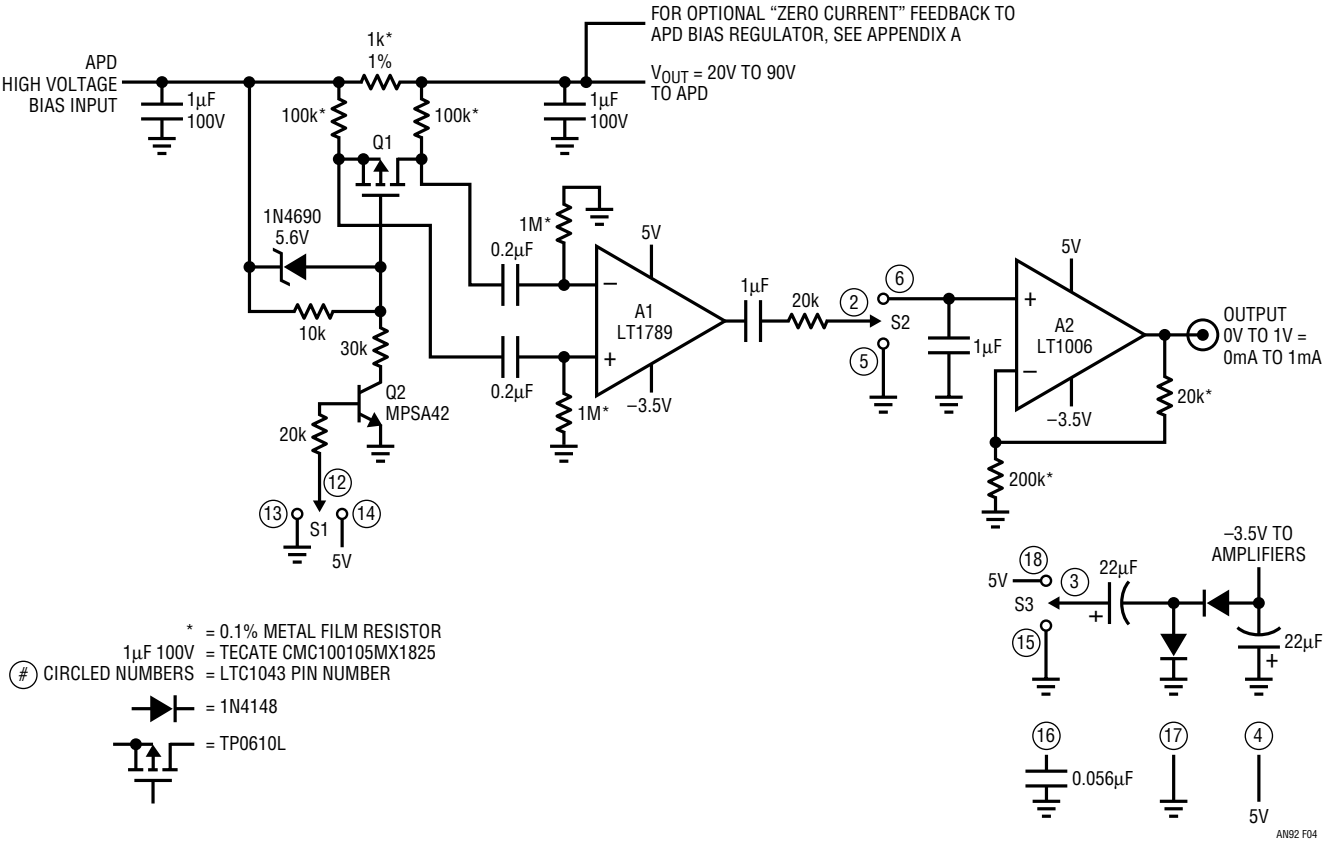


Figure 4. Lock-In Amplifier Technique Permits 1% Accurate APD Current Measurement Over 100nA to 1mA Range. APD Current Is AC Modulated by Q1, Single-Ended at A1 and Demodulated to DC by S2-A2

Note 1. See Appendix A, "Low Error Feedback Signal Derivation Techniques," for details.

Note 2. Appropriate high value load resistors, perhaps augmented with a monitoring current meter, are available from Victoreen and other suppliers. Tight resistor tolerance, while convenient, is not strictly required, as output target value is set by current meter indication.

positive input voltage and its drain current sets the voltage across its source resistor. Q1's drain current produces a voltage drop across the ground referred 1k resistor identical to the drop across the 1kΩ current shunt and, hence, APD current. This relationship holds across the 20V to 90V APD bias voltage range. The 5.6V zener assures A1's inputs are always within their common mode operating range and the 10M resistor maintains adequate zener current when APD current is at very low levels.

Two output options are shown. A2, a chopper stabilized amplifier, provides an analog output. Its output is able to swing to (and below) zero because its V^- pin is supplied with a negative voltage. This potential is generated by using A2's internal clock to activate a charge pump which, in turn, biases A2's V^- pin.[3]

A second output option substitutes an A-to-D converter, providing a serial format digital output. No V^- supply is required, as the LTC2400 A-to-D will convert inputs to (and slightly below) zero volts.

Resistors at strategic locations prevent destructive failures. The 51kΩ unit protects A1 if the APD bias line shorts to ground. The 10k resistor limits current to a safe value if Q1 fails and the 100k resistor serves a similar purpose if Q2 malfunctions. As in the previous figure, APD voltage regulator feedback may be taken at the current shunt's output to maintain optimal regulation.[4] As stated, this circuit does not require trimming and maintains 0.5% accuracy. It does, however, pull current approximately equalling the current delivered to the APD, in addition to Q2's collector current. This can be an issue if the APD bias supply has restricted current capability.

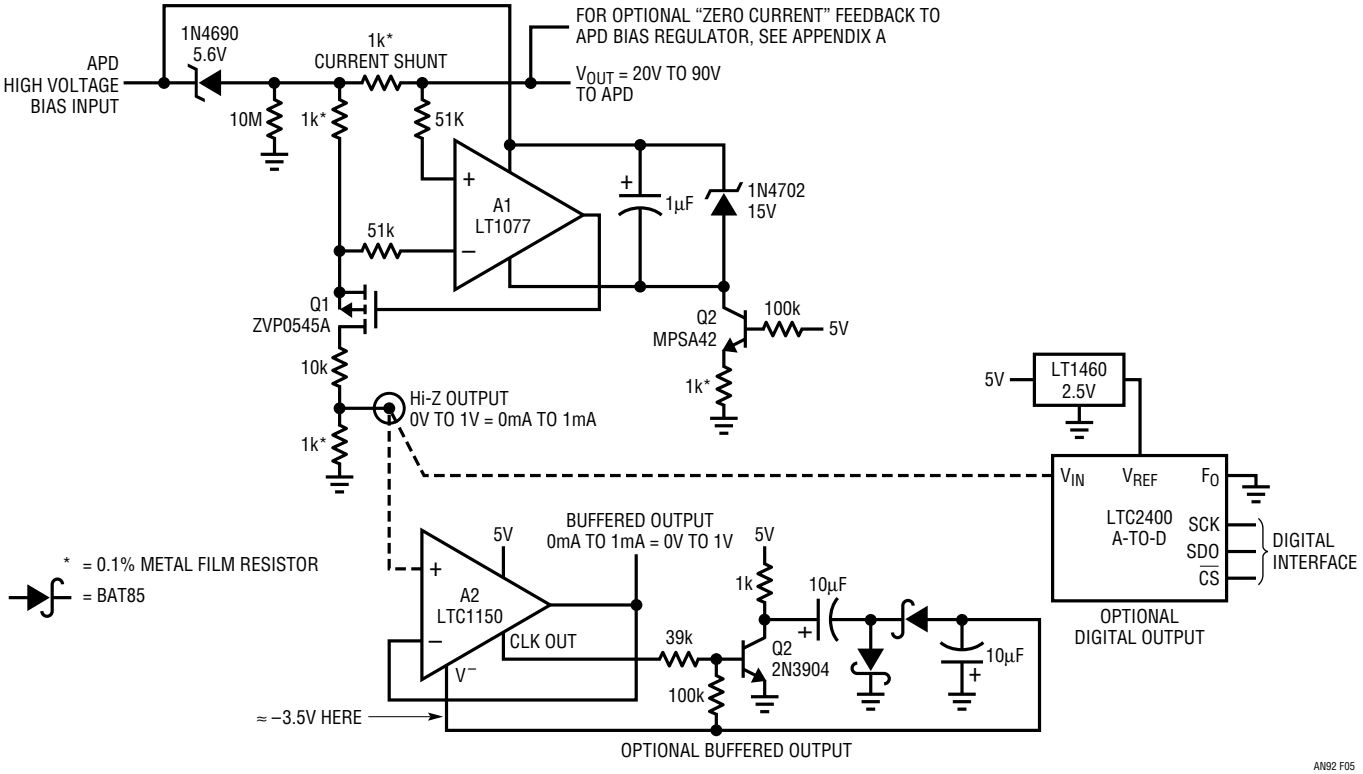


Figure 5. A1-Q1 Float at High Voltage Rail, Measuring APD Current Via 1kΩ Shunt. Q1's Ground Referred Drain Current Provides Hi-Z Output. Buffer Options Include Analog (Figure Bottom Left) and Digital (Figure Bottom Right)

Note 3. Circuit veterans will exercise extreme wariness when confronted with a bootstrapped biasing scheme such as this. Appendix D, "A Single Rail Amplifier with True Zero Volt Output Swing," should soothe anxieties.

Note 4: See Appendix A, "Low Error Feedback Signal Derivation Techniques."

APD Bias Supply

All previous examples have been current monitors. Figure 6, developed by Michael Negrete, is a high voltage APD bias supply.[5] The LT1930A switching regulator and L1 form a flyback based boost stage. The flyback events pump a diode-capacitor network tripler, producing a high voltage DC output. Feedback from the output via the R1-R2 combination stabilizes the regulator's operating point. D6 and D7 protect the switch and feedback pins, respectively, from parasitic negative excursions and the 10Ω resistors prevent excessive switch current. C8 and C9, series connected for high voltage capability, minimize output noise. A 0V to 4.5V programming voltage results in a corresponding 90V to 30V output (3% accuracy) with about 2mA of current capacity.

Circuit output noise is quite low. Figure 7, taken with 500µA loading at V_{OUT} = 50V, shows about 200µV ripple and harmonic residue in a 10MHz bandwidth. This is adequate for most APD receivers.[6]

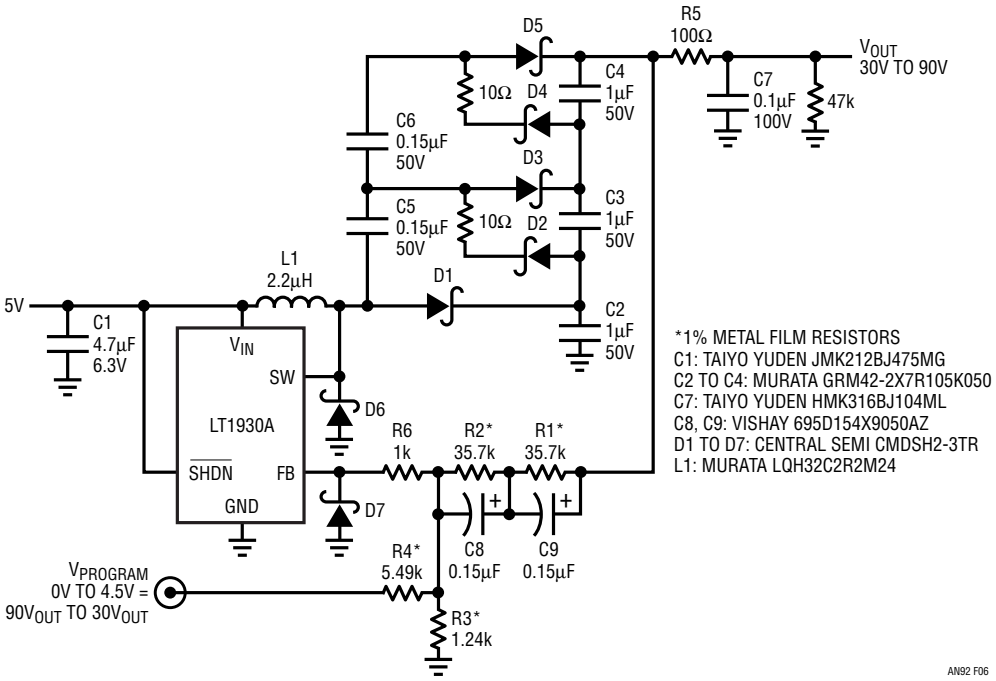


Figure 6. Boost Regulator/Charge Pump Supplies 30V to 90V APD Bias with Only 200µV_{P-P} Noise

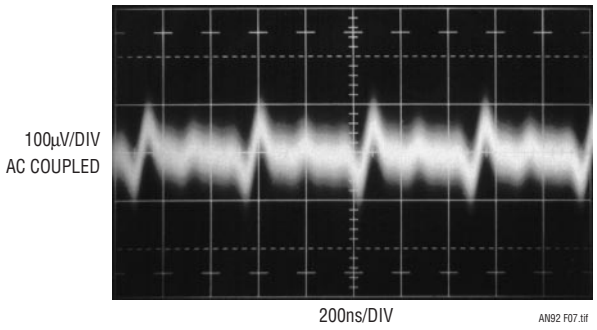


Figure 7. Figure 6's APD Bias Supply Shows 200µV_{P-P} Ripple and Harmonic Residue in 10MHz Bandwidth

Note 5: See Reference 7.

Note 6: Faithful noise measurements at these low levels requires considerable care. See Appendices B and C for practical details.

APD Bias Supply and Current Monitor

Figure 8, the Martin Configuration, combines the previous circuit with Figure 5's current monitor, providing a complete APD signal conditioner.[7] The programmable APD bias supply is as before, except that feedback comes via A2. A2, sensing after the 1kΩ current shunt, isolates the R1-R2 path loading, preventing it from influencing the shunt's voltage drop. A2's action also insures tight output regulation, despite the current shunt's presence.[8]

The current monitor, borrowing from Figure 5, measures across the 1kΩ current shunt, presenting its output in Q1's drain line. As shown, the output has about 1kΩ output impedance, although either of Figure 5's output options may be employed.

When considering circuit operation, note that both amplifiers are powered by the charge pump's high voltage output, with their V^- pin returned to the "2/3 V_{OUT}" point. This biasing permits the amplifiers to process high voltage signals, although the voltage across them never exceeds 30V.

Transformer Based APD Bias Supply and Current Monitor

Figure 9's circuit, another complete APD bias supply and current monitor, uses different techniques than the previous example. Advantages include 0.25% bias voltage and current monitoring accuracy, small size and fewer high voltage components for greater reliability. The LT1946 switching regulator and T1 form a flyback type boost configuration. T1's turn ratio provides voltage gain and the high voltage flyback events are rectified and smoothed to DC by the diode and capacitor in T1's secondary. This DC potential is divided down and fed back to A1. A1 compares this signal to the APD bias programming input and sets the LT1946's operating point, closing a control loop. Loop compensation is furnished by local rolloff at A1 and a lead network across the 10M feedback resistor. This loop establishes and maintains the APD bias output in accordance with the programming input's value. C1, active at V_{SUPPLY} = 1.2V, prevents output overshoot at power turn on by grounding the programming input command while

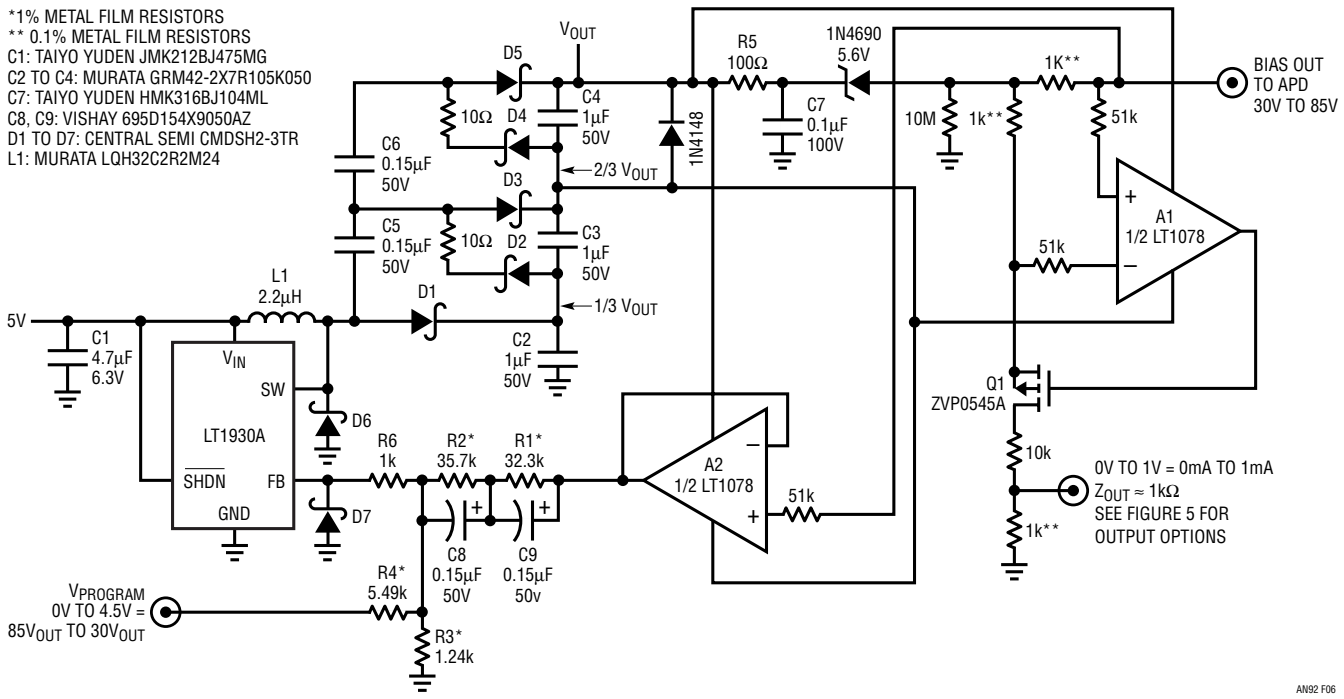


Figure 8. Figure 5's Current Monitor Combines with Figure 6's Bias Supply, Providing APD Bias and Current Measurement. A2 Buffers LT1930A's Feedback Path Loading from Bias Supply Output, Eliminating Current Error. Amplifiers Process 85V Signals, Although Voltage Across Them Never Exceeds 30V

Note 7: This circuit is based on work by Alan Martin.

Note 8: See Appendix A, "Low Error Feedback Signal Derivation Techniques," for further discussion.

simultaneously forcing A1's output low. This shuts off the switching regulator and no high voltage is produced. When power at turn on reaches ≈4V, C1 changes state and A1's positive input ramps to the programming voltage. The switching regulator's output follows this turn-on profile and no overshoot occurs. The LT1004 clamps spurious programming inputs beyond 2.5V, preventing excessive high voltage outputs.[9]

The circuit's current monitor portion takes full advantage of T1's floating secondary. Here, the 1kΩ current shunt resides in T1's secondary return path (Pin 3), eliminating the high common mode voltages encountered in the previous "high side" sensed examples. Circuit ground is declared at the shunt's uncommitted terminal, meaning T1's Pin 3 will undergo increasing negative excursion with greater APD current. Inverter A2 converts the shunt's negative voltage to a buffered positive output. Its gain, scaled 1% above unity, compensates its input resistor's shunt loading error. Swing to zero is facilitated by returning A2's V^- pin to a small negative potential derived from the LT1946's V_{SW} pin switching. The 10M-287k divider's current loading error is prevented from appearing in A2's output by a compensatory current from the APD bias programming input. This compensating current, arriving at A2 via the 100k-3.65k-1M network, is scaled to precisely balance out the shunt's output portion due to the 10M-287k path's loading error. See Appendix A for detailed discussion of this technique.

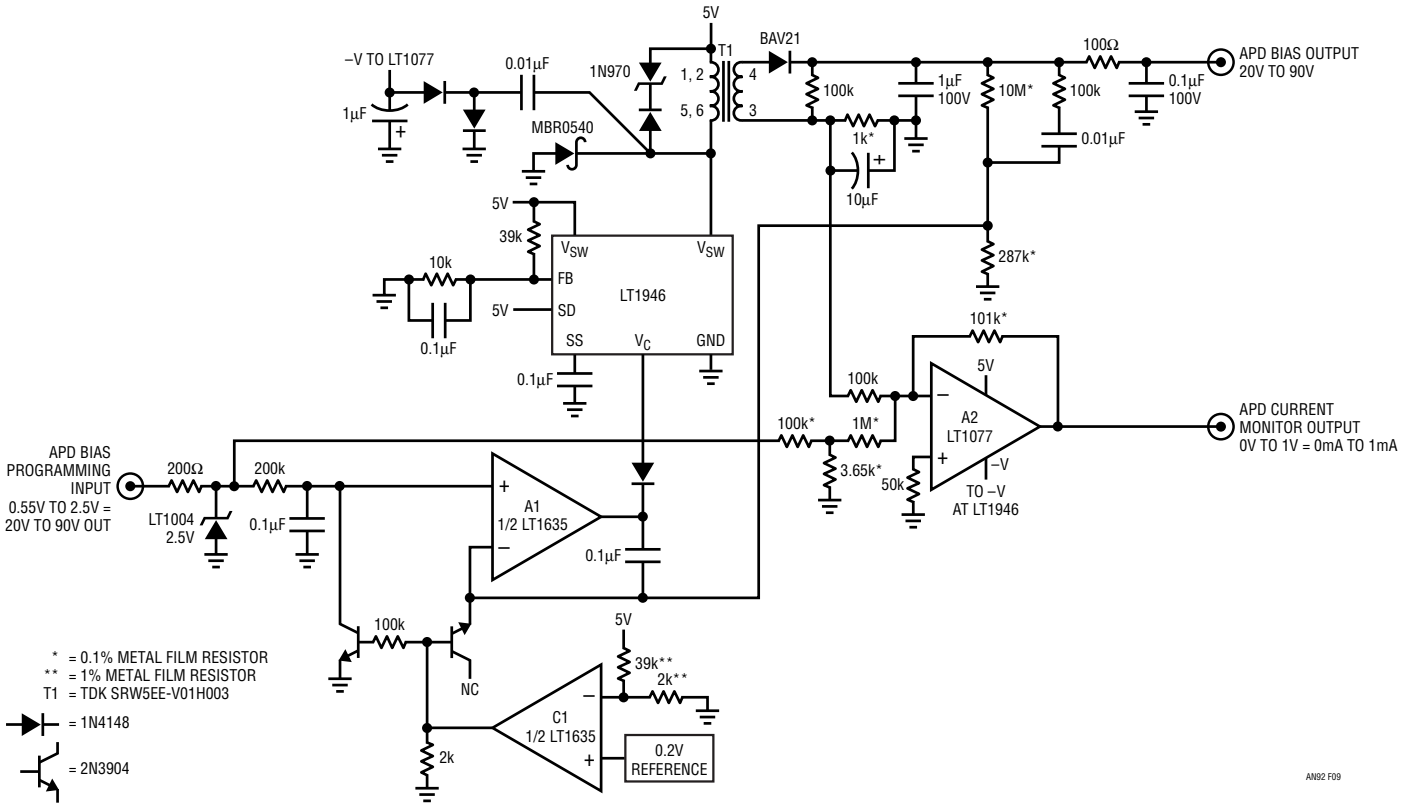


Figure 9. A1 Controls LT1946 Boost Regulator to Supply 20V to 90V Bias. C1 Prevents Output Overshoot at Power Turn-On. A2 Senses APD Current Across 1kΩ Shunt in T1's Output Return. Programming Input Feedforward to A2 Cancels 10M-287k Feedback Divider's Loading Error, Preserving Current Monitor Accuracy

Note 9: Optional circuitry allows input clamping at any desired voltage. See Appendix E, "APD Protection Circuits."

Output noise for this circuit, shown in Figure 10, is about 1mV$_{P-P}$ in a 10MHz bandwidth. This is characteristic of flyback regulators and somewhat higher than Figure 8's charge pump based arrangement. It is still acceptable for most APD receivers, although special switching regulator techniques (read on!) can considerably reduce this figure.

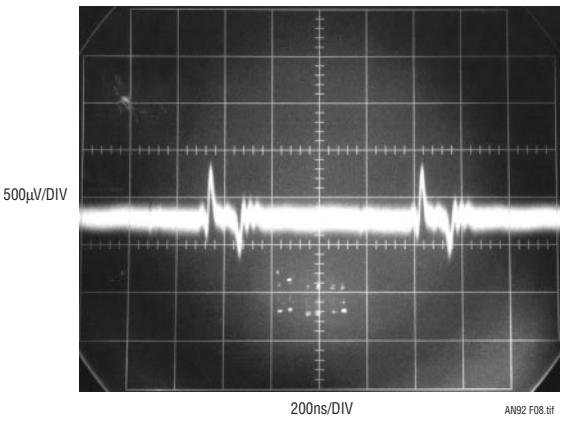


Figure 10. Figure 9's Output Noise Measures 1mV$_{P-P}$ in 10MHz Bandwidth

Inductor Based APD Bias Supply

Figure 11 borrows from Figure 9's flyback technique to form a simple, small area APD bias supply. Figure 9's current monitor function has been deleted—this circuit provides only the bias supply. Additionally, Figure 9's transformer has been replaced with a 2-terminal inductor. The circuit is a basic inductor flyback boost regulator with a single important deviation. Q1, a high voltage device, has been interposed between the LT1946 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high voltage stress. Q1, operating as a "cascode" with the LT1946's internal switch, withstands L1's high voltage flyback events.[10] Diodes associated with Q1's source terminal clamp L1 originated spikes arriving via Q1's junction capacitance. The high voltage is rectified and filtered to DC, forming the circuit's output. Feedback to the regulator stabilizes the output, which may be varied by appropriate biasing at the V$_{PROGRAM}$ input. Components at the LT1946 V$_C$ pin compensate the loop. Over a 20V to 90V output range, the circuit remains within 2% of the V$_{PROGRAM}$ input dictated output voltage. Figure 12 shows switching related output noise is about 1.3 millivolts peak-to-peak in a 10MHz bandwidth.

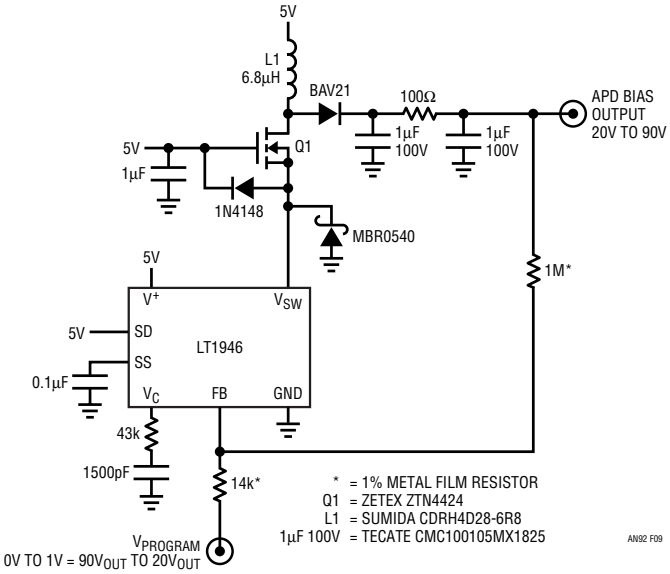


Figure 11. Q1 Cascoded with LT1946 Switches L1, Providing 20V to 90V APD Bias Output. Q1's Source Diodes Clamp Parasitic Conducted Spikes to Safe Levels

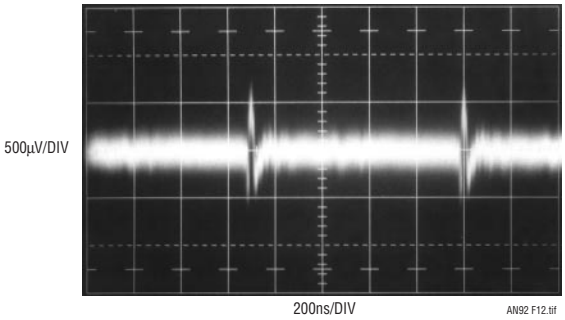


Figure 12. Cascode Based Bias Supply Noise in 10MHz Bandwidth Is About 1.3mV$_{P-P}$

Note 10: See Reference 11.

200µV Output Noise APD Bias Supply

Some APD receiver applications require extremely low noise in an extended bandwidth. Figure 13's APD bias supply uses special switching regulator techniques to achieve 200µV noise in a 100MHz bandwidth. The LT1533 is a "push-pull" output switching regulator with controllable switch transition times. Output harmonic content ("noise") is notably reduced with slower switch transition times.[11] Switch current and voltage transition times are controlled by resistors at the R_{CSL} and R_{VSL} pins, respectively. In all other respects, the circuit behaves as a classical push-pull, transformer based, step-up converter. The V_{PROGAM} input biases a feedback loop, setting the output anywhere between 20V and 90V.

The controlled transition times result in a dramatic decrease in output noise. Figure 14 shows ripple and switching related residue of 200µV in a 100MHz bandwidth. This is far below conventional regulators, meeting the most stringent noise requirement.

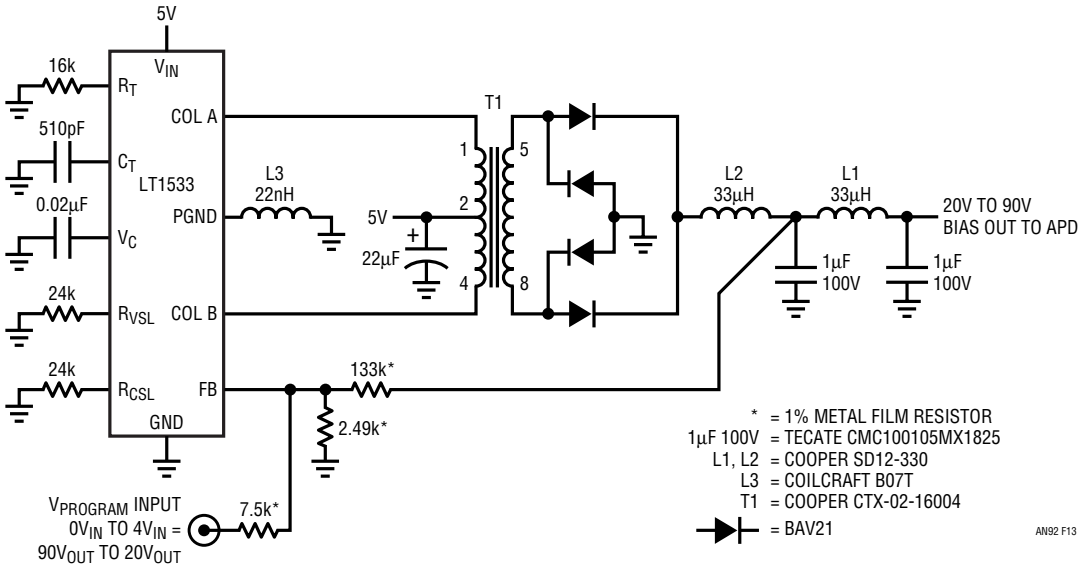


Figure 13. Transformer Coupled 20V to 90V APD Bias Supply Controls Switch Transition Time for Extremely Low Output Noise

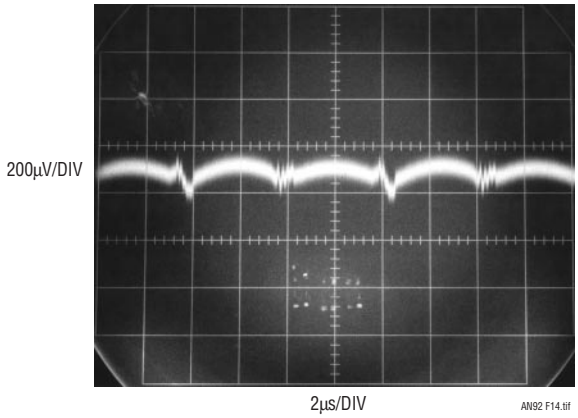


Figure 14. LT1533's Controlled Transition Times Achieve Spectacularly Low Output Harmonic Residue. Switching Related Noise Is Below 100µV, Fundamental Ripple About 200µV. Measurement Bandwidth is 100MHz

Note 11: Noise contains no regularly occurring or coherent components. As such, switching regulator output "noise" is a misnomer. Unfortunately, undesired switching related components in the regulated output are almost always referred to as "noise." Accordingly, although technically incorrect, this publication treats all undesired output signals as "noise." See Reference 2.

Low Noise APD Bias Supply and Current Monitor

Figure 15 builds on the previous circuit's performance, forming a complete, high performance APD signal conditioner. The bias supply is identical to Figure 13's low noise example, with the addition of the A1 based feedback buffer. This stage, similar to the one in Figure 8, isolates the regulator's feedback path current from the 1kΩ shunt, preserving current monitor accuracy. A1's zener-current source power biasing scheme permits it to process high voltage signals even though it is a low voltage device.[12] The current monitor, shown in block form, may be selected from the choices indicated depending upon requirements.

0.02% Accuracy Current Monitor

Some APD current monitor applications call for high accuracy and stability. Figure 16's unusual optical switching based approach achieves 0.02% accuracy over a sensed 100nA to 1μA range. This scheme measures shunt current by switching (S1A, S1B) a capacitor across the shunt ("ACQUIRE"). After a time the capacitor charges to the voltage across the shunt. S1A and S1B open and S2A and S2B close ("READ"). This grounds one capacitor plate and the capacitor discharges into the grounded 1μF unit at S2B. This switching cycle is continuously repeated, resulting in A1's ground referred positive input assuming the same voltage that is across the floating 1kΩ shunt. The LED driven MOSFET switches specified do not have junction potentials and the optical drive contributes no charge injection error. A nonoverlapping clock prevents simultaneous conduction in S1 and S2, which would result in charge loss, causing errors and possible circuit damage. The 5.1V zener prevents switched capacitor failure if the bias output is shorted to ground.

A1, a chopper stabilized amplifier, has a clock output. This clock, level shifted and buffered by Q3, drives a logic divider chain. The first flip-flop activates a charge pump, pulling A1's V^- pin negative, permitting amplifier swing to (and below) zero volts.[13] The divider chain terminates into a logic network. This network provides phase opposed charging of the 0.02μF capacitors (Traces A and B, Figure 17). The gating associated with these capacitors is arranged so the logic provides nonoverlapping, complementary biasing to Q1 and Q2. These transistors supply this nonoverlapping drive to the S1 and S2 actuating LEDs (Traces C and D).

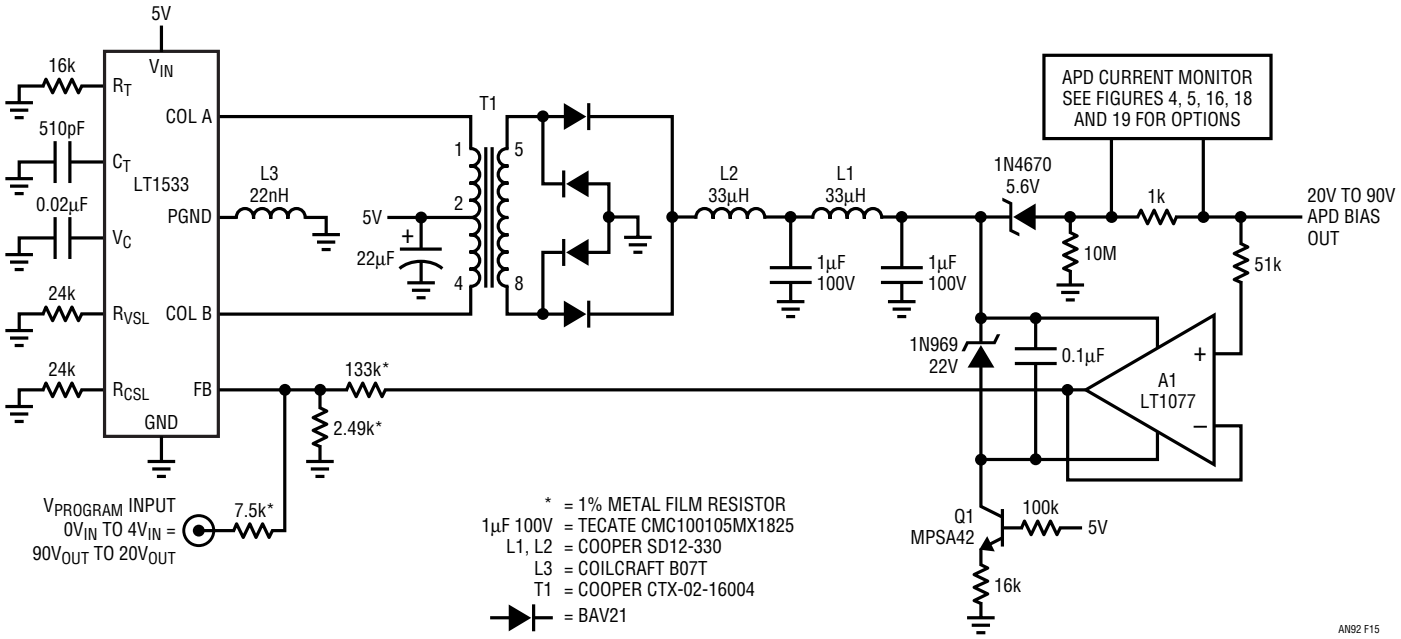


Figure 15. Figure 13 Augmented with Feedback Divider Buffer and Current Monitor Provides Complete 100μV Noise APD Signal Conditioner

Note 12: The feedback buffer is considered in detail in Appendix A, "Low Error Feedback Signal Derivation Techniques."

Note 13: This scheme, a variant of the one described back in Figure 5, is detailed in Appendix D, "A Single Rail Amplifier with True Zero Volt Output Swing."

The extremely small parasitic error terms in the LED driven MOSFET switches results in nearly theoretical circuit performance. However, residual error (≈0.1%) is caused by S1A's high voltage switching pumping S2B's 3pF to 4pF junction capacitance. This results in a slight quantity of unwanted charge being transferred to the 1µF capacitor at S2B. The amount of charge transferred varies with the APD bias voltage (20V to 90V) and, to a lesser extent, the varactor-like response of S2B's off-state capacitance. These terms are partially cancelled by DC feedforward to A1's negative input and AC feedforward from Q1's gate to S2B. The corrections compensate error by a factor of five, resulting in 0.02% accuracy.

Optical switch failure could expose A1 to high voltage, destroying it and possibly presenting destructive voltages to the 5V rail. This most unwelcome state of affairs is prevented by the 47k resistors in A1's positive input.

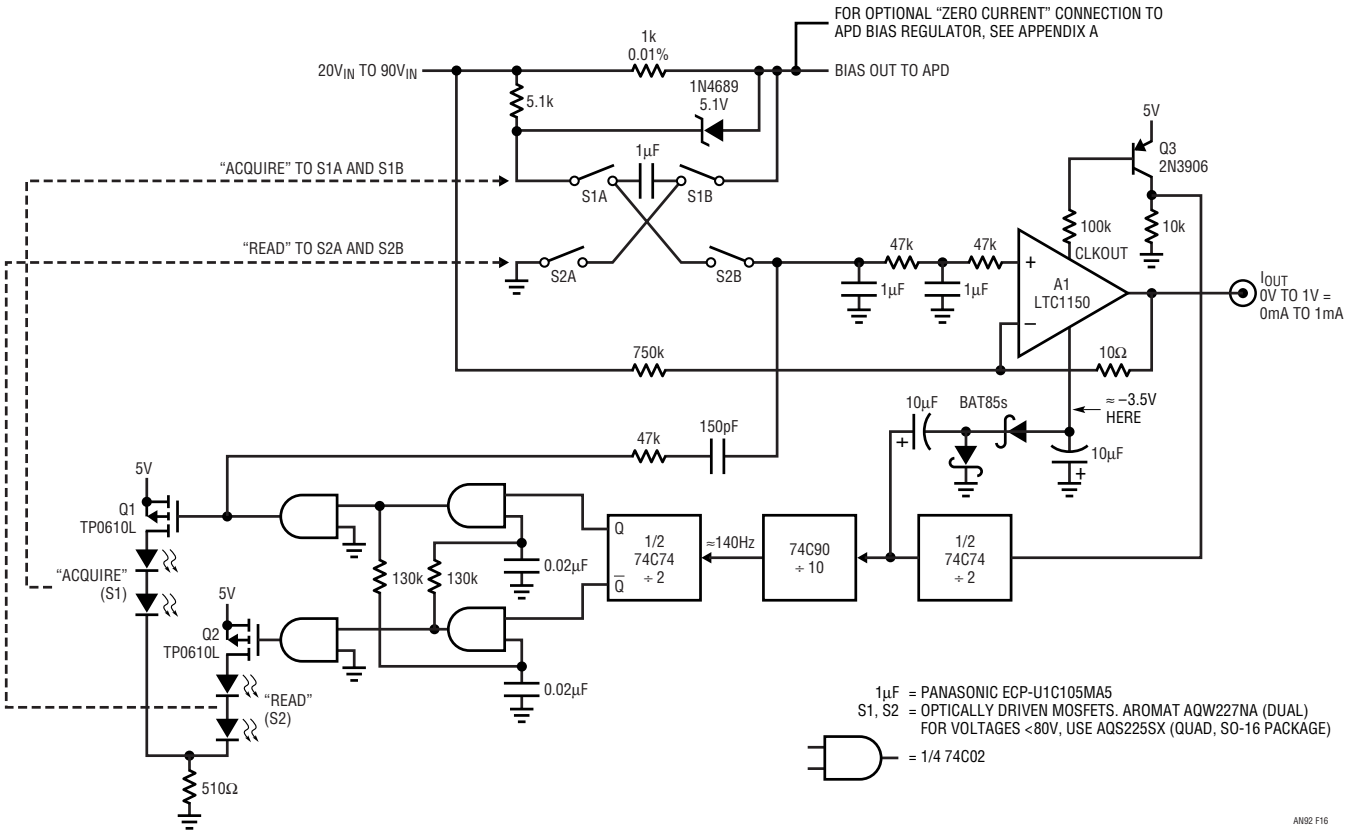


Figure 16. A 0.02% Accurate APD Current Monitor Utilizes Optically Driven FETs and Flying Capacitor. Logic Driven Q1-Q2 Provides Nonoverlapping Clocking to S1-S2 LEDs. Clock Derives from A1's Internal Oscillator

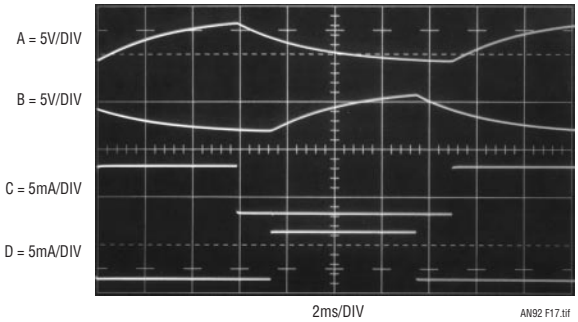


Figure 17. Clocked, Cross Coupled Capacitors (Traces A and B) in 74C02 Based Network Result in Nonoverlapping Drive (Traces C and D) to S1-S2 Actuating LEDs

Digital Output 0.09% Accuracy Current Monitor

Figure 18 modifies the optically based current monitor to supply a digital output. The schematic is essentially identical to Figure 16's, with two significant differences. Here, a digital output is supplied via the LTC2431 A-to-D converter. The converter's differential inputs allow the same feedforward based error correction used in the previous example. The divider chain countdown ratio has changed to accomodate a higher speed clock, sourced by the LTC1799 oscillator. This higher speed clock, which times A-to-D operation, centers the A-to-D's internal notch filter at the optical switches commutation frequency, maximizing rejection.[14]

This circuit's 0.09% accuracy does not equal the previous analog ouput's version because of the LT1460 reference's 0.075% tolerance, which is not trimmable. The circuit can be adjusted to 0.02% accuracy by trimming the 1kΩ shunt so measured output current directly corresponds to A-to-D output.

Digital Output Current Monitor

Previous current monitor examples furnish digital output from ground referenced A-to-D converters fed from analog level shifting stages. Figure 19 directly digitizes shunt current by floating the A-to-D converter in the APD bias line. The A-to-D output is level shifted in the digital

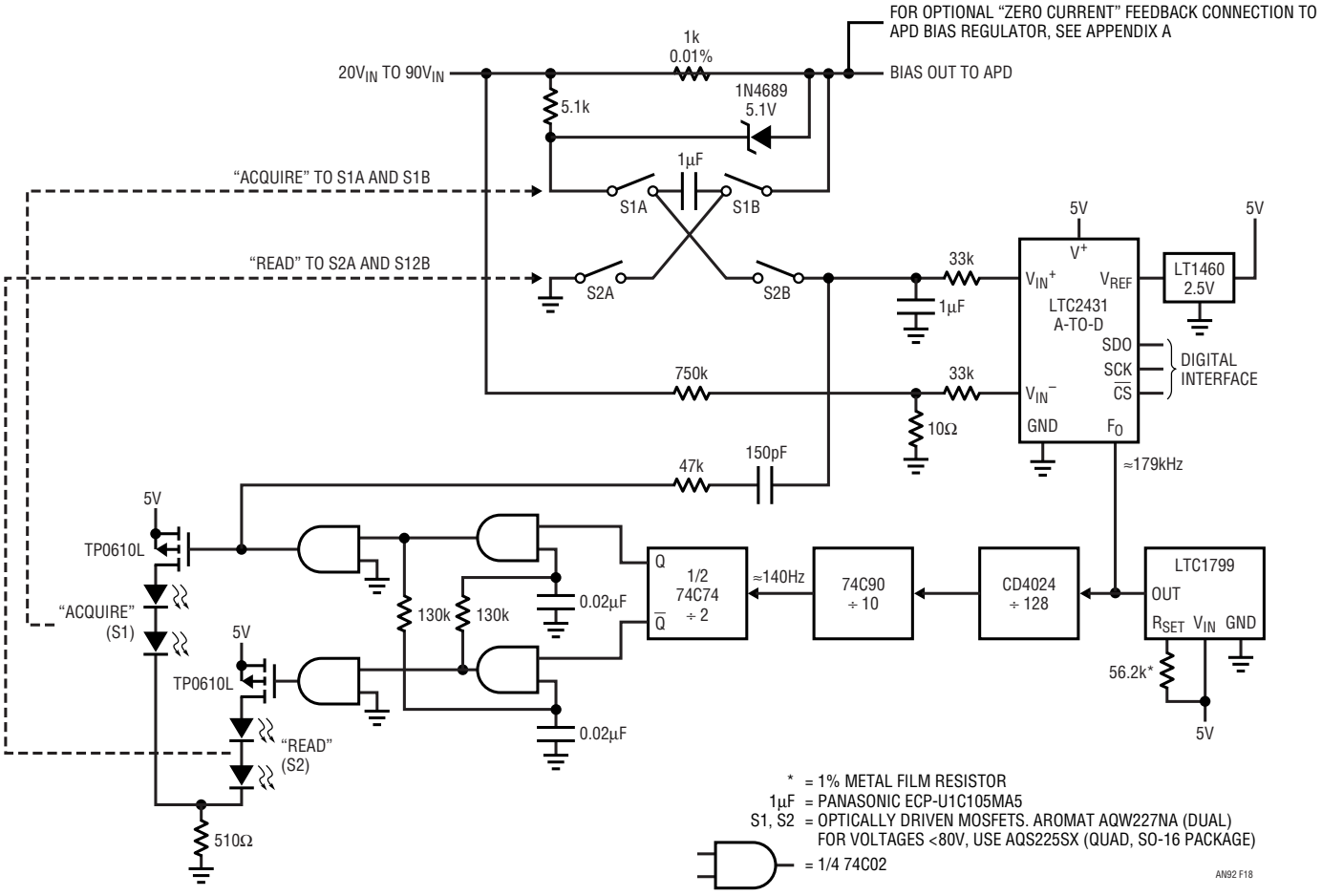


Figure 18. Figure 16's Optically Driven FET Based Current Monitor Modified for Digital Output. LTC1799 Clocks A-to-D and Optical Switch LEDs. 0.09% Accuracy, Trimmable to 0.02%

Note 14: The LTC2431's internal digital filter's first null occurs at 1/2560 of the frequency applied to its F_O pin. For details, see the LTC2431 data sheet.

domain, presenting ground referred digital data. This simple approach is attractive, although the available APD bias supply must supply about 3mA to the A-to-D and its attendant circuitry.

The LTC2410 and its LT1029 reference are powered directly from the high voltage APD bias supply input. Current sink Q3 and the LT1029 bias the LTC2410 V^- pin, maintaining 5V across the A-to-D over the 20V to 90V bias rail range. The A-to-D's differential inputs measure across the 1kΩ current shunt. Resistors and a zener clamp protect the A-to-D from excessive voltages if the APD bias line is shorted to ground. The A-to-D's digital outputs, floating at high voltage, drive level shifts which provide ground referred data. One of the identical stages is shown; the other indicated in conceptual form. The stage is designed for low quiescent and dynamic current consumption while maintaining data fidelity. This is necessary to minimize current drain from the APD bias supply and to avoid modulating it with transient loading artifacts. High voltage common emitter Q1 sources current to Q2, which provides a ground referred logic compatible output. Capacitive feedforwards maintain data edge speed while minimizing standing current requirements.

This circuit's 0.25% untrimmed accuracy is due to shunt and LT1029 tolerances. Trimming the LT1029 (see schematic note) permits 0.05% accuracy.

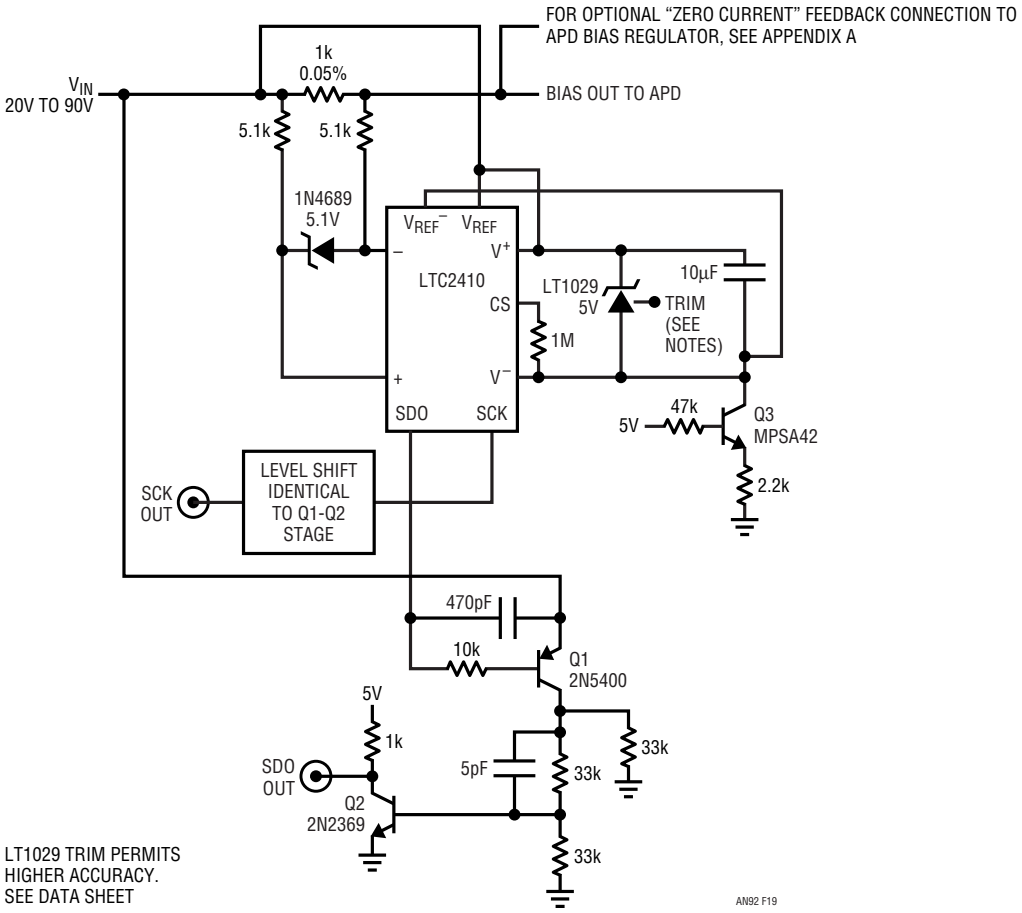
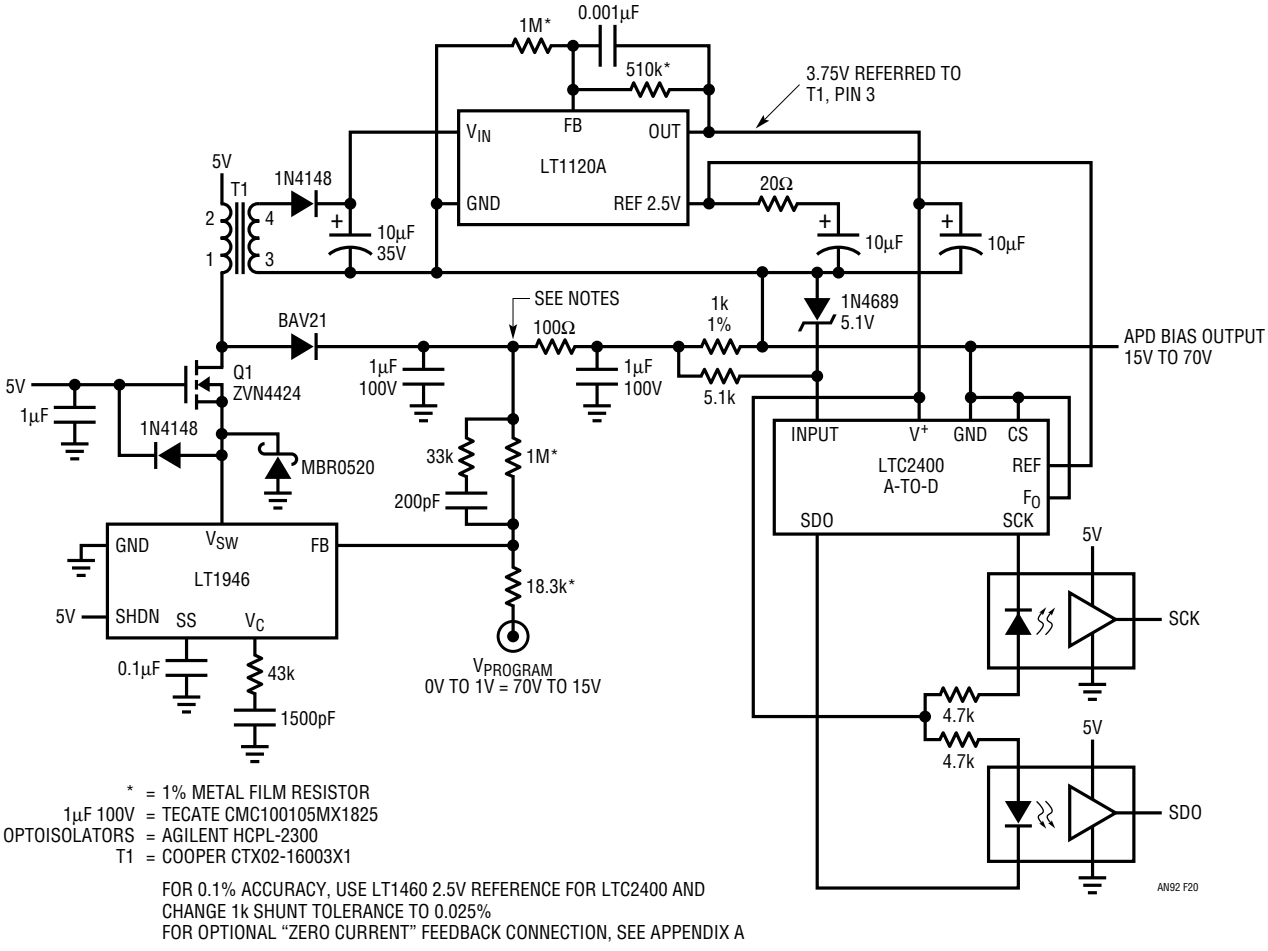


Figure 19. A-to-D Converter Floats at High Voltage, Forming Digital Output Current Monitor. Q1-Q2 Level Shift Provides Ground Referenced Digital Output. 0.25% Accuracy Is Trimmable to 0.05%

Digital Output Current Monitor and APD Bias Supply

Figure 20 also floats an A-to-D converter across the shunt, while including an APD bias supply. The bias supply is derived from the LT1946 switching regulator and Q1, operating in nearly identical fashion to Figure 11's circuit. The primary difference is that Figure 11's inductor is replaced here with a transformer. The transformer's primary winding furnishes high voltage step-up, similar to Figure 11. The floating secondary drives an isolated LT1120 based 3.75V regulator. This floating regulator's output, stacked on top of the APD bias line, powers the LTC2400 A-to-D converter. The isolated 3.75V supply permits the A-to-D to measure across the 1kΩ shunt without pulling operating power from the APD supply. Resistive current limiting and the 5.1V zener protect the A-to-D from high voltage if the APD bias output is shorted to ground. Low power optoisolators provide ground referred digital output while eliminating floating supply "starve out" due to cross regulation interaction with the APD regulation loop. Specifically, very low power APD bias outputs could result in insufficient transformer flux to furnish floating supply loading requirements. Common optoisolators require significant current, mandating the low power types specified. The previous circuit's discrete level shift stage would draw even less power but the optoisolators are simple and adequate.



* = 1% METAL FILM RESISTOR
1µF 100V = TECATE CMC100105MX1825
OPTOISOLATORS = AGILENT HCPL-2300
T1 = COOPER CTX02-16003X1

FOR 0.1% ACCURACY, USE LT1460 2.5V REFERENCE FOR LTC2400 AND CHANGE 1k SHUNT TOLERANCE TO 0.025%
FOR OPTIONAL "ZERO CURRENT" FEEDBACK CONNECTION, SEE APPENDIX A

Figure 20. APD Bias Supply with Digital Output Current Monitor. T1's Primary Supplies APD High Voltage Source, Similar to Figure 11; Secondary Furnishes Power to Floating Circuitry. 1kΩ Shunt Voltage Drop Is Compensatible Using Optional Feedback Circuitry. Optoisolators Provide Ground Referred Digital Output. Current Monitor Accuracy is 2%, Trimmable to 0.1%

The LT1120 2.5V reference and 1kΩ shunt tolerances dictate 2% circuit accuracy. If the tighter tolerance components noted in the schematic are used, 0.1% accuracy is practical.

Summary

Figure 21's chart is an attempt to summarize the circuits presented, although such brevity breeds oversimplification. As such, although the chart reviews salient features, there is no substitute for a thorough investigation of any particular application's requirements.

FIGURE NUMBER	BIAS SUPPLY CAPABILITY	ANALOG OUTPUT CURRENT MONITOR (100nA to 1mA)	DIGITAL OUTPUT CURRENT MONITOR (100nA to 1mA)	COMMENTS
4	No	Yes	No	0.4% Accuracy. High Noise Rejection
5	No	Yes	Yes	0.5% Accuracy. Draws Current from APD Bias Supply Approximately Equalling Current Delivered to the APD in Addition to Housekeeping Current
6	Yes 30V to 90V	No	No	200μV Noise in 10MHz Bandwidth. 3% Accuracy
8	Yes 30V to 85V	Yes	No	3% Bias Voltage Accuracy. 0.5% Current Monitor Accuracy. Current Monitor Has 1kΩ Output Impedance
9	Yes 20V to 90V	Yes	No	0.25% Bias Voltage Accuracy. 1mV Output Noise in 10MHz Bandwidth. 0.25% Current Monitor Accuracy. Small Size. Few Large Value, High Voltage Capacitors Improves Reliability. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level
11	Yes 20V to 90V	No	No	2% Bias Voltage Accuracy. 1.5mV Output Noise in 10MHz Bandwidth. Small Size, Simple
13	Yes 20V to 90V	No	No	2% Bias Voltage Accuracy. 200μV Ripple and Noise in 100MHz Bandwidth. Relatively Large Solution Size Due to 250kHz Oscillator Frequency
15	Yes 20V to 90V	Yes	Yes	2% Bias Voltage Accuracy. 200μV Ripple and Noise in 100MHz Bandwidth. Current Monitor Accuracy Depends on Option Selected. Relatively Large Solution Size Due to 250kHz Oscillator Frequency
16	No	Yes	No	0.02% Accuracy. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level
18	No	No	Yes	0.09% Accuracy. 0.02% Achievable with Shunt Trimming. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level
19	No	No	Yes	0.25% Accuracy. Trimmable to 0.05% by Adjusting Reference
20	Yes 15V to 70V	No	Yes	2% Bias Voltage Accuracy. 2% Current Monitor Accuracy. 0.1% Accuracy Obtainable with Optional LT1460 Reference. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level

Figure 21. Summarized Characteristics of Techniques Presented. Applicable Circuit Depends on Application Specifics

Note: *This application note was derived from a manuscript originally prepared for publication in EDN magazine.*

REFERENCES

1. Meade, M.L., "Lock-In Amplifiers and Applications," London, P. Peregrinus, Ltd.
2. Williams, J., "A Monolithic Switching Regulator with 100μV Output Noise," Linear Technology Corporation, Application Note 70, October 1997.
3. Williams, J., "Measurement and Control Circuit Collection," "ΔV_{BE} Based Thermometer," Linear Technology Corporation, Application Note 45, June 1991, pp. 7–8
4. Williams, J., "Applications for a Switched Capacitor Instrumentation Building Block," Linear Technology Corporation, Application Note 3, July 1985.
5. Williams, J., "Monolithic CMOS-Switch IC Suits Diverse Applications," EDN Magazine, October 4, 1984.
6. Williams, J., "A Fourth Generation of LCD Backlight Technology," "Floating Lamp Circuits," Linear Technology Corporation, Application Note 65, November 1995, pp. 40–43, Figure 48.
7. Negrete, M., "Fiberoptic Communication Systems Benefit from Tiny, Low Noise Avalanche Photodiode Bias Supply," Linear Technology Corporation, Design Note 273, December 2001.
8. Martin, A., "Charge Pump Based APD Circuits," Private Communication, May 2002.
9. Williams, J., "Applications of New Precision Op Amps," "Instrumentation Amplifier with V_{CM} = 300V and 160dB CMRR," Linear Technology Corporation, Application Note 6, January 1985, pp. 1–2.
10. Williams, J., "Bridge Circuits," "Optically Coupled Switched Capacitor Instrumentation Amplifier," Linear Technology Corporation, Application Note 43, June 1990, pp. 9–10
11. Hickman, R. W. and Hunt, F. V., "On Electronic Voltage Stabilizers," "Cascode," Review of Scientific Instruments, January 1939, pp. 6–21, p. 16.

APPENDIX A

LOW ERROR FEEDBACK SIGNAL DERIVATION TECHNIQUES

Various text circuits either detail or make reference to counteracting loading effects of the APD bias supply's output feedback divider. If the divider is located before the 1kΩ current shunt, its current drain is not included in the current monitor's output and no error is incurred. A potential difficulty with this approach is that the 1kΩ shunt appears in series with the bias supply output, degrading load regulation. The maximum 1mA shunt current produces a 1V output regulation drop. In some cases this is permissible and no further consideration is required. Circumstances dictating tighter load regulation require compensation techniques.

Divider Current Error Compensation—"Low Side" Shunt Case

When the shunt is in a transformer's return path ("low side shunt"), divider error is cancelled by introducing a compensatory term into the APD current monitor circuitry. Figure A1 shows details. The output voltage divider's current loading error is prevented from appearing in A1's output by feeding forward a compensatory current from the APD bias programming input. This compensating current, arriving at A1 via R_{LARGE}, is scaled to precisely balance out the portion of shunt output contributed by the voltage divider's loading error.

Divider Current Error Compensation—"High Side" Shunt Case

Figure A2 addresses situations where the shunt resides in the "high side." Such arrangements involve high common mode voltages, seemingly mandating a high voltage buffer amplifier to isolate the divider's current loading. Figure A2 shows a way around this, using standard low voltage amplifiers to process high voltage signals. A1, sensing after the 1kΩ shunt, isolates the feedback divider's loading while permitting the APD bias regulator to include the shunt within its feedback loop. A1 is powered directly from the bias regulator's high voltage output but its V^- pin is

zener clamped with respect to its V+ pin. Current sink Q1 maintains this bias over the wide range of possible APD regulator outputs. Although A1 processes high voltage signals, the voltage across it is held to safe levels. The 5.6V zener in the APD bias line ensures A1's inputs are always inside their common mode operating range. The 10M resistor maintains adequate zener bias when APD currents are extremely low. A 51k resistor protects A1 from destructive high voltage if the APD bias output is shorted to ground. Similarly, the 100k resistor prevents high voltage from appearing on the 5V supply if Q1 fails.

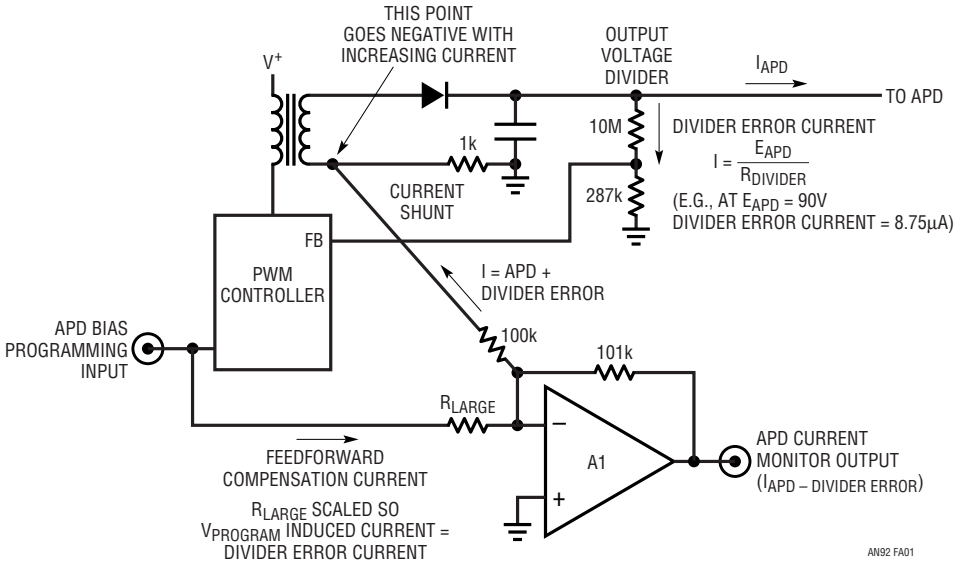


Figure A1. Output Voltage Divider Current Loading Error Is Compensated with Feedforward from Programming Input. A1 Algebraically Sums Feedforward Term and Current Shunt Information, Presents Corrected Output

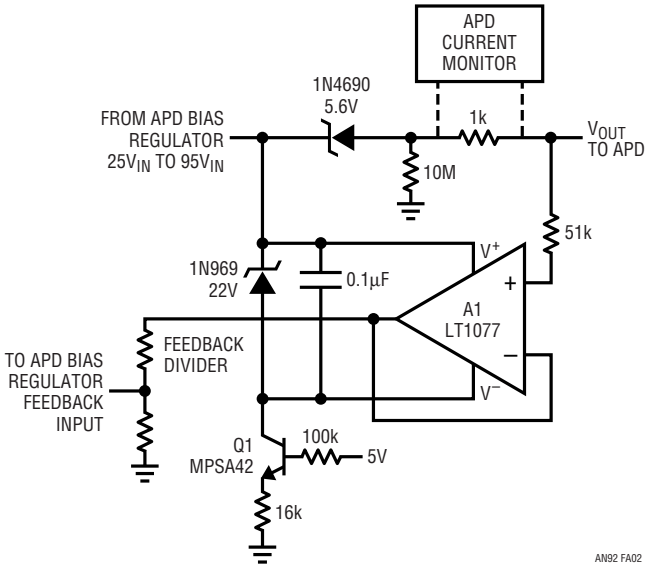


Figure A2. A1 Follower Floats from High Voltage Rail, Eliminates Feedback Divider Current Loading Error. Q1 Current Source and 22V Zener Maintain Low Voltage Across Amplifier; 5.6V Zener Accomodates A1's Input Range

APPENDIX B

PREAMPLIFIER AND OSCILLOSCOPE SELECTION

The low level measurements described require some form of preamplification for the oscilloscope. Current generation oscilloscopes rarely have greater than 2mV/DIV sensitivity, although older instruments offer more capability. Figure B1 lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units feature wideband, low noise performance. It is particularly significant that many of these instruments are no longer produced. This is in keeping with current instrumentation trends, which emphasize digital signal acquisition as opposed to analog measurement capability.

The monitoring oscilloscope should have adequate bandwidth and exceptional trace clarity. In the latter regard high quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments is well-suited to low level noise measurement.[1] The digitizing uncertainties and raster scan limitations of DSOs impose display resolution penalties. Many DSO displays will not even register the small levels of switching-based noise.

INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Amplifier	Hewlett-Packard	461A	150MHz	Gain = 100	Secondary Market	50Ω Input, Standalone
Differential Amplifier	Tektronix	1A5	50MHz	1mV/DIV	Secondary Market	Requires 500 Series Mainframe
Differential Amplifier	Tektronix	7A13	100MHz	1mV/DIV	Secondary Market	Requires 7000 Series Mainframe
Differential Amplifier	Tektronix	11A33	150MHz	1mV/DIV	Secondary Market	Requires 11000 Series Mainframe
Differential Amplifier	Tektronix	P6046	100MHz	1mV/DIV	Secondary Market	Standalone
Differential Amplifier	Preamble	1855	100MHz	Gain = 10	Current Production	Standalone, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Standalone, Settable Bandstops

Figure B1. Some Applicable High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability

Note 1: In our work we have found Tektronix types 453, 453A, 454, 454A, 547 and 556 excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise floor limited background.

APPENDIX C

PROBING AND CONNECTION TECHNIQUES FOR LOW LEVEL, WIDEBAND SIGNAL INTEGRITY[1]

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. The low level, wideband measurements demand care in routing signals to test instrumentation.

Ground Loops

Figure C1 shows the effects of a ground loop between pieces of line-powered test equipment. Small current flow between test equipment's nominally grounded chassis creates 60Hz modulation in the measured circuit output. *This problem can be avoided by grounding all line powered test equipment at the same outlet strip or otherwise ensuring that all chassis are at the same ground potential. Similarly, any test arrangement that permits circuit current flow in chassis interconnects must be avoided.*

Pickup

Figure C2 also shows 60Hz modulation of the noise measurement. In this case, a 4-inch voltmeter probe at the feedback input is the culprit. *Minimize the number of test connections to the circuit and keep leads short.*

Poor Probing Technique

Figure C3's photograph shows a short ground strap affixed to a scope probe. The probe connects to a point which provides a trigger signal for the oscilloscope. Circuit output noise is monitored on the oscilloscope via the coaxial cable shown in the photo.

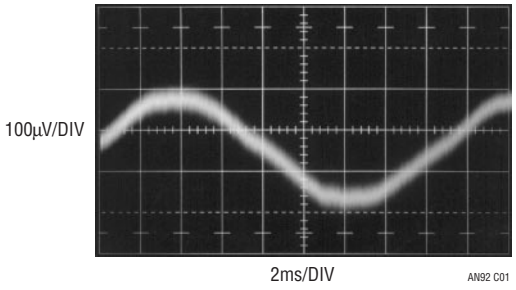


Figure C1. Ground Loop Between Pieces of Test Equipment Induces 60Hz Display Modulation

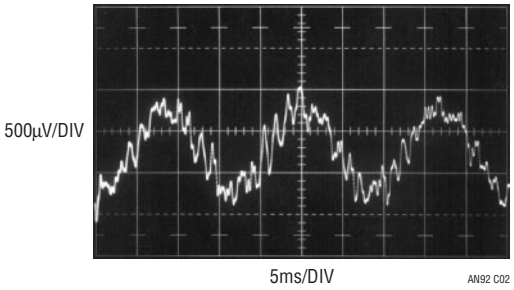


Figure C2. 60Hz Pickup Due to Excessive Probe Length at Feedback Node

Note 1: Veterans of LTC Application Notes, a hardened crew, will recognize this Appendix from AN70 (see Reference 2). Although that publication concerned considerably more wideband noise measurement, the material is directly applicable to this effort. As such, it is reproduced here for reader convenience.

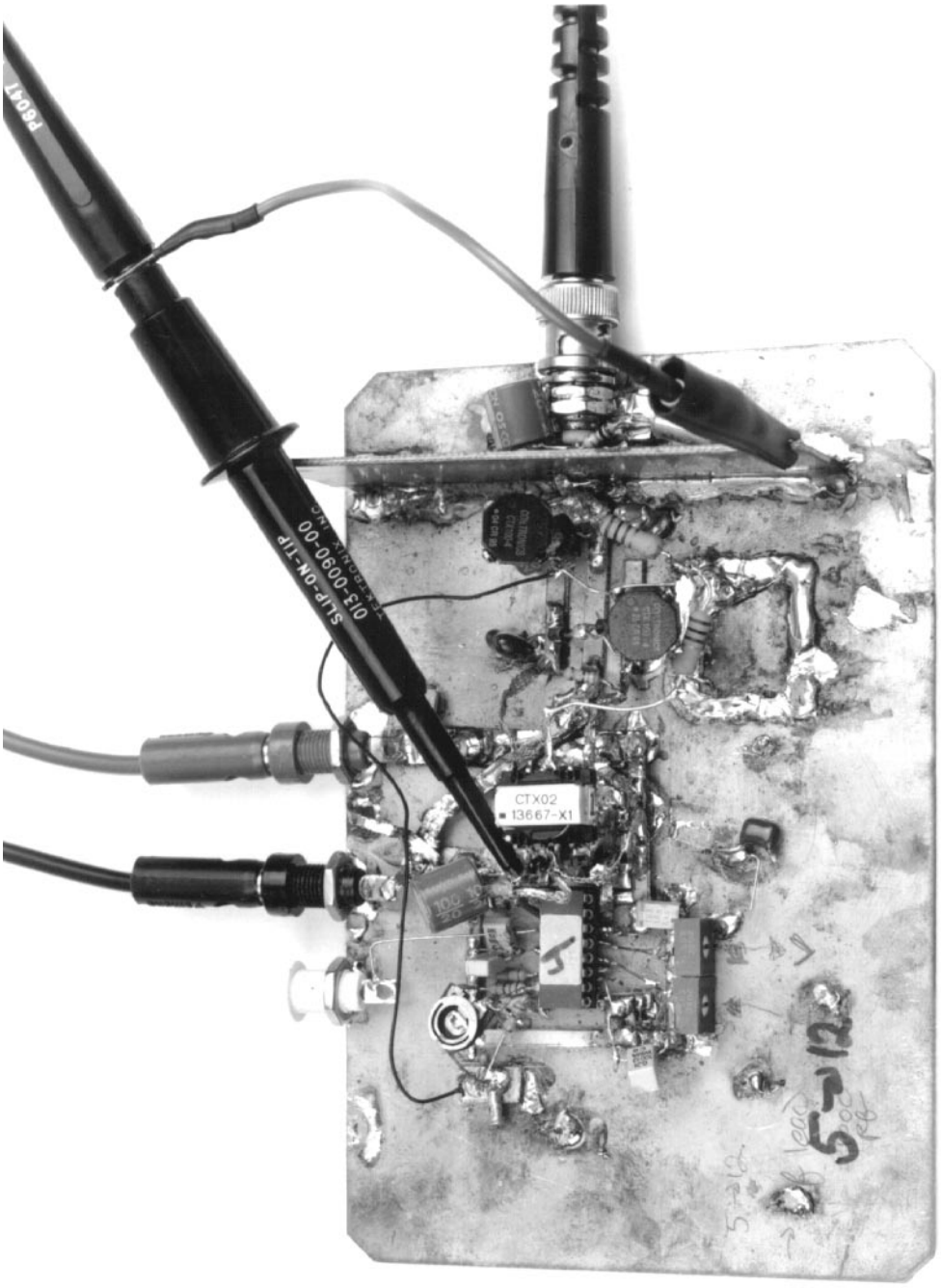


Figure C3. Poor Probing Technique. Trigger Probe Ground Lead Can Cause Ground Loop-Induced Artifacts to Appear in Display

Figure C4 shows results. A ground loop on the board between the probe ground strap and the ground referred cable shield causes apparent excessive ripple in the display. *Minimize the number of test connections to the circuit and avoid ground loops*.

Violating Coaxial Signal Transmission—Felony Case

In Figure C5, the coaxial cable used to transmit the circuit output noise to the amplifier-oscilloscope has been replaced with a probe. A short ground strap is employed as the probe's return. The error inducing trigger channel probe in the previous case has been eliminated; the 'scope is triggered by a noninvasive, isolated probe.[2] Figure C6 shows excessive display noise due to breakup of the coaxial signal environment. The probe's ground strap violates coaxial transmission and the signal is corrupted by RF. *Maintain coaxial connections in the noise signal monitoring path*.

Violating Coaxial Signal Transmission—Misdemeanor Case

Figure C7's probe connection also violates coaxial signal flow, but to a less offensive extent. The probe's ground strap is eliminated, replaced by a tip grounding attachment. Figure C8 shows better results over the preceding case, although signal corruption is still evident. *Maintain coaxial connections in the noise signal monitoring path*.

Proper Coaxial Connection Path

In Figure C9, a coaxial cable transmits the noise signal to the amplifier-oscilloscope combination. In theory, this affords the highest integrity cable signal transmission. Figure C10's trace shows this to be true. The former example's aberrations and excessive noise have disappeared. The switching residuals are now faintly outlined in the amplifier noise floor. *Maintain coaxial connections in the noise signal monitoring path*.

Direct Connection Path

A good way to verify there are no cable-based errors is to eliminate the cable. Figure C11's approach eliminates all cable between breadboard, amplifier and oscilloscope. Figure C12's presentation is indistinguishable from Figure C10, indicating no cable-introduced infidelity. *When results seem optimal, design an experiment to test them. When results seem poor, design an experiment to test them. When results are as expected, design an experiment to test them. When results are unexpected, design an experiment to test them*.

Test Lead Connections

In theory, attaching a voltmeter lead to the regulator's output should not introduce noise. Figure C13's increased noise reading contradicts the theory. The regulator's output impedance, albeit low, is not zero, especially as frequency scales up. The RF noise injected by the test lead works against the finite output impedance, producing the 200μV of noise indicated in the figure. If a voltmeter lead must be connected to the output during testing, it should be done through a 10kΩ-10μF filter. Such a network eliminates Figure C13's problem while introducing minimal error in the monitoring DVM. *Minimize the number of test lead connections to the circuit while checking noise. Prevent test leads from injecting RF into the test circuit*.

Note 2: To be discussed. Read on.

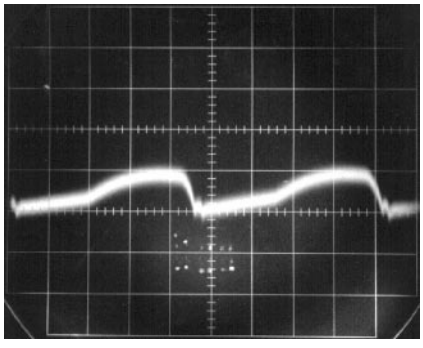


Figure C4. Apparent Excessive Ripple Results from Figure C3's Probe Misuse. Ground Loop on Board Introduces Serious Measurement Error

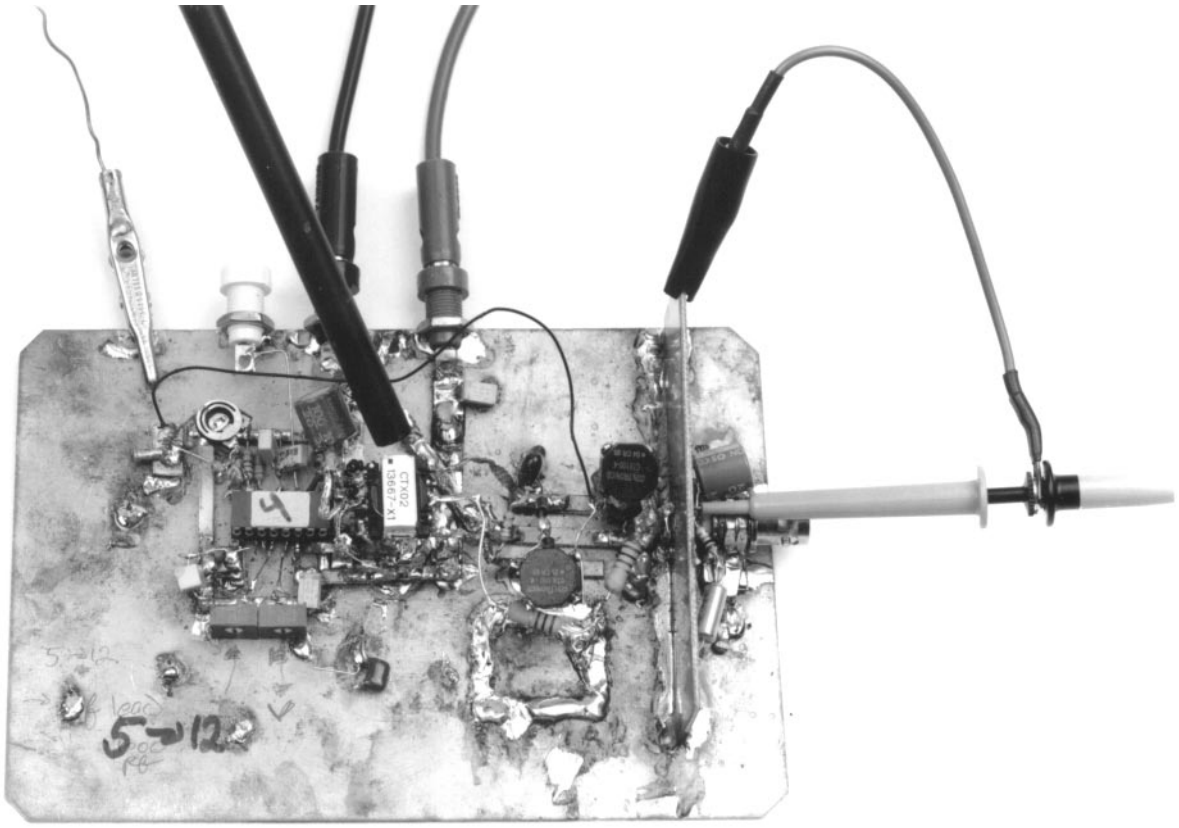


Figure C5. Floating Trigger Probe Eliminates Ground Loop, But Output Probe Ground Lead (Photo Upper Right) Violates Coaxial Signal Transmission

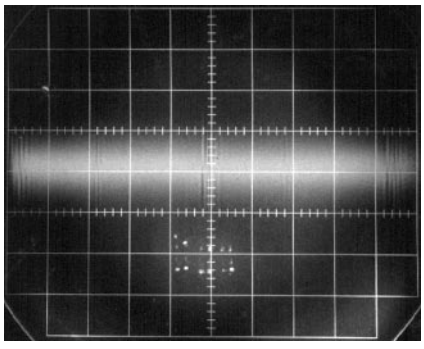


Figure C6. Signal Corruption Due to Figure C5's Noncoaxial Probe Connection

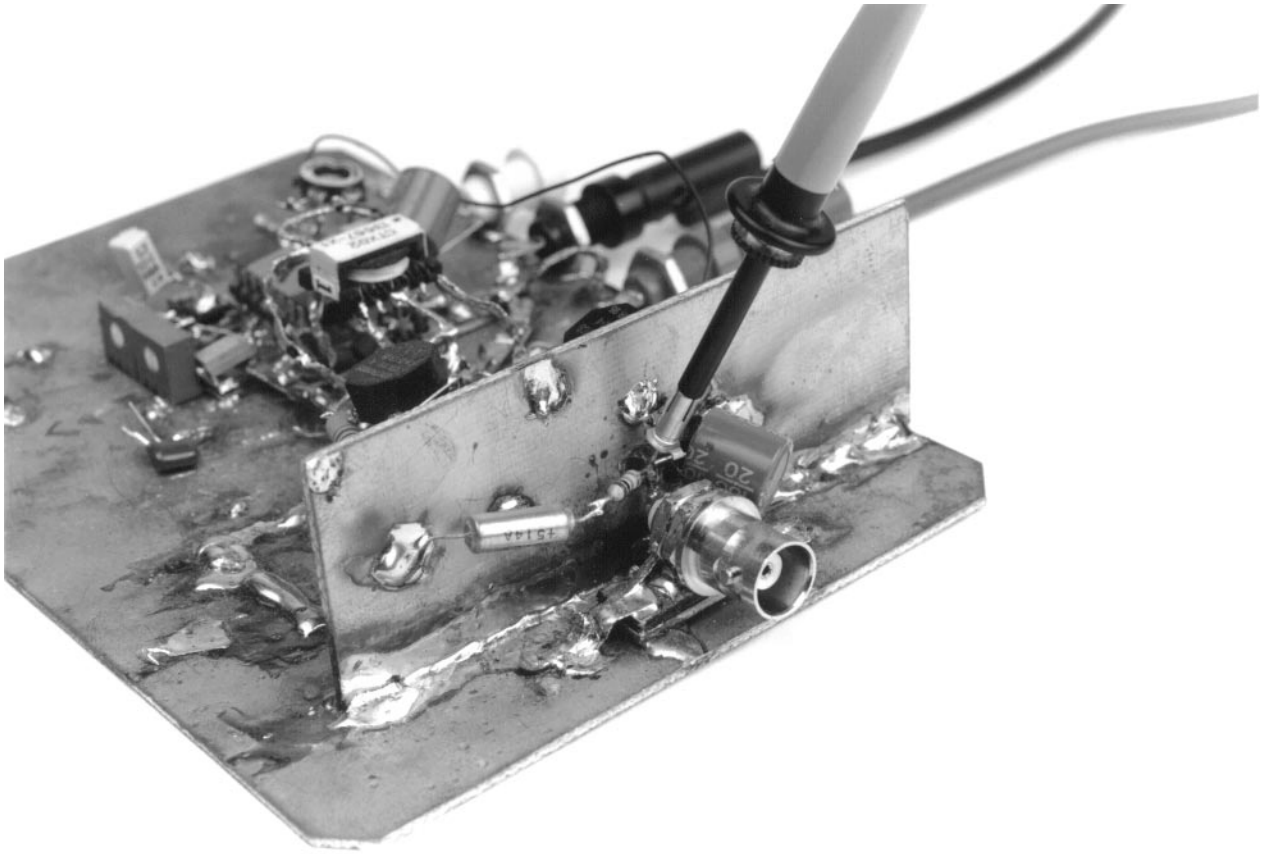


Figure C7. Probe with Tip Grounding Attachment Approximates Coaxial Connection

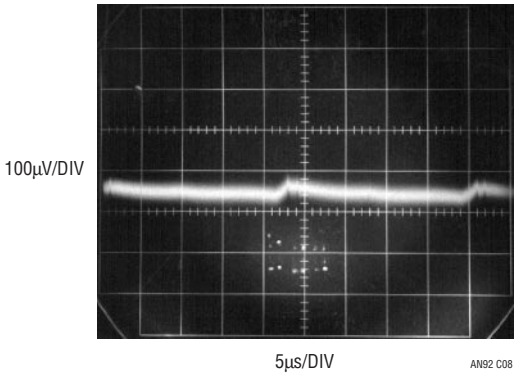


Figure C8. Probe with Tip Grounding Attachment Improves Results. Some Corruption Is Still Evident

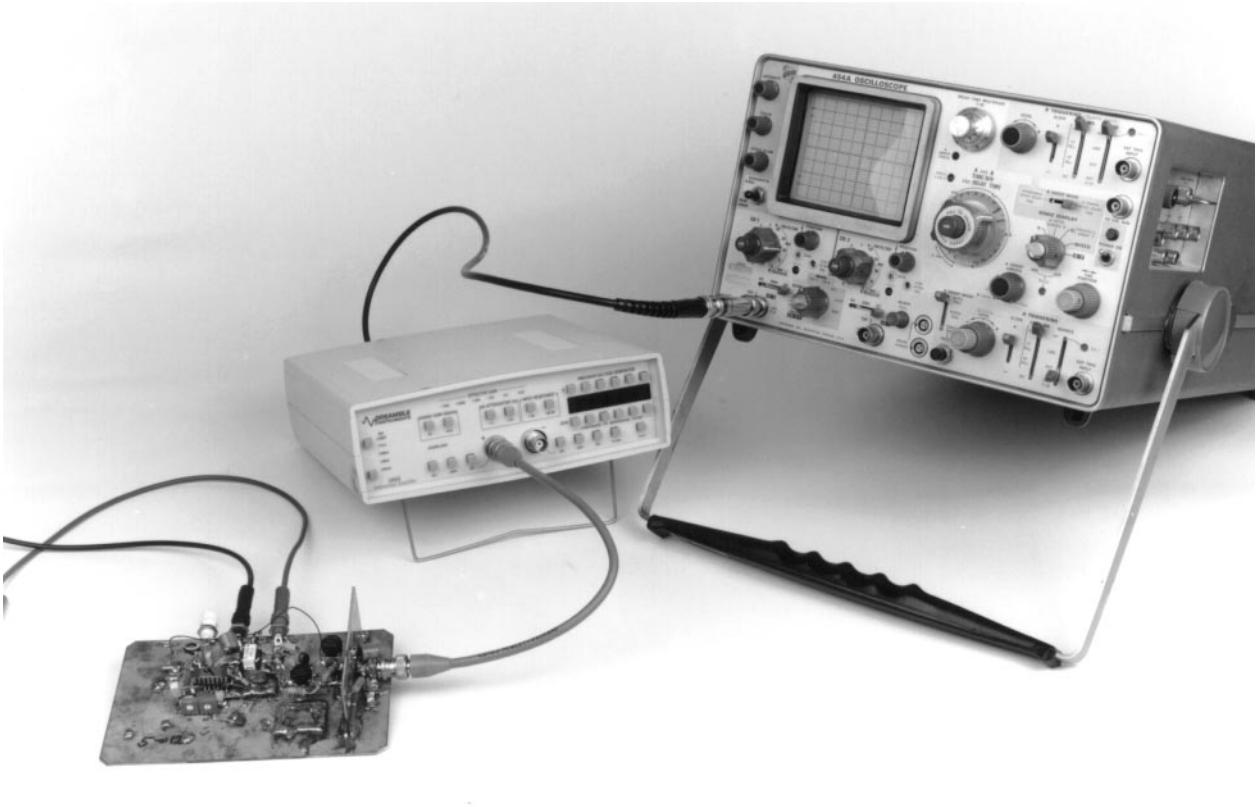


Figure C9. Coaxial Connection Theoretically Affords Highest Fidelity Signal Transmission

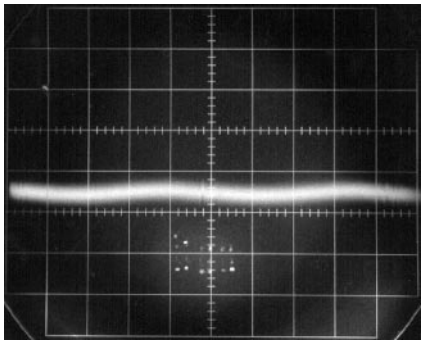


Figure C10. Life Agrees with Theory. Coaxial Signal Transmission Maintains Signal Integrity. Switching Residuals Are Faintly Outlined in Amplifier Noise

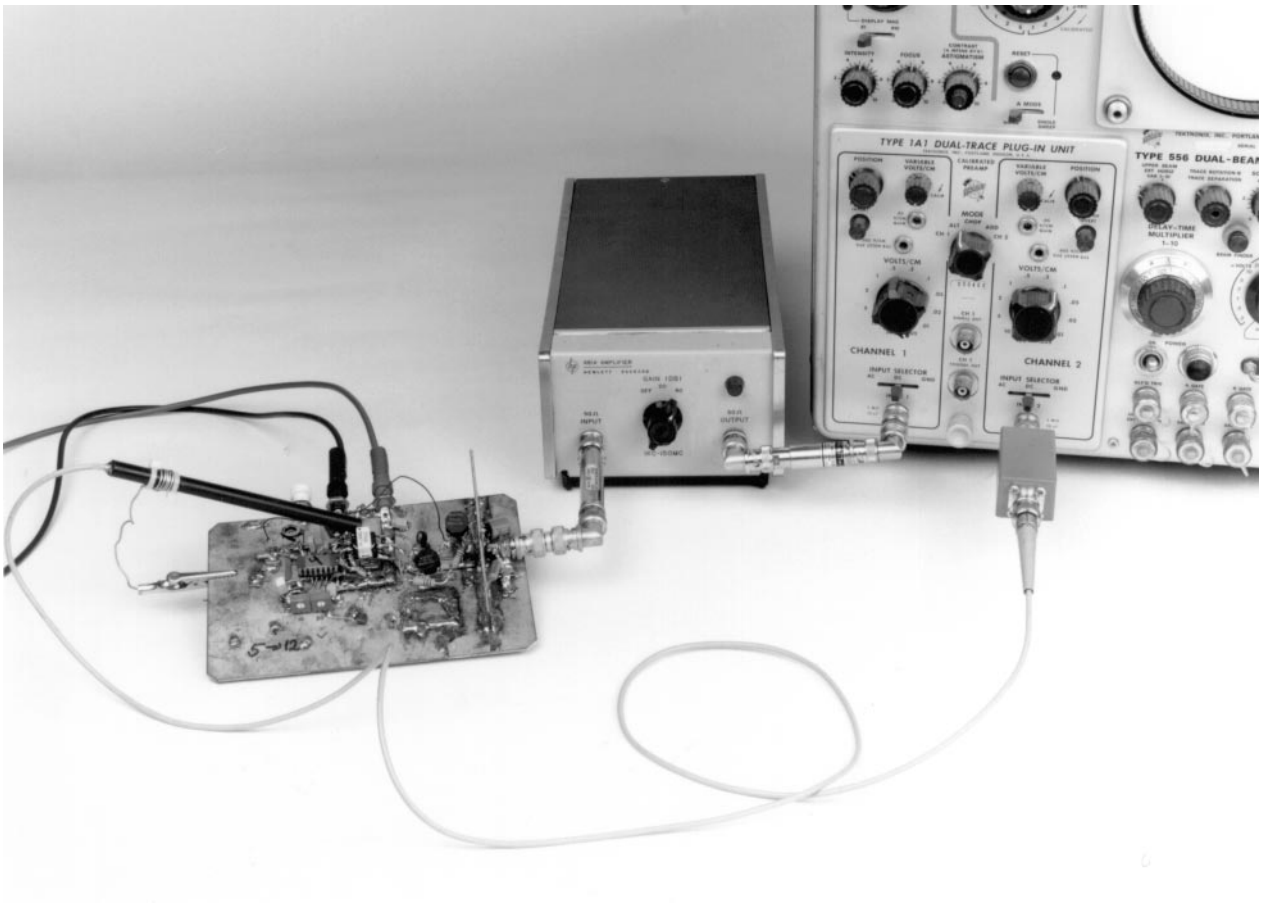


Figure C11. Direct Connection to Equipment Eliminates Possible Cable-Termination Parasitics, Providing Best Possible Signal Transmission

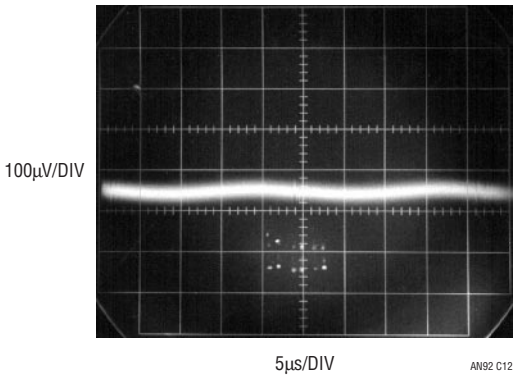


Figure C12. Direct Connection to Equipment Provides Identical Results to Cable-Termination Approach. Cable and Termination Are Therefore Acceptable

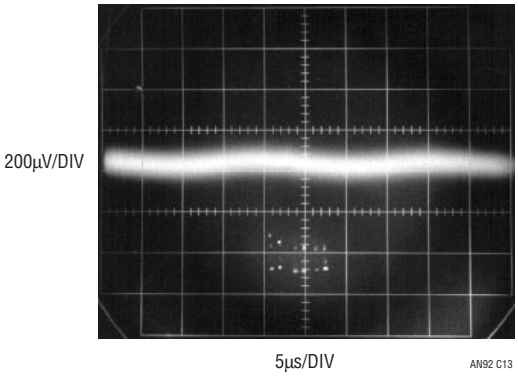


Figure C13. Voltmeter Lead Attached to Regulator Output Introduces RF Pickup, Multiplying Apparent Noise Floor

Isolated Trigger Probe

The text associated with Figure C5 somewhat cryptically alluded to an "isolated trigger probe." Figure C14 reveals this to be simply an RF choke terminated against ringing. The choke picks up residual radiated field, generating an isolated trigger signal. This arrangement furnishes a 'scope trigger signal with essentially no measurement corruption. The probe's physical form appears in Figure C15. For good results, the termination should be adjusted for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces Figure C16's output, which will cause poor 'scope triggering. Proper adjustment results in a more favorable output (Figure C17), characterized by minimal ringing and well-defined edges.

Trigger Probe Amplifier

The field around the switching magnetics is small and may not be adequate to reliably trigger some oscilloscopes. In such cases, Figure C18's trigger probe amplifier is useful. It uses an adaptive triggering scheme to compensate for variations in probe output amplitude. A stable 5V trigger output is maintained over a 50:1 probe output range. A1, operating at a gain of 100, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's trigger output, is unaffected by >50:1 signal amplitude variations. An X100 analog output is available at A1.

Figure C19 shows the circuit's digital output (Trace B) responding to the amplified probe signal at A1 (Trace A).

Figure C20 is a typical noise testing setup. It includes the breadboard, trigger probe, amplifier, oscilloscope and coaxial components.

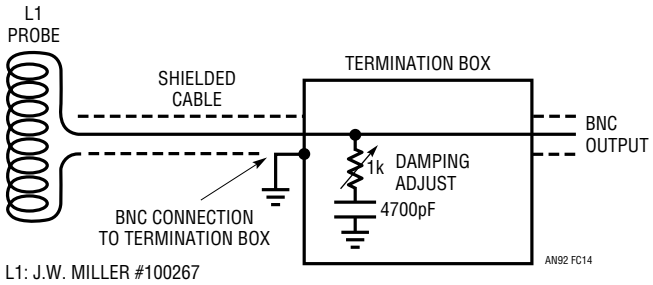


Figure C14. Simple Trigger Probe Eliminates Board Level Ground Loops. Termination Box Components Damp L1's Ringing Response

Figure C15. The Trigger Probe and Termination Box. Clip Lead Facilitates Mounting Probe, Is Electrically Neutral

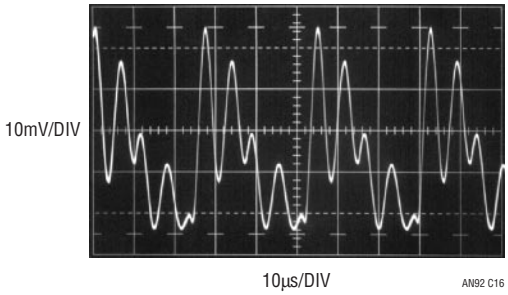


Figure C16. Misadjusted Termination Causes Inadequate Damping. Unstable Oscilloscope Triggering May Result

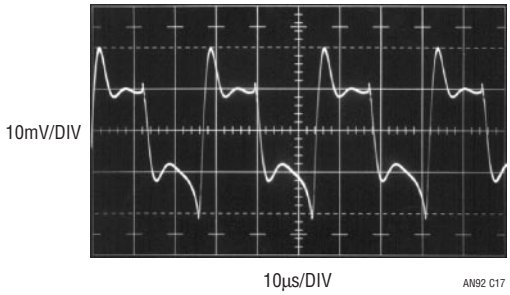


Figure C17. Properly Adjusted Termination Minimizes Ringing with Small Amplitude Penalty

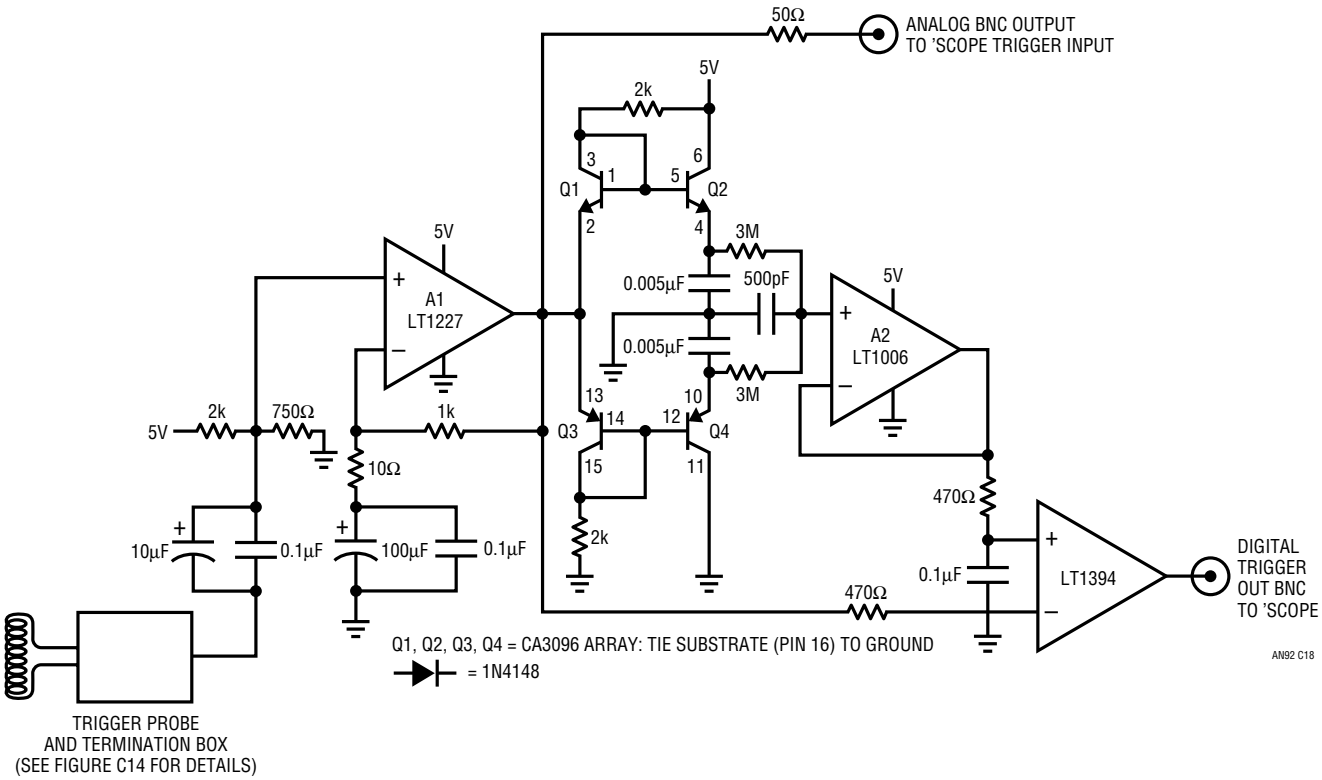


Figure C18. Trigger Probe Amplifier Has Analog and Digital Outputs. Adaptive Threshold Maintains Digital Output Over 50:1 Probe Signal Variations

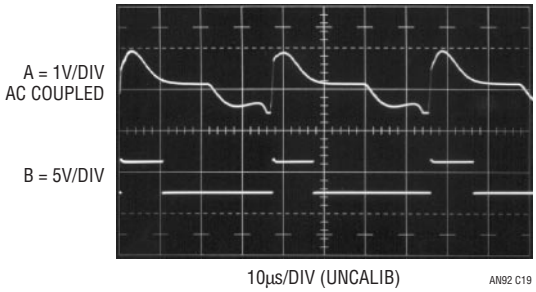


Figure C19. Trigger Probe Amplifier Analog (Trace A) and Digital (Trace B) Outputs

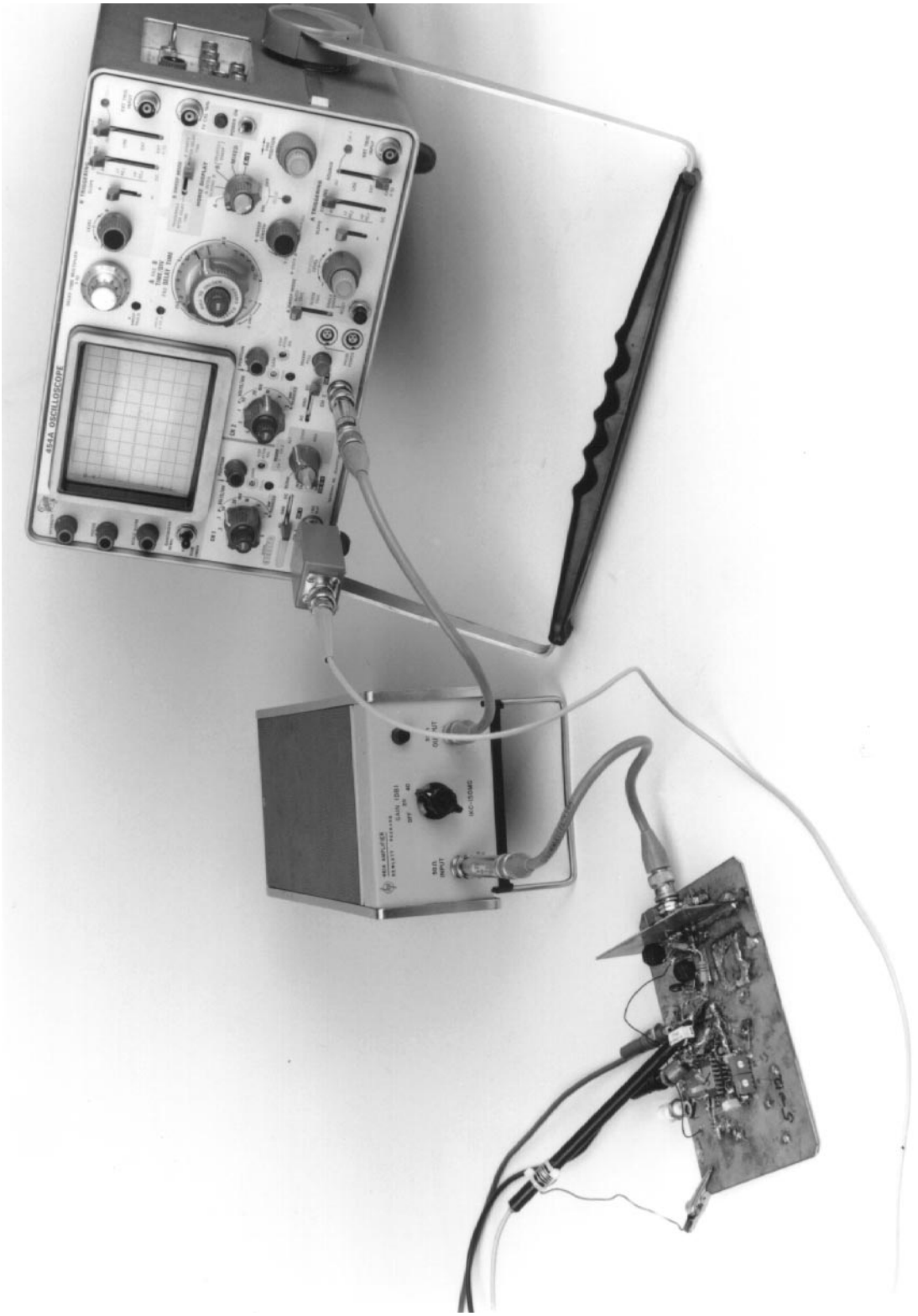


Figure C20. Typical Noise Test Setup Includes Trigger Probe, Amplifier, Oscilloscope and Coaxial Components

APPENDIX D

A SINGLE RAIL AMPLIFIER WITH TRUE ZERO VOLT OUTPUT SWING

Performance requirements necessitate analog output current monitors to swing within 100µV of zero. This is difficult because the circuits run from a single, positive rail. No single rail amplifier can swing this close to zero while maintaining accurate outputs. Figure D1's power supply bootstrapping scheme achieves the desired characteristics with minimal component addition.

A1, a chopper stabilized amplifier, has a clock output. This output switches Q1, providing drive to the diode-capacitor charge pump. The charge pump output feeds A1's V^- terminal, pulling it below zero, permitting output swing to (and below) ground. If desired, negative output excursion can be limited by either clamp option shown.

Reliable start-up of this bootstrapped power supply scheme is a valid concern, warranting investigation. In Figure D2, the amplifier's V^- pin (Trace C) initially rises at supply turn-on (Trace A) but heads negative when amplifier clocking (Trace B) commences at about midscreen.

The circuit provides a simple way to obtain output swing to zero volts, permitting a true "live at zero" output.

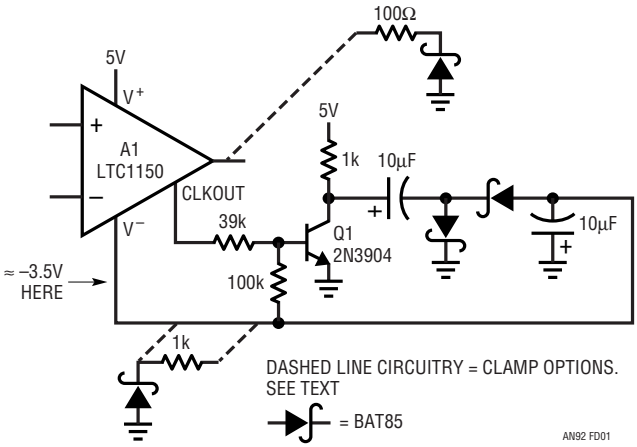


Figure D1. Single Rail Powered Amplifier Has True Zero Volt Output Swing. A1's Clock Output Switches Q1, Driving Diode-Capacitor Charge Pump. A1's V^- Pin Assumes Negative Voltage, Permitting Zero (and Below) Volt Output Swing

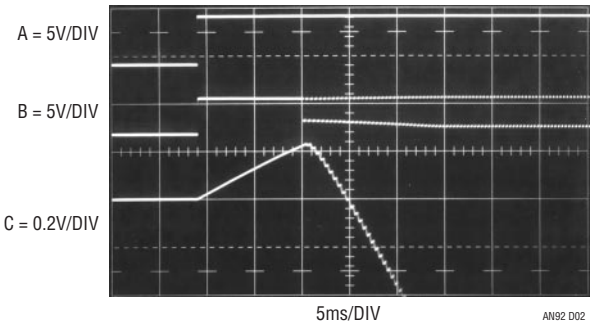


Figure D2. Amplifier Bootstrapped Supply Start-Up. Amplifier V^- Pin (Trace C) Initially Rises Positive at 5V Supply (Trace A) Turn-On. When Amplifier Internal Clock Starts (Trace B, 5th Vertical Division), Charge Pump Activates, Pulling V^- Pin Negative

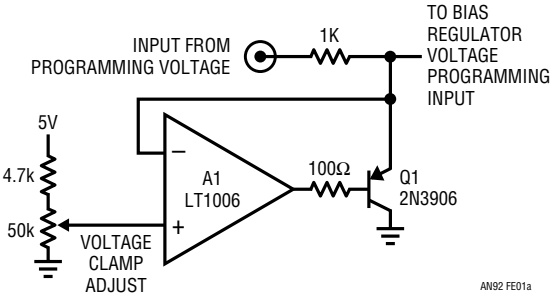
APPENDIX E

APD PROTECTION CIRCUITS

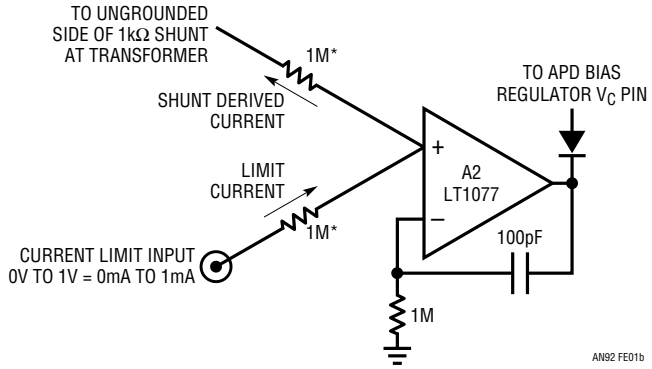
APD receiver modules are electrically delicate and expensive devices. Because of this, Figure E1's protection circuits may be of interest. They are designed to protect the APD module from bias programming overvoltage error (Figure E1a), excessive current (E1b) or destructive voltage (Figure E1c). In Figure E1a, Q1 is normally off and programming voltage passes to the bias regulator voltage programming input. Abnormally high inputs, defined by the potentiometer's setting, cause A1 to swing low, biasing Q1 and closing A1's feedback loop. This causes Q1's emitter to clamp at the potentiometer wiper's voltage, safely limiting the bias regulator's programming input.

Figure E1b is an APD current limiter. This particular circuit is designed for use with "low side" shunts in transformer coupled APD supplies, such as text Figure 9, although the technique is generally applicable. As long as the shunt current's absolute value is below the current limit point, A2 is saturated high and the associated APD bias regulator functions normally. Shunt overcurrent forces A2's output lower, pulling the regulator's control pin (V_C) lower and limiting current. The 100pF-1MΩ combination stabilizes A2 and the bias regulator assumes the characteristics of a current source.

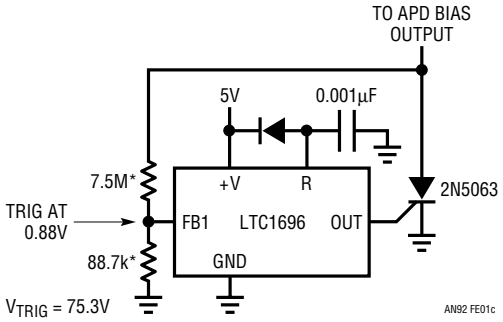
Figure E1c is an overvoltage crowbar. It is intended as the last line of defense against uncontrolled APD bias supply high voltage outputs. Normally, the LTC1696 crowbar IC is below its 0.88V trigger threshold and the SCR is off. If the APD bias rises too high the LTC1696 triggers, firing the SCR. SCR turn-on "crowbars" the APD bias line, arresting the high voltage and maintaining a short across the line via its latch characteristic. If the APD bias supply has significant output impedance, prolonged SCR loading is not deleterious; if not, the bias supply should be fused.



(E1a) Programming Voltage Clamp



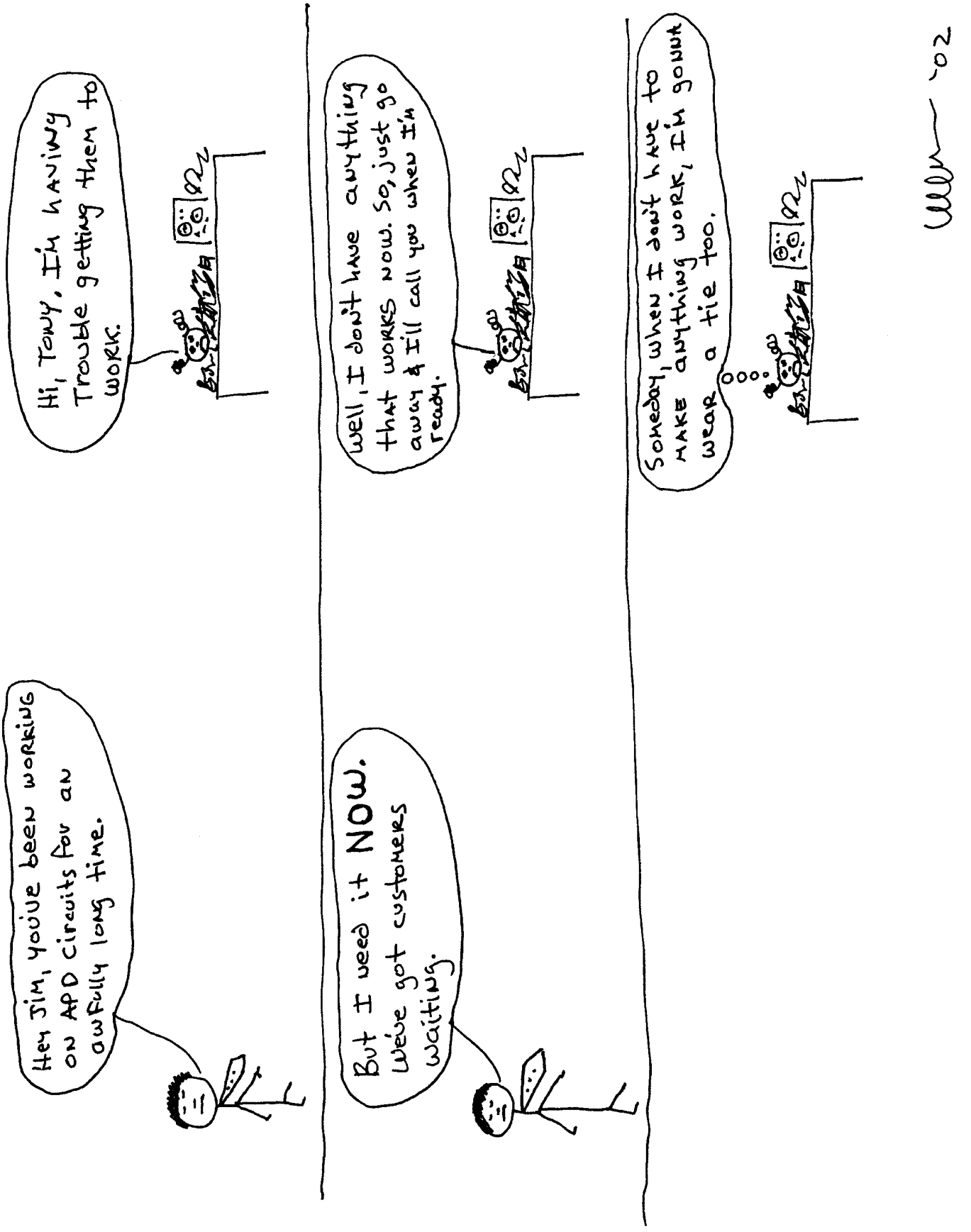
(E1b) Current Limiter



(E1c) Bias Voltage Crowbar

* = 1% METAL FILM RESISTOR
= 1N4148

Figure E1. Protection Circuits Prevent APD Destruction Due to Hardware or Software Failures. Options Include Programming Voltage Clamp (Figure E1a), Current Limiter (Figure E1b) and Bias Voltage Crowbar (Figure E1c)



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