Deska „Nastavitelný čítač“

pro praktikum z číslicové elektroniky

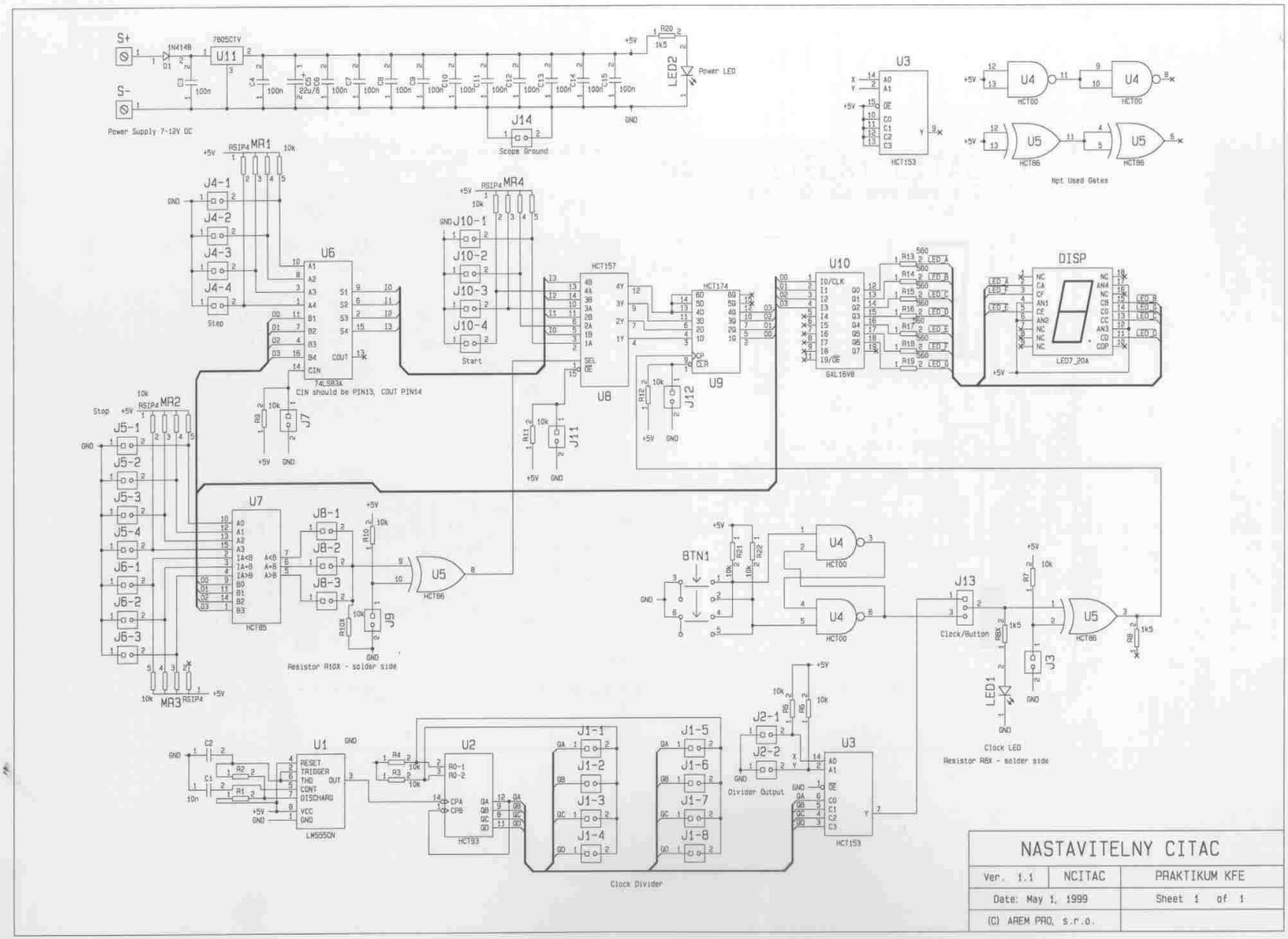
Základ desky pro praktikum z číslicové elektroniky tvoří čtyřbitový synchronní čítač, který se skládá z registru stavu čítače (U9 74174), z aritmetického obvodu (U6 7483) pro výpočet příštího stavu, komparátoru (U7 7485) pro vyhodnocení podmínky pro přednastavení (preset) čítače a multiplexoru (U8 74157) pro řízení nastavení výchozího stavu čítače. Takto koncipovaný čítač umožňuje čítat vpřed i vzad o krok nastavený konstantou aritmetického obvodu pro výpočet příštího stavu (odčítaní se provádí volbou záporného čísla jako druhý doplněk), nastavit počáteční i koncovou hodnotu čítání. Stav čítače je signalizován sedmisegmentovým displejem připojeným přes dekodér (U10 GALl6V8) na výstup čítače. Zdrojem hodinového signálu může být jednak tlačítko (BTN1) připojené přes RS klopný obvod (U4 7400) pro vyloučení zákmitů při spínání, jednak generátor obdélníkového signálu. Ten se skládá z generátoru obdélníkového signálu realizovaného univerzálním časovačem (U1 NE555) s periodou 200ms, na který je připojen asynchronní děliče (U2 7493). Ten spolu s multiplexorem (U3 74153) umožňuje generovat různé kmitočty dle nastavení dělicího poměru. Deska má vlastní stabilizátor napětí (U11 7805) s ochrannou sériovou diodou proti přepólování a lze jej napájet ze zdroje stejnosměrného napětí v rozsahu od 8V do 12V.

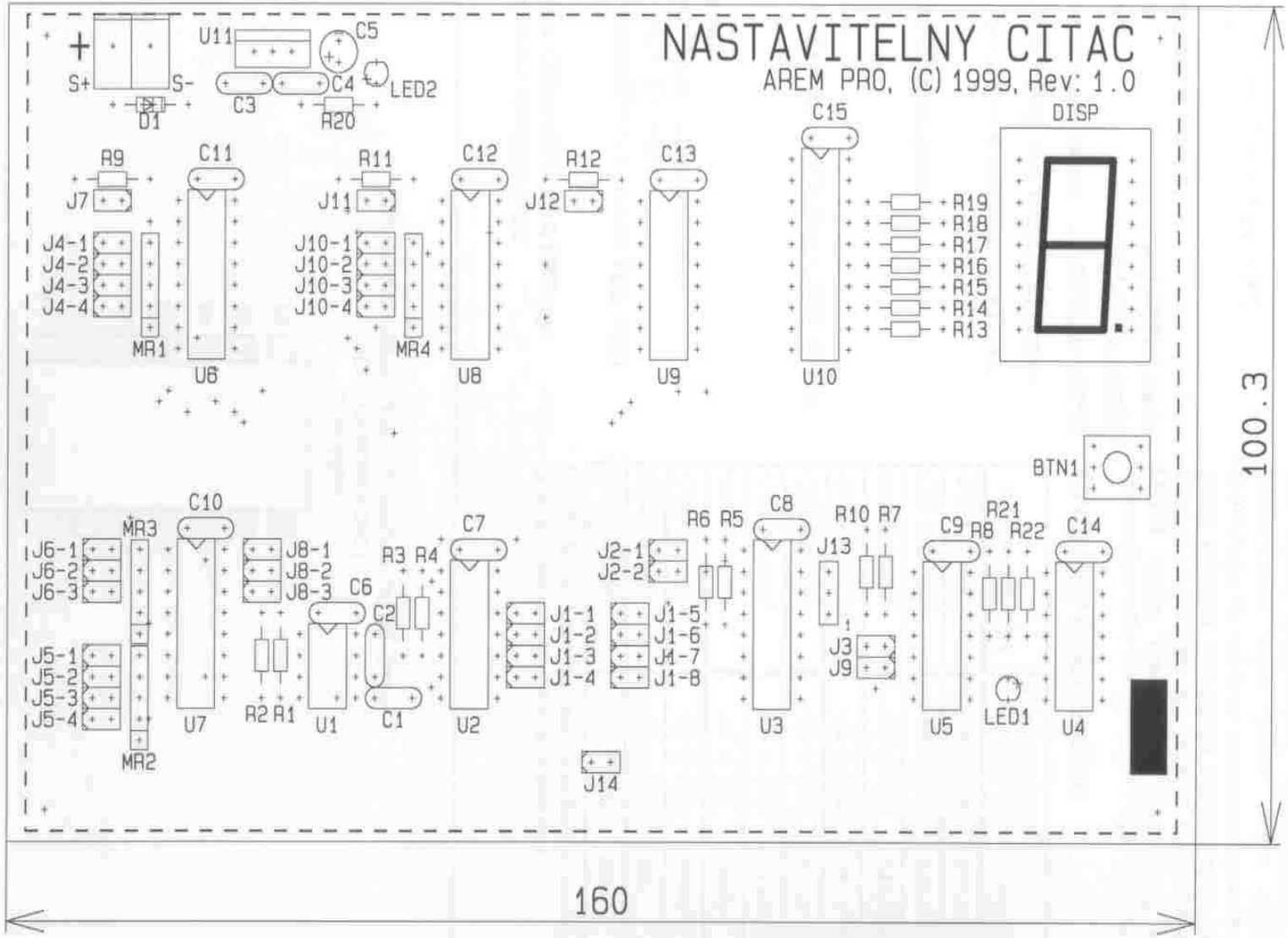
Úloha praktika je zaměřena na detailní pochopení funkce synchronního čítače a správné nastavení jeho „jumperů“ tak, aby vykonával funkci stanovenou vedoucím praktika. Možnosti nastavení jsou následující:

- nastavení správných podmínek pro děličku kmitočtu hodinového signálu
- nastavení dle požadavku na řídící hranu hodinového signálu
- nastavení periody čítače - 400ms až 3.2s
- nastavení výchozí hodnoty čítače - 0 až 9 (popř. 15)
- nastavení koncové hodnoty čítače - 0 až 9 (popř. 15)
- nastavení kroku čítače - 0 až 9 (popř. 15), resp. druhý doplněk pro odčítaní
- nastavení správných podmínek pro funkci obvodů
- nastavení správné polarity signálu pro řízení multiplexoru přednastavení

Deska výše popsaného obvodu je vyrobena jako prokovený dvouvrstvý plošný spoj s nepájivou maskou. Dále je opatřena potiskem s popisem součástek a nastavovacích prvků. Deska je vmontována do vaničky z umělé hmoty, aby se vyloučilo její poškození z důvodu zkratu na spodní straně desky během provádění praktika. K vlastní desce jsou kromě jejího schématu jako příslušenství přiloženy katalogové listy použitých obvodů.

v1 M.Kropík 1998
v2 J.Blažej, 2005


S+
S-
Power Supply 7-12V DC
1N4148
7805CTV
U11
LED2
Power LED
J14
Scope Ground
U3
HCT153
U4
HCT00
U5
HCT86
Not Used Gates
MR1
MR2
MR3
MR4
RSIP4
Step
Start
Stop
U6
74LS83A
CIN should be PIN13, COUT PIN14
U7
HCT85
U8
HCT157
U9
HCT174
U10
GAL16V8
DISP
LED7_20A
Resistor R10X - solder side
BTN1
Clock/Button
LED1
Clock LED
Resistor R8X - solder side
U1
LM555CN
U2
HCT93
Divider Output
Clock Divider
NASTAVITELNY CITAC
Ver. 1.1
NCITAC
PRAKTIKUM KFE
Date: May 1, 1999
Sheet 1 of 1
(C) AREM PRO, s.r.o.


NASTAVITELNY CITAC
AREM PRO, (C) 1999, Rev: 1.0
S+
S-
D1
U11
C5
C3
C4
LED2
R20
C15
DISP
R9
C11
R11
C12
R12
C13
J7
J11
J12
J4-1
J4-2
J4-3
J4-4
J10-1
J10-2
J10-3
J10-4
MR1
MR4
U6
U8
U9
U10
R19
R18
R17
R16
R15
R14
R13
BTN1
C10
MR3
C7
R6
R5
C8
R10
R7
C9
R8
R21
R22
C14
J6-1
J6-2
J6-3
J8-1
J8-2
J8-3
R3
R4
C6
C2
J2-1
J2-2
J13
J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
J1-7
J1-8
J5-1
J5-2
J5-3
J5-4
MR2
U7
R2
R1
U1
C1
U2
U3
U5
LED1
U4
J3
J9
J14
100.3
160

CD54HC00, CD54HCT00, CD74HC00, CD74HCT00

High Speed CMOS Logic Quad 2-Input NAND Gate

Data sheet acquired from Harris Semiconductor
SCHS116

January 1998

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 7ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **Alternate Source is Philips/Signetics**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**
- **Related Literature**
  - **CD54HC00F3A and CD54HCT00F3A Military Data Sheet, Document Number 3753**

Description

The Harris CD54HC00, CD54HCT00, CD74HC00 and CD74HCT00 logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally pin compatible with the standard 74LS logic family.

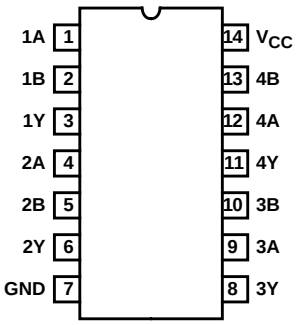
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC00E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT00E	-55 to 125	14 Ld PDIP	E14.3
CD74HC00M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT00M	-55 to 125	14 Ld SOIC	M14.15
CD54HC00F	-55 to 125	14 Ld CERDIP	F14.3
CD54HCT00F	-55 to 125	14 Ld CERDIP	F14.3
CD54HC00W	-55 to 125	Wafer	
CD54HCT00W	-55 to 125	Wafer	
CD54HC00H	-55 to 125	Die	
CD54HCT00H	-55 to 125	Die	

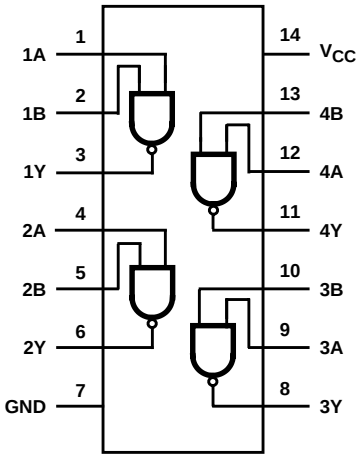
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD54HC00, CD54HCT00, CD74HC00, CD74HCT00
(PDIP, CERDIP, SOIC)
TOP VIEW



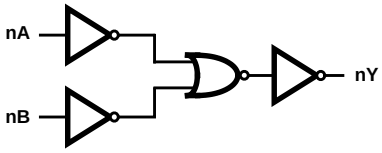
Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Logic Symbol



CD54HCT32, CD74HC32, CD74HCT32

High Speed CMOS Logic Quad 2-Input OR Gate

Data sheet acquired from Harris Semiconductor
SCHS274

September 1997

Features

- **Typical Propagation Delay: 7ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**
- **Related Literature**
  - **CD54HC32F3A and CD54HCT32F3A Military Data Sheet, Document Number 3765**

Description

The Harris CD74HC32, CD74HCT32 contain four 2-input OR gates in one package. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally pin compatible with the standard 74LS logic family.

Ordering Information

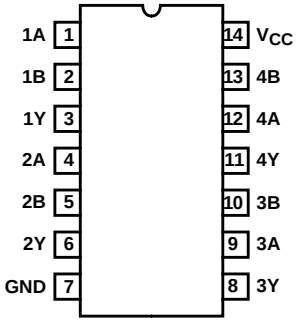
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC32E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT32E	-55 to 125	14 Ld PDIP	E14.3
CD74HC32M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT32M	-55 to 125	14 Ld SOIC	M14.15
CD54HCT32F	-55 to 125	14 Ld CERDIP	F14.3
CD54HC32W	-55 to 125	Wafer	

NOTES:

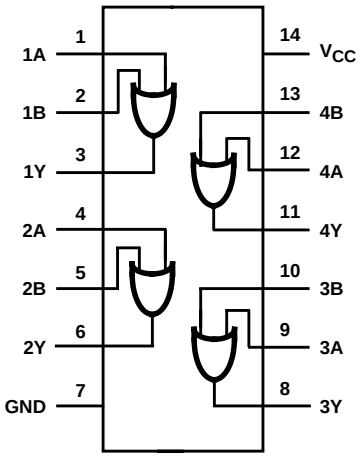
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD54HCT32, CD74HC32, CD74HCT32
(PDIP, CERDIP, SOIC)
TOP VIEW



Functional Diagram

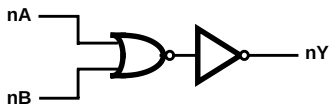


TRUTH TABLE

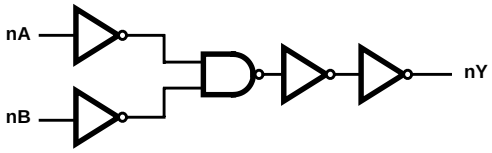
INPUTS		OUTPUT
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	H

NOTE: H = High Voltage Level, L = Low Voltage Level

HC Logic Symbol



HCT Logic Symbol



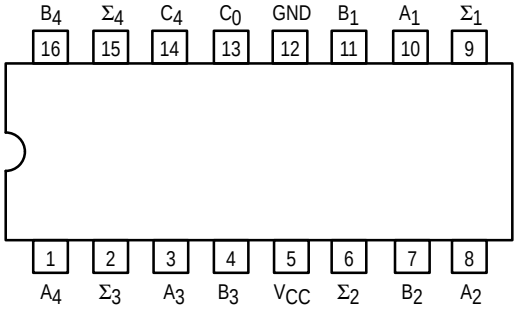
MOTOROLA

SN54/74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS83A is a high-speed 4-Bit binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4, B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1-\Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

CONNECTION DIAGRAM DIP (TOP VIEW)



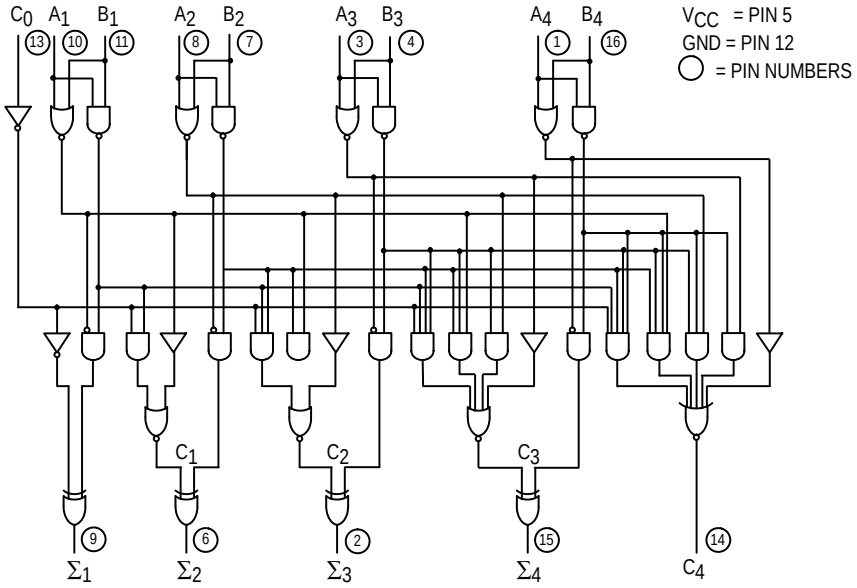
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_1-A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)	10 U.L.	5 (2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5 (2.5) U.L.

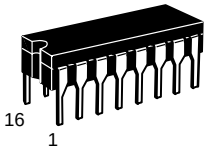
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

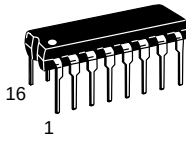


4-BIT BINARY FULL ADDER WITH FAST CARRY

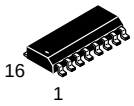
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

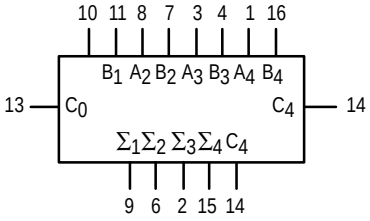


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_4) outputs.

$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

C (n–1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS136

August 1997

CD74HC85, CD74HCT85

High Speed CMOS Logic 4-Bit Magnitude Comparator

Features

- **Buffered Inputs and Outputs**
- **Typical Propagation Delay: 13ns (Data to Output at V_{CC} = 5V, C_L = 15pF, T_A = 25^oC**
- **Serial or Parallel Expansion Without External Gating**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The CD74HC85 and CD74HCT85 are high speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs (A > B, A < B, and A = B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B_3 are the most significant bits.

The devices are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially expanded application. The parallel expansion scheme is described by the last three entries in the truth table.

Ordering Information

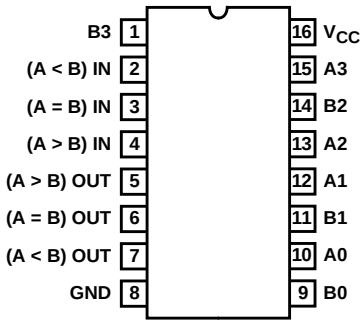
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74HC85E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT85E	-55 to 125	16 Ld PDIP	E16.3
CD74HC85M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT85M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

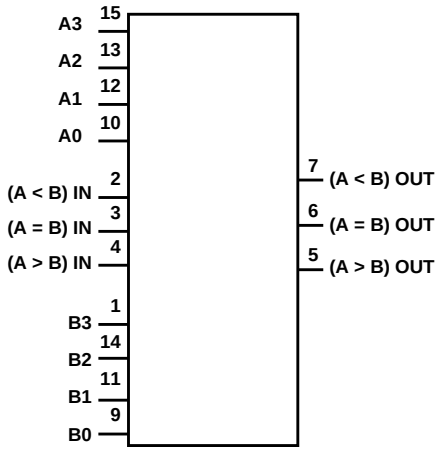
Pinout

CD74HC85, CD74HCT85
(PDIP, SOIC)
TOP VIEW



File Number **1770.1**

Functional Diagram



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**A > B**	**A < B**	**A = B**	**A > B**	**A < B**	**A = B**
SINGLE DEVICE OR SERIES CASCADING									
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 >B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
PARALLEL CASCADING									
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2S	A1 = B1	A0 = B0	L	L	L	H	H	L

NOTE: H = High Voltage Level, L = Low Voltage, Level, X = Don’t Care

Data sheet acquired from Harris Semiconductor
SCHS137

CD74HC86, CD74HCT86

High Speed CMOS Logic Quad 2-Input EXCLUSIVE OR Gate

August 1997

Features

- **Typical Propagation Delay: 9ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Applications

- **Logical Comparators**
- **Parity Generators and Checkers**
- **Adders and Subtractors**

Description

The Harris CD74HC86, CD74HCT86 contain four independent EXCLUSIVE OR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE OR function. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally pin compatible with the standard 74LS logic family.

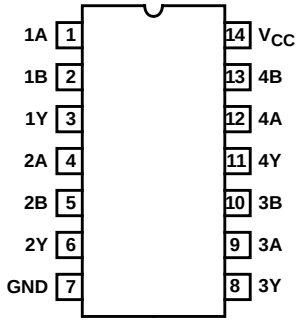
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC86E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT86E	-55 to 125	14 Ld PDIP	E14.3
CD74HC86M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT86M	-55 to 125	14 Ld SOIC	M14.15
CD54HC86W	-55 to 125	Wafer	
CD54HCT86W	-55 to 125	Wafer	
CD54HC86H	-55 to 125	Die	

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

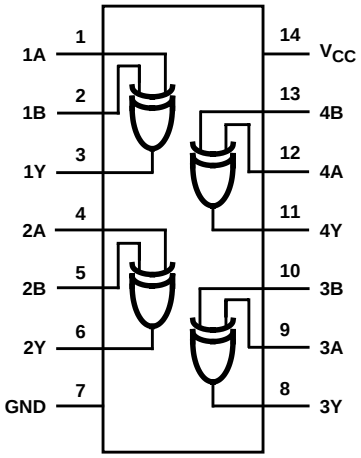
CD74HC86, CD74HCT86
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1644.1**

Functional Diagram

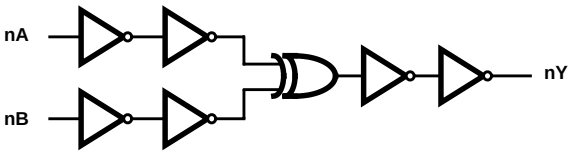


TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level

Logic Symbol



TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS138

CD74HC93, CD74HCT93

High Speed CMOS Logic 4-Bit Binary Ripple Counter

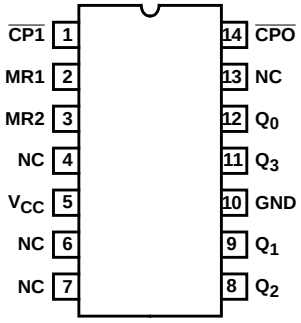
August 1997

Features

- **Can Be Configured to Divide By 2, 8, and 16**
- **Asynchronous Master Reset**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD74HC93, CD74HCT93
(PDIP, SOIC)
TOP VIEW



Description

The Harris CD74HC93 and CD74HCT93 are high speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two-section and a divid- by-eight-section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to innate state changes of the counter on the HIGH to LOW clock transition. Sate changes of the Qn outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR1 and MR2 is provided which overrides both clocks and resets (clears) all flip-flops.

Because the output from the divide by two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output Q0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q0, Q1, Q2, and Q3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CD74HC93E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT93E	-55 to 125	14 Ld PDIP	E14.3
CD74HC93M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT93M	-55 to 125	14 Ld SOIC	M14.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1849.1**

TRUTH TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: H = High Voltage Level, L = Low Voltage Level

MODE SELECTION

RESET OUTPUTS		OUTPUTS			
MR1	MR2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count	Count	Count	Count
H	L				
L	L				

NOTE: H = High Voltage Level, L = Low Voltage Level

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS151

September 1997

CD74HC153, CD74HCT153

High Speed CMOS Logic Dual 4-Input Multiplexer

Features

- **Common Select Inputs**
- **Separate Enable Inputs**
- **Buffered inputs and Outputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The Harris CD74HC153 and CD74HCT153 are dual 4 to line selector/multiplexers which select one of 4 to 1 line selector/multiplexers which select one of four sources for each section by the common select inputs, S0 and S1. When the enable inputs ($1\overline{E}$, $2\overline{E}$) are HIGH, the outputs are in the LOW state.

Ordering Information

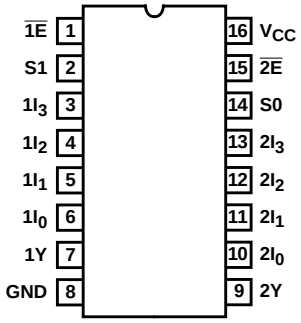
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CD74HC153E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT153E	-55 to 125	16 Ld PDIP	E16.3
CD74HC153M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT153M	-55 to 125	16 Ld SOIC	M16.15
CD54HC153W	-55 to 125	Wafer	

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

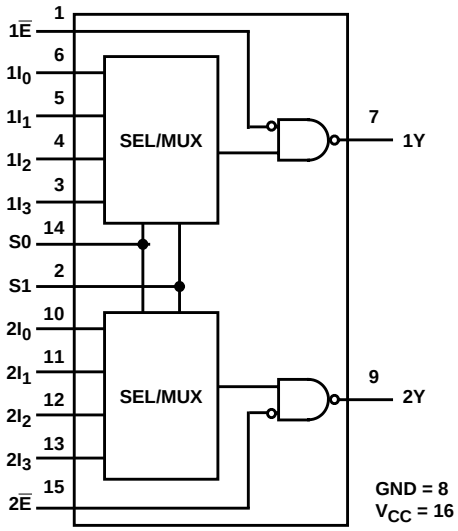
CD74HC153, CD74HCT153
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1774.1**

Functional Diagram



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE	OUTPUT
S1	S0	I0	I_1	I_2	I_3	$\overline{E}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTE:
Select inputs S1 and S0 are common to both sections.
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS153

CD74HC157, CD74HCT157, CD74HC158, CD74HCT158

High Speed CMOS Logic Quad 2-Input Multiplexers

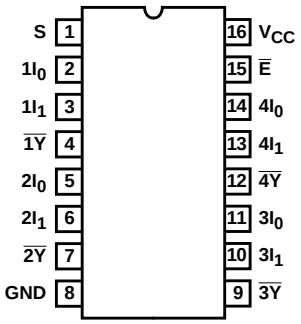
September 1997

Features

- Common Select Inputs
- Separate Enable Inputs
- Buffered inputs and Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^{o}C$ to $125^{o}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Pinout

CD74HC157, CD74HCT157, CD74HC158, CD74HCT158
(PDIP, SOIC)
TOP VIEW



File Number **1642.2**

Description

The Harris CD74HC157, CD74HCT157, CD74HC158 and CD74HCT158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active Low. When ($\overline{E}$) is High, all of the outputs in the 158, the inverting type, ($\overline{1Y}$-$\overline{4Y}$) are forced High and in the 157, the non-inverting type, all of the outputs ($\overline{1Y}$-$\overline{4Y}$) are forced Low, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

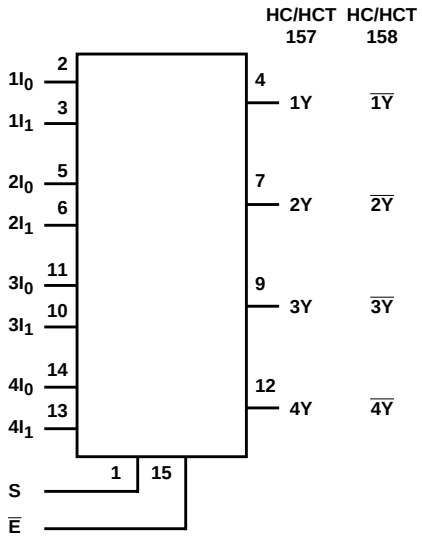
Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CD74HC157E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT157E	-55 to 125	16 Ld PDIP	E16.3
CD74HC158E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT158E	-55 to 125	16 Ld PDIP	E16.3
CD74HC157M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT157M	-55 to 125	16 Ld SOIC	M16.15
CD74HC158M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Functional Diagram



TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT	
				157	158
$\overline{E}$	S	I0	I1	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS159

August 1997

CD74HC174, CD74HCT174

High Speed CMOS Logic Hex D-Type Flip-Flop with Reset

Features

- **Buffered Positive Edge Triggered Clock**
- **Asynchronous Common Reset**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The Harris CD74HC174 and CD74HCT174 are edge triggered flip-flops which utilize silicon gate CMOS circuitry to implement D-type flip-flops. They possess low power and speeds comparable to low power Schottky TTL circuits. The devices contain six master-slave flip-flops with a common clock and common reset. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The $\overline{MR}$ input, when low, sets all outputs to a low state.

Each output can drive ten low power Schottky TTL equivalent loads. The CD74HCT174 is functional as well as, pin compatible to the 74LS174.

Ordering Information

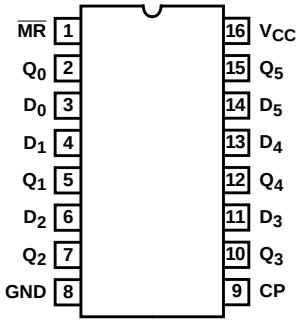
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CD74HC174E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT174E	-55 to 125	16 Ld PDIP	E16.3
CD74HC174M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT174M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT174W	-55 to 125	Wafer	

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

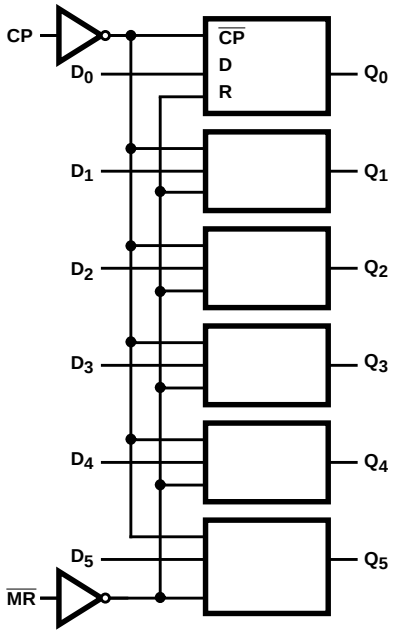
CD74HC174, CD74HCT174
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1608.1**

Functional Diagram

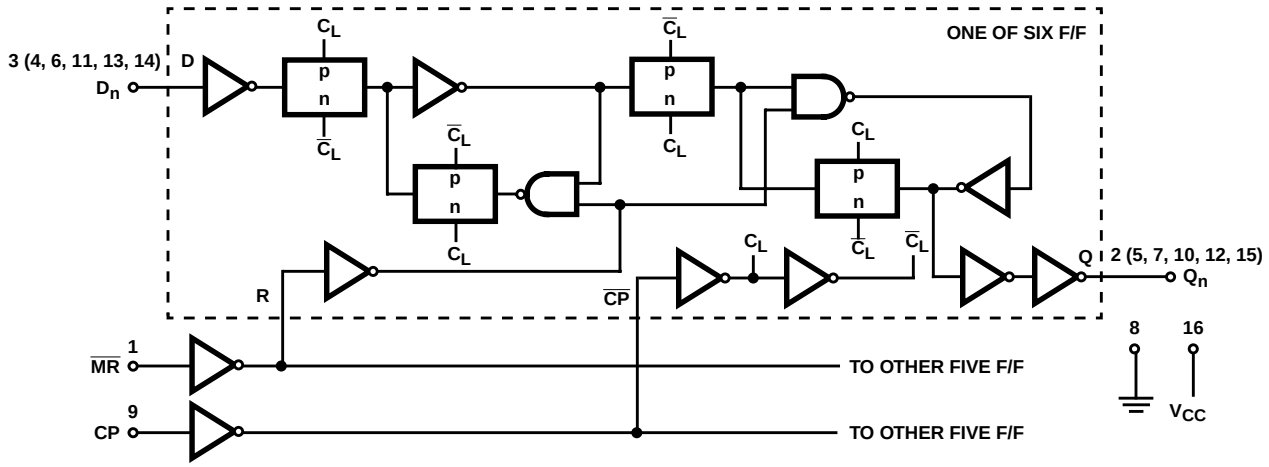


TRUTH TABLE

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA D_n	Q_n
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Irrelevant, ↑ = Transition from Low to High Level, Q_0 = Level Before the Indicated Steady-State Input Conditions Were Established

Logic Diagram



GAL16V8

High Performance E²CMOS PLD
Generic Array Logic™

Lead-Free Package Options Available!

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 3.5 ns Maximum Propagation Delay**
  - **— Fmax = 250 MHz**
  - **— 3.0 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
  - **— 45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **LEAD-FREE PACKAGE OPTIONS**

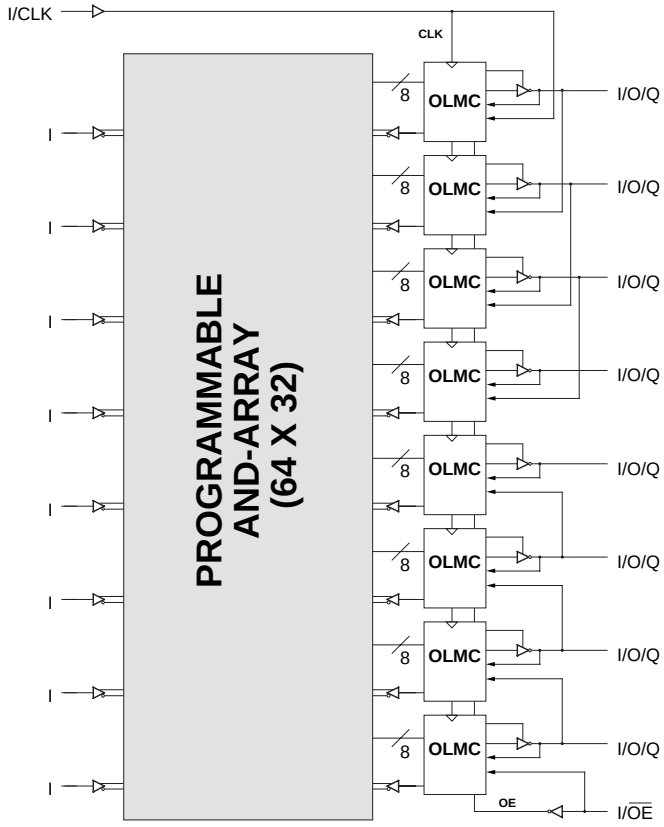
Description

The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

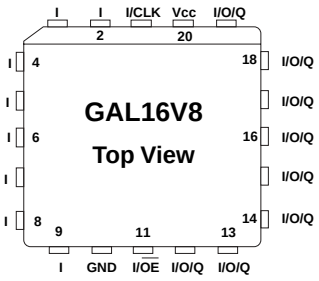
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram

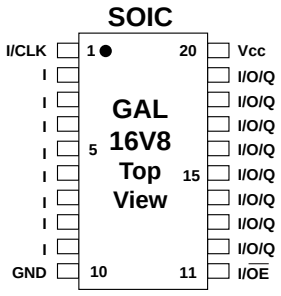


Pin Configuration

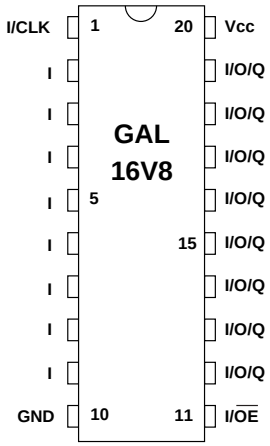
PLCC



SOIC



DIP



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Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

August 2004

General purpose CMOS timer ICM7555

DESCRIPTION

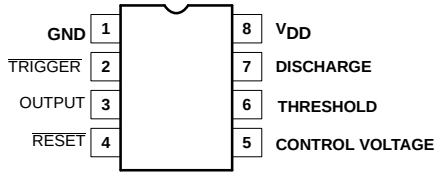
The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$, and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ inputs are active low. The output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

PIN CONFIGURATION

D and N Packages



FEATURES

- Exact equivalent in most applications for NE/SE555
- Low supply current: 80µA (typ)
- Extremely low trigger, threshold, and reset currents: 20pA (typ)
- High-speed operation: 500kHz guaranteed
- Wide operating supply voltage range guaranteed 3 to 16V over full automotive temperatures
- Normal reset function; no crowbarring of supply during output transition
- Can be used with higher-impedance timing elements than the bipolar 555 for longer time constants
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005%/°C at 25°C
- Rail-to-rail outputs

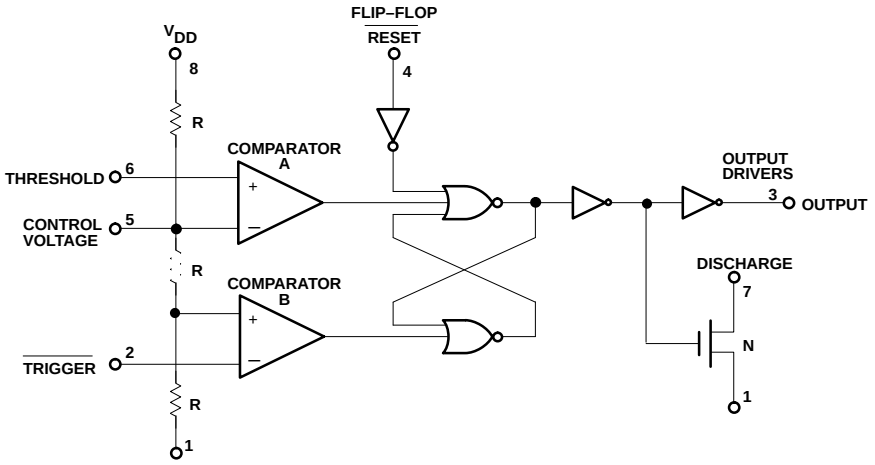
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	ICM7555CN	0404B
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	ICM7555CD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	ICM7555IN	0404B
8-Pin Plastic Small Outline (SO) Package	-40 to +85°C	ICM7555ID	0174C

EQUIVALENT BLOCK DIAGRAM



NOTE:
UNUSED INPUTS SHOULD BE CONNECTED TO APPROPRIATE VOLTAGE FROM TRUTH TABLE.

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V+)	> 1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V+)	HIGH	HIGH	OFF

NOTES:
1. $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	+18	V
V_{TRIG}[1]	$\overline{\text{Trigger}}$ input voltage		
V_{CV}	Control voltage	> -0.3 to	
V_{TH}	Threshold input voltage	<V_{DD} + 0.3	V
V_{RST}	$\overline{\text{RESET}}$ input voltage		
I_{OUT}	Output current	100	mA
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still air)[2]		
	N package	1160	mW
	D package	780	mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} + 0.3V or less than GND -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.
2. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
3. See "Power Dissipation Considerations" section.