April 9, 2012

LMP91050

Configurable AFE for Nondispersive Infrared (NDIR) Sensing Applications

General Description

The LMP91050 is a programmable integrated Sensor Analog Front End (AFE) optimized for thermopile sensors, as typically used in NDIR applications. It provides a complete signal path solution between a sensor and microcontroller that generates an output voltage proportional to the thermopile voltage. The LMP91050's programmability enables it to support multiple thermopile sensors with a single design as opposed to the multiple discrete solutions.

The LMP91050 features a programmable gain amplifier (PGA), “dark phase” offset cancellation, and an adjustable common mode generator (1.15V or 2.59V) which increases output dynamic range. The PGA offers a low gain range of 167V/V to 1335V/V plus a high gain range of 1002V/V to 7986V/V which enables the user to utilize thermopiles with different sensitivities. The PGA is highlighted by low gain drift (100 ppm/°C), output offset drift (1.2mV/°C at G = 1002 V/V), phase delay drift (500ns) and noise specifications (0.1 μV_{RMS} 0.1 to 10Hz) . The offset cancellation circuitry compensates for the “dark signal” by adding an equal and opposite offset to the input of the second stage, thus removing the original offset from the output signal. This offset cancellation circuitry allows optimized usage of the ADC full scale and relaxes ADC resolution requirements.

The LMP91050 allows extra signal filtering (high pass, low pass or band pass) through dedicated pins A0 and A1, in order to remove out of band noise. The user can program through the on board SPI interface. Available in a small form factor 10–pin MSOP package, the LMP91050 operates from -40 to +105°C.

Key Specifications

■ Programmable gain	167V/V to 7986V/V
■ Low noise (0.1 to 10 Hz)	0.1μV_{RMS}
■ Gain Drift	100 ppm/°C (max)
■ Phase Delay Drift	500ns (max)
■ Power supply voltage range	2.7V to 5.5V

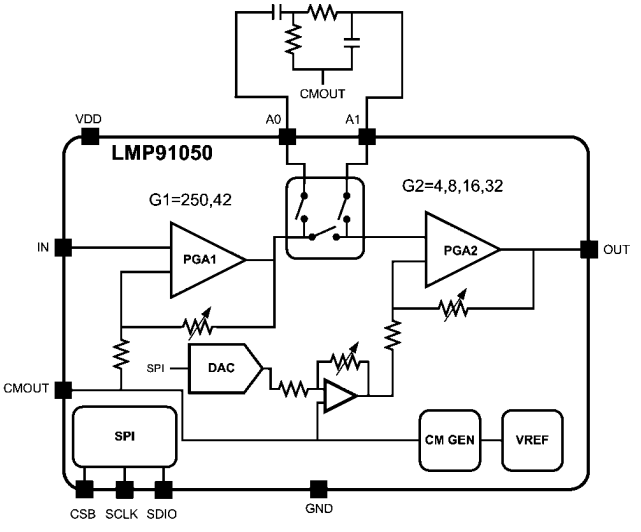
Features

- Programmable gain amplifier
- “Dark Signal” offset cancellation
- Supports external filtering
- Common mode generator and 8 bit DAC
- 10 pin MSOP package

Applications

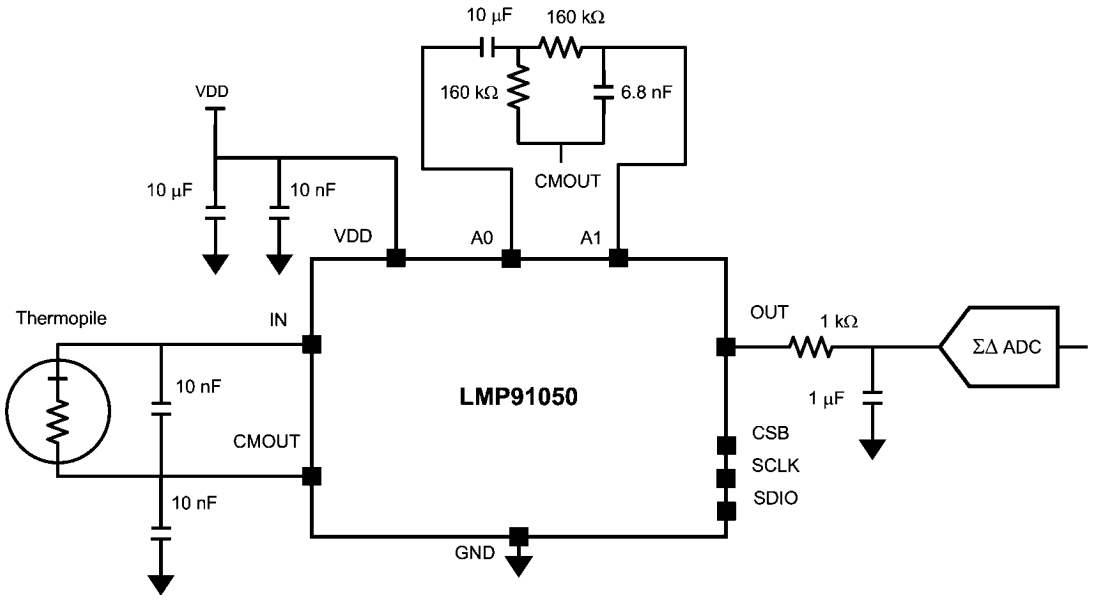
- NDIR sensing
- Demand control ventilation
- Building monitoring
- CO2 cabin control — Automotive
- Alcohol detection — Automotive
- Industrial safety and security
- GHG & Freons detection platforms

Block Diagram



Configurable AFE for NDIR

Typical Application

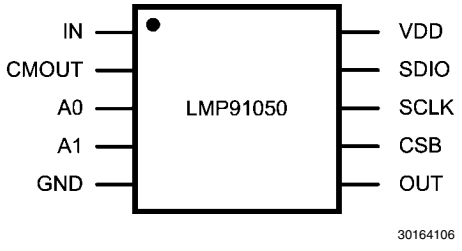


Typical NDIR Sensing Application Circuit

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
10–Pin MSOP	LMP91050MM	AN8A	1K units tape and reel	MUB10A
	LMP91050MME		250 units tape and reel	
	LMP91050MMX		3.5K units tape and reel	

Connection Diagram



Pin Descriptions

Pin	Symbol	Type	Description
1	IN	Analog Input	Signal Input
2	CMOUT	Analog Output	Common Mode Voltage Output
3	A0	Analog Output	First Stage Output
4	A1	Analog Input	Second Stage Input
5	GND	Power	Ground
6	OUT	Analog Output	Signal Output, reference to the same potential as CMOUT
7	CSB	Digital Input	Chip Select, active low
8	SCLK	Digital Input	Interface Clock
9	SDIO	Digital Input / Output	Serial Data Input / Output
10	VDD	Power	Positive Supply

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

ESD Tolerance(Note 2)	
Human Body Model	2500V
Machine Model	250V
Charged Device Model	1250V
Supply Voltage (VDD)	–0.3V to 6.0V
Voltage at Any Pin	– 0.3V to VDD + 0.3V
Input Current at Any Pin	5mA
Storage Temperature Range	-65°C to 150°C
Junction Temperature(Note 3)	150°C

For soldering specifications:
see product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.5V
Junction Temperature Range (Note 3)	-40°C to 105°C
Package Thermal Resitance, θ_{JA}	
10 Lead MSOP	176 °C/W

Electrical Characteristics (Note 4)

The following specifications apply for VDD = 3.3V, VCM = 1.15V, **Bold** values for T_A = -40°C to +85°C unless otherwise specified. All other limits apply to $T_A = T_J$ = +25°C.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Power Supply						
VDD	Supply Voltage		2.7	3.3	5.5	V
IDD	Supply Current	All analog block ON	3.1	3.7	4.2	mA
	Power Down Supply Current	All analog block OFF	45	85	121	µA
Offset Cancellation (Offset DAC)						
	Resolution			256		steps
	LSB	All gains		33.8		mV
	DNL		-1		2	LSB
	Error	Output referred offset error, all gains		±100		mV
	Offset adjust Range	Output referred, all gains	0.2		VDD – 0.2	V
	DAC settling time			480		µs
Programmable Gain Amplifier (PGA) 1st Stage, R_L = 10kΩ, C_L = 15pF						
IBIAS	Bias Current			5	**200**	pA
VINMAX _HGM	Max input signal High gain mode	Referenced to CMOUT voltage, it refers to the maximum voltage at the IN pin before clipping; It includes dark voltage of the thermopile and signal voltage.		±2		mV
VINMAX _LGM	Max input signal Low gain mode			±12		mV
VOS	Input Offset Voltage			-165		µV
G _HGM	Gain High gain mode			250		V/V
G_LGM	Gain Low gain mode			42		V/V
GE	Gain Error	Both HGM and LGM		2.5		%
VOUT	Output Voltage Range		0.5		VDD – 0.5	V
PhDly	Phase Delay	1mV input step signal, HGM, Vout measured at Vdd/2		6		µs
TCPhDly	Phase Delay variation with Temperature	1mV input step signal, HGM, Vout measured at Vdd/2,		416		ns
SSBW	Small Signal Bandwidth	Vin = 1mVpp, Gain = 250 V/V		18		kHz
Cin	Input Capacitance			100		pF
Programmable Gain Amplifier (PGA) 2nd Stage, R_S = 1kΩ, C_L = 1µF						

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
VINMAX	Max input signal	GAIN = 4 V/V		1.65		V
VINMIN	Min input signal			0.82		V
G	Gain	Programmable in 4 steps	4		32	V/V
GE	Gain Error	Any gain		2.5		%
VOUT	Output Voltage Range		0.2		VDD – 0.2	V
PhDly	Phase Delay	100mV input sine 35kHz signal, Gain = 8, VOUT measured at 1.65V, R_L = 10kΩ		1		µs
TCPhDly	Phase Delay variation with Temperature	250mV input step signal, Gain = 8, Vout measured at Vdd/2		84		ns
SSBW	Small Signal Bandwidth	Gain = 32 V/V		360		kHz
Cin	Input Capacitance			5		pF
CLOAD, OUT	OUT Pin Load Capacitance	Series RC		1		µF
RLOAD, OUT	OUT Pin Load Resistance	Series RC		1		kΩ
Combined Amplifier Chain Specification						
en	Input-Referred Noise Density	Combination of both current and voltage noise, with a 86kΩ source impedance at 5Hz, Gain = 7986		30		nV/√Hz
	Input-Referred Integrated Noise	Combination of both current and voltage noise, with a 86kΩ source impedance 0.1Hz to 10Hz, Gain = 7986		0.1	0.12 (Note 9)	µVrms
G	Gain	PGA1 GAIN = 42, PGA2 GAIN = 4		167		V/V
		PGA1 GAIN = 42, PGA2 GAIN = 8		335		
		PGA1 GAIN = 42, PGA2 GAIN = 16		669		
		PGA1 GAIN = 42, PGA2 GAIN = 32		1335		
		PGA1 GAIN = 250, PGA2 GAIN = 4		1002		
		PGA1 GAIN = 250, PGA2 GAIN = 8		2004		
		PGA1 GAIN = 250, PGA2 GAIN = 16		4003		
		PGA1 GAIN = 250, PGA2 GAIN = 32		7986		
GE	Gain Error	Any gain		5		%
TCCGE	Gain Temp Coefficient (Note 7)				**100**	ppm/°C
PSRR	Power Supply Rejection Ratio	DC, 3.0V to 3.6V supply, gain = 1002V/V	90	110		dB
PhDly	Phase Delay	1mV input step signal, Gain = 1002, Vout measured at Vdd/2		9		µs
TCPhDly	Phase Delay variation with Temperature (Note 8)	1mV input step signal, Gain=1002, Vout measured at Vdd/2			**500**	ns
TCVOS	Output Offset Voltage Temperature Drift (Note 7)	Gain = 167 V/V	**–0.525**		**0.525**	mV/°C
		Gain = 335 V/V	**–0.60**		**0.60**	
		Gain = 669 V/V	**–0.90**		**0.90**	
		Gain = 1335 V/V	**–1.50**		**1.50**	
		Gain = 1002 V/V	**–1.20**		**1.20**	
		Gain = 2004 V/V	**–1.90**		**1.90**	
		Gain = 4003 V/V	**–3.70**		**3.70**	
		Gain = 7986V/V	**–7.10**		**7.10**	
Common Mode Generator						
VCM	Common Mode Voltage	Programmable, see Common Mode Generation		1.15 or 2.59		V

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
	VCM accuracy			2		%
CLOAD	CMOut Load Capacitance			10		nF

SPI Interface (Note 4) The following specifications apply for VDD = 3.3V, VCM = 1.15V, C_L = 15pF, **Bold** values for T_A = -40°C to +85°C unless otherwise specified. All other limits apply to $T_A = T_J$ = +25°C.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{IH}	Logic Input High		0.7 × VDD			V
V_{IL}	Logic Input Low				0.8	V
V_{OH}	Logic Output High		2.6			V
V_{OL}	Logic Output Low				0.4	V
IIH/IIL	Input Digital Leakage Current		–100 **–200**		100 **200**	nA

Timing Characteristics (Note 4) The following specifications apply for VDD = 3.3V, VCM = 1.15V, C_L = 15pF, **Bold** values for T_A = -40°C to +85°C unless otherwise specified. All other limits apply to $T_A = T_J$ = +25°C.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
t_{WU}	Wake up time			1		ms
f_{SCLK}	Serial Clock Frequency				10	MHz
t_{PH}	SCLK Pulse Width High		$0.4/f_{SCLK}$			ns
t_{PL}	SCLK Pulse Width Low		$0.4/f_{SCLK}$			ns
t_{CSS}	CSB Setup Time		10			ns
t_{CSH}	CSB Hold Time		10			ns
t_{SU}	SDI Setup Time prior to rise edge of SCLK		10			ns
t_{SH}	SDI Hold Time prior to rise edge of SCLK		10			ns
t_{DOD1}	SDO Disable Time after rise edge of CSB				45	ns
t_{DOD2}	SDO Disable Time after 16th rise edge of SCLK				45	ns
t_{DOE}	SDO Enable Time from the fall edge of 8th SCLK				35	ns
t_{DOA}	SDO Access Time after the fall edge of SCLK				35	ns
t_{DOH}	SDO hold time after the fall edge of SCLK		5			ns
t_{DOR}	SDO Rise time			5		ns
t_{DOF}	SDO Fall time			5		ns

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

Note 7: TCCGE and TCVOS are calculated by taking the largest slope between -40°C and 25°C linear interpolation and 25°C and 85°C linear interpolation.

Note 8: TCPhDly is largest change in phase delay between -40°C and 25°C measurements and 25°C and 85°C measurements.

Note 9: Guaranteed by design and characterization. Not tested on shipped production material.

Timing Diagrams

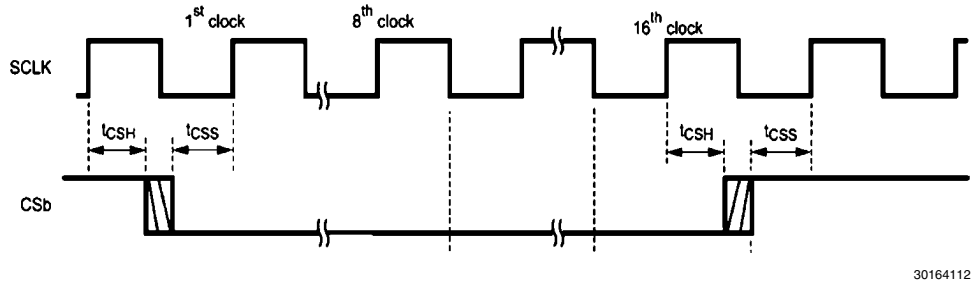


FIGURE 1. SPI Timing Diagram

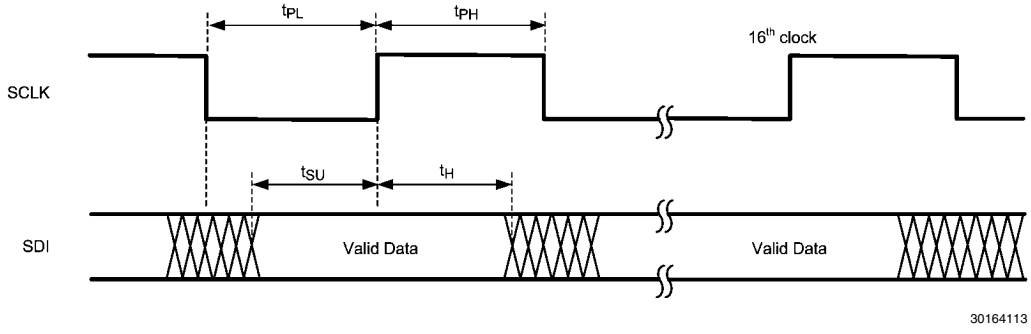


FIGURE 2. SPI Set-up Hold Time

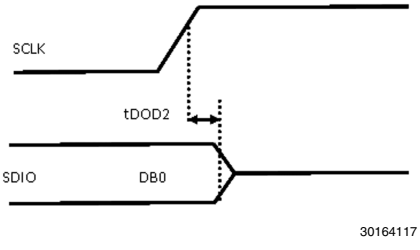


FIGURE 3. SDO disable time after 16th rise edge of SCLK

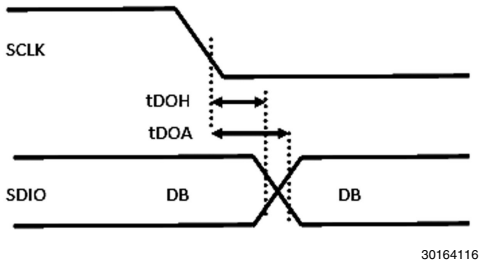


FIGURE 4. SDO access time (t_{DOA}) and SDO hold time (t_{DOH}) after the fall edge of SCLK

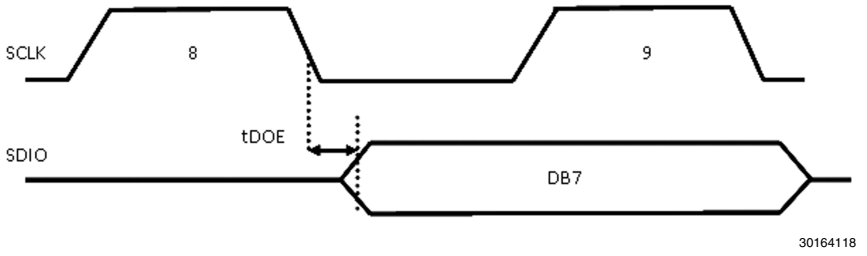


FIGURE 5. SDO Enable time from the fall edge of 8th SCLK

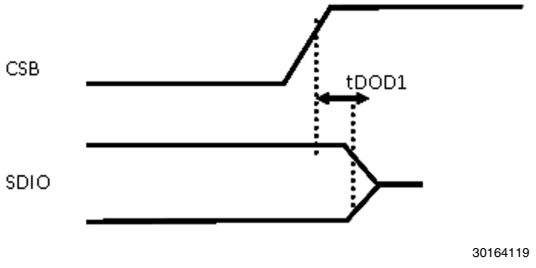


FIGURE 6. SDO disable time after rise edge of CSB

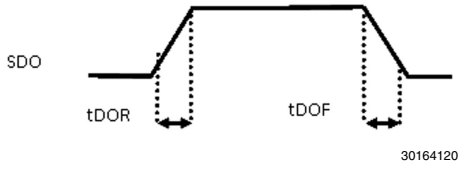
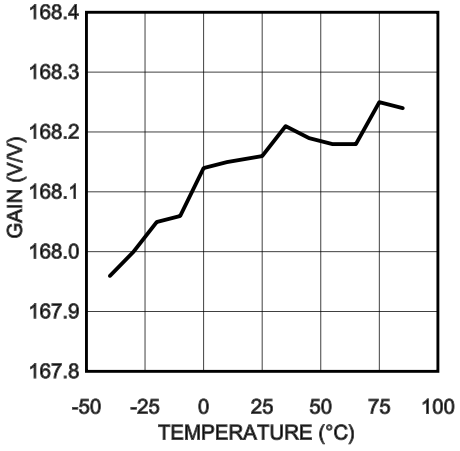


FIGURE 7. SDO rise and fall times

Typical Performance Characteristics

VDD = +3.3V, VCM = 1.15V, and T_A = 25°C unless otherwise noted

Gain = 167 V/V vs. Temperature



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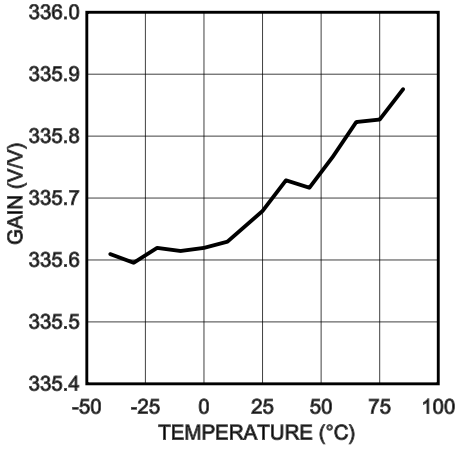
Gain = 335 V/V vs. Temperature



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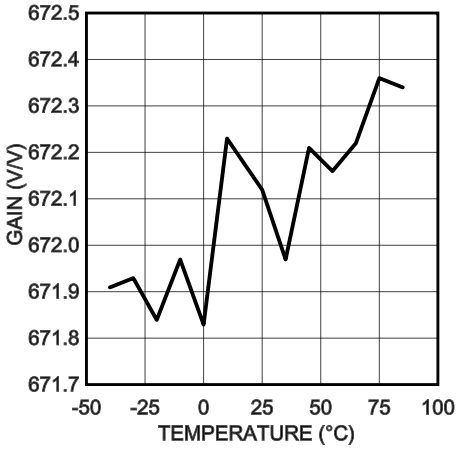
Gain = 669 V/V vs. Temperature



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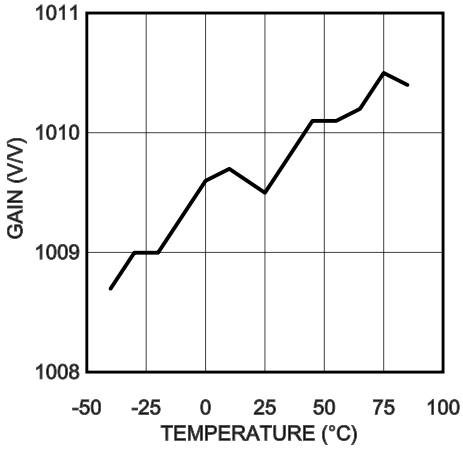
Gain = 1002 V/V vs. Temperature



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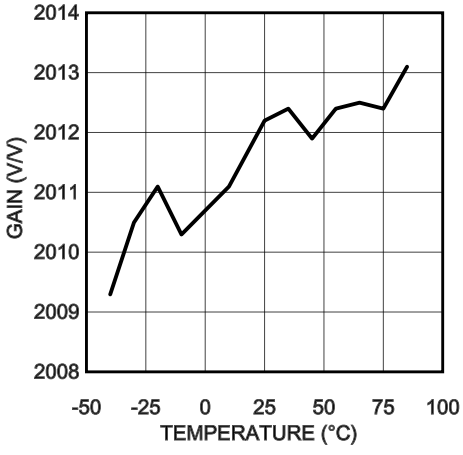
Gain = 2004 V/V vs. Temperature



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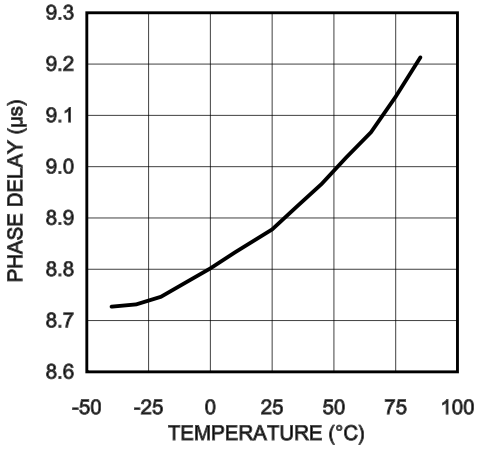
Phase Delay vs. Temperature



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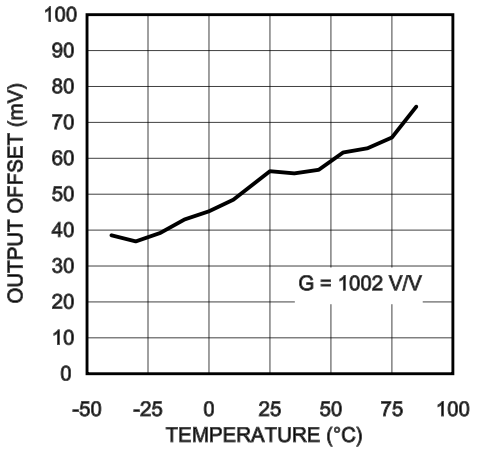
Output Offset vs. Temperature



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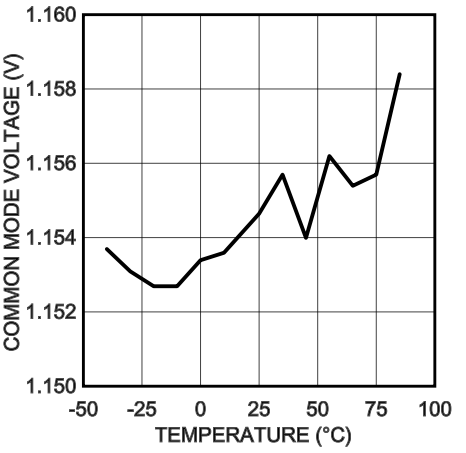
Common Mode Voltage vs. Temperature



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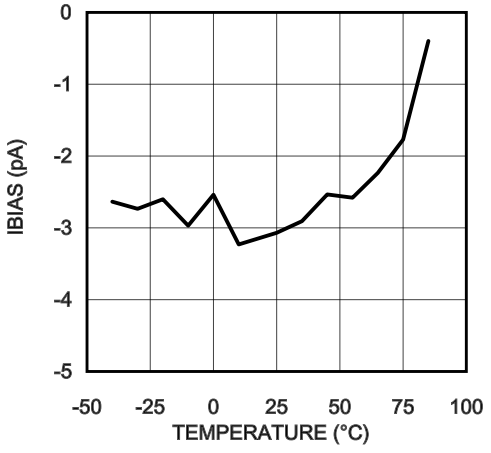
Input Bias Current vs. Temperature



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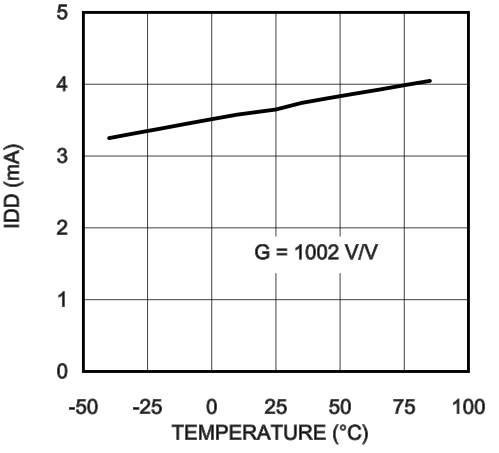
Supply Current vs. Temperature



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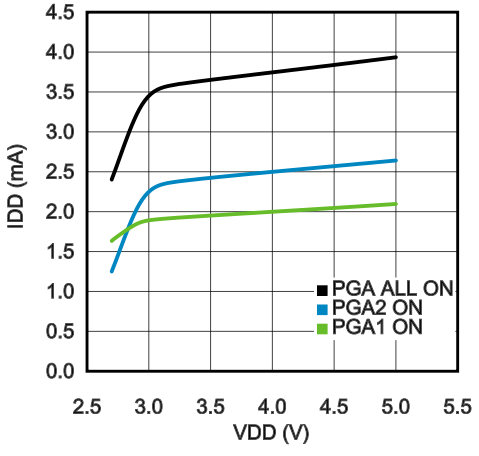
Supply Current vs. Supply Voltage



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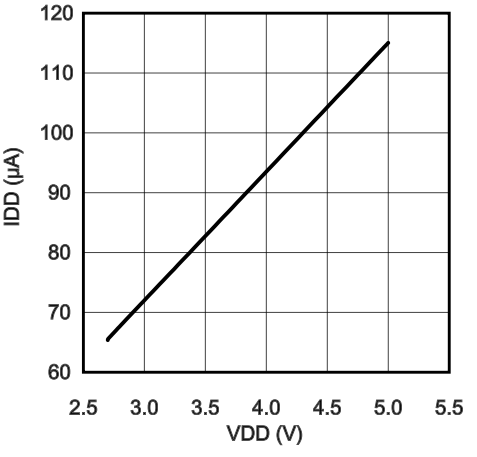
Power Down Supply Current vs. Supply Voltage



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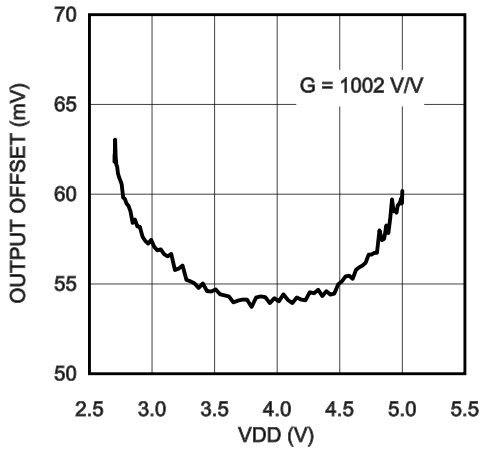
Output Offset vs. Supply Voltage



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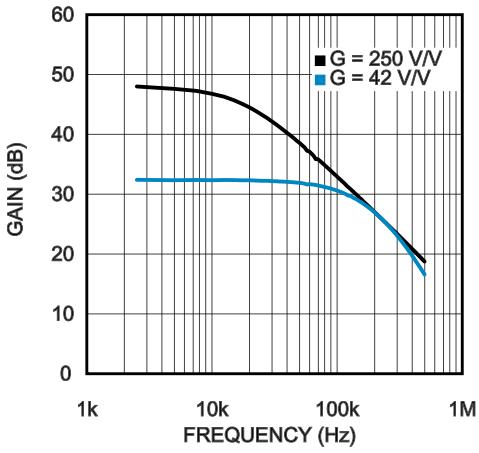
PGA1 Small Signal Bandwidth



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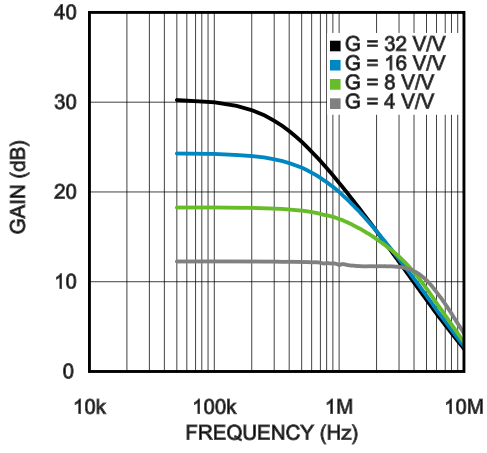
PGA2 Small Signal Bandwidth



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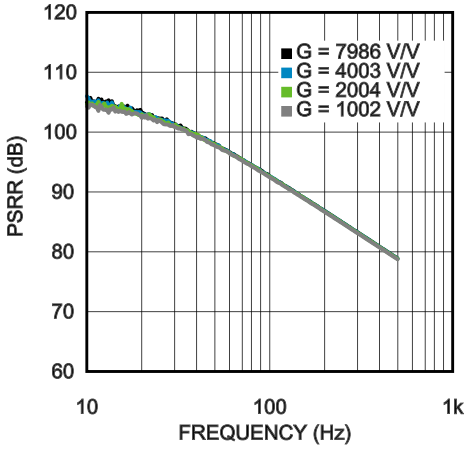
Power Supply Rejection Ratio vs. Frequency



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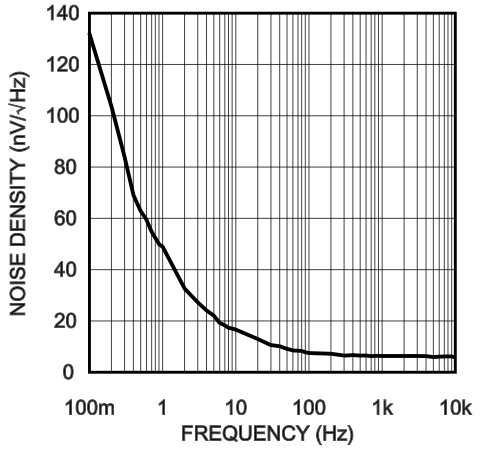
Input-Referred Noise Density vs. Frequency



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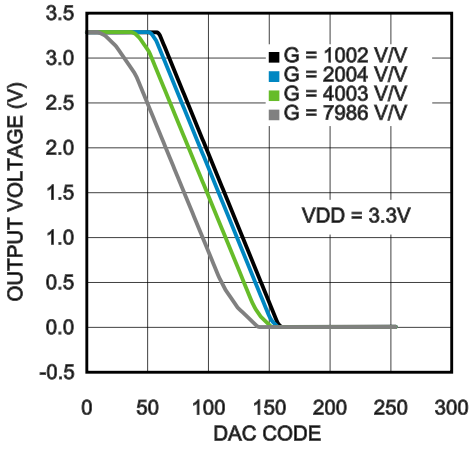
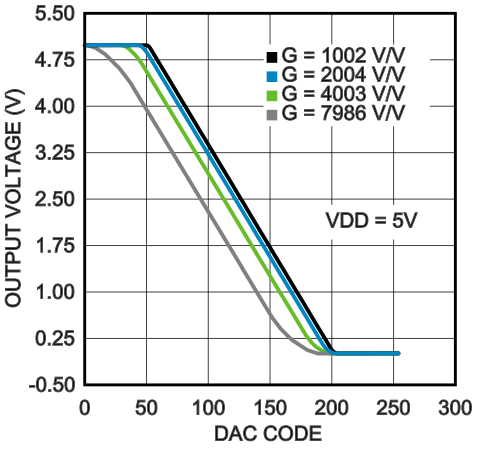
DAC DC Sweep



30164139

DAC DC Sweep



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Functional Description

PROGRAMMABLE GAIN AMPLIFIER

The LMP91050 offers two programmable gain modes (low/high) with four programmable gain settings each. The purpose of the gain mode is to enable thermopiles with larger dark voltage levels. All gain settings are accessible through bits GAIN1 and GAIN2[1:0]. The low gain mode has a range of 167 V/V to 1335 V/V while the high gain mode has a range of 1002 V/V to 7986 V/V. The PGA is referenced to the internally generated VCM. Input signal, referenced to this VCM voltage, should be within +/-2mV (see VINMAX_HGM specification) in high gain mode. In the low gain mode the first stage will provide a gain of 42 V/V instead of 250 V/V, thus allowing a larger maximum input signal up to +/-12mV (VINMAX_LGM).

TABLE 1. Gain Modes

Bit Symbol	Gain
GAIN1	**0: 250 (default)** 1: 42
GAIN2 [1:0]	**00: 4 (default)** 01: 8 10: 16 11: 32

EXTERNAL FILTER

The LMP91050 offers two different measurement modes selectable through EXT_FILT bit. EXT_FILT bit is present in the Device configuration register and is programmable through SPI.

TABLE 2. Measurement Modes

Bit Symbol	Measurement Mode
EXT_FILT	**0: The signal from the thermopile is being processed by the internal PGAs, without additional external decoupling or filtering (default).**
	1: The signal from the thermopile is being processed by the first internal PGA and fed to the A0 pin. An external low pass, high pass or band pass filter can be connected through pins A0, A1.

An external filter can be applied when EXT_FILT = 1. A typical band pass filter is shown in the picture below. Resistor and capacitor can be connected to the CMOUT pin of the LMP91050 as shown. Discrete component values have been added for reference.

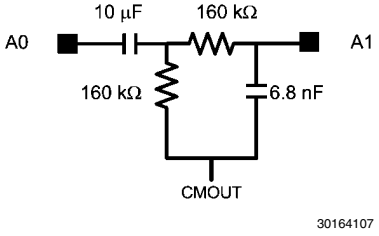


FIGURE 8. Typical Bandpass Filter

OFFSET ADJUST

Procedure of the offset adjust is to first measure the “dark signal”, program the DAC to adjust, and then measure in a second cycle the residual of the dark signal for further signal manipulation within the µC. The signal source is expected to have an offset component (dark signal) larger than the actual signal. During the “dark phase”, the time when no light is detected by the sensor, the µC can program LMP91050 internal DAC to compensate for a measured offset. A low output offset voltage temperature drift (TCVOS) ensures system accuracy over temperature. See *Figure 9* below which plots the maximum TCVOS allowed over a given temperature drift in order to achieve n bit system accuracy.

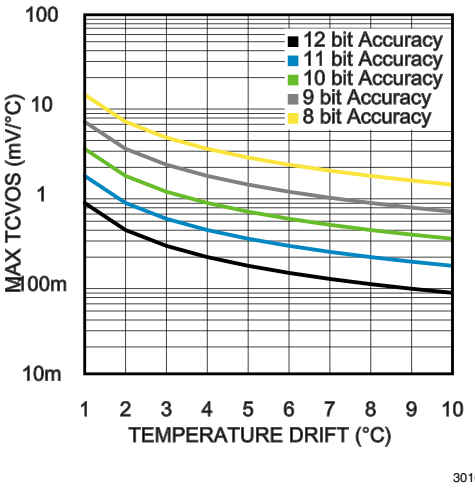


FIGURE 9. System Accuracy vs. TCVOS and Temperature Drift

COMMON MODE GENERATION

As the sensor's offset is bipolar, there is a need to supply a VCM to the sensor. This can be programmed as 1.15V or 2.59V (approximately mid rail of 3.3V or 5V supply). It is not recommended to use 2.59V VCM with 3.3V supply

SPI INTERFACE

An SPI interface is available in order to program the device parameters like PGA gain of two stages, enabling external filter, enabling power for PGAs, offset adjust and common mode (VCM) voltage.

Interface Pins

The Serial Interface consists of SDIO (Serial Data Input / Output), SCLK (Serial Interface Clock) and CSB (Chip Select Bar). The serial interface is write-only by default. Read operations are supported after unlocking the SDIO_MODE_PASSWD. This is discussed in detail later in the document.

CSB

Chip Select is a active-low signal. CSB needs to be asserted throughout a transaction. That is, CSB should not pulse between the Instruction Byte and the Data Byte of a single transaction.

Note that CSB de-assertion always terminates an on-going transaction, if it is not already complete. Likewise, CSB assertion will always bring the device into a state, ready for next transaction, regardless of the termination status of a previous transaction.

CSB may be permanently tied low for a 2-wire SPI communication protocol.

SCLK

SCLK can idle High or Low for a write transaction. However, for a READ transaction, SCLK should idle high. SCLK features a Schmitt-triggered input and although it has hysterisis, it is recommened to keep SCLK as clean as possible to prevent glitches from inadvertently spoiling the SPI frame.

Communication Protocol

Communication on the SPI normally involves Write and Read transactions. Write transaction consists of single Write Command Byte, followed by single Data byte. The following figure shows the SPI Interface Protocol for write transaction.

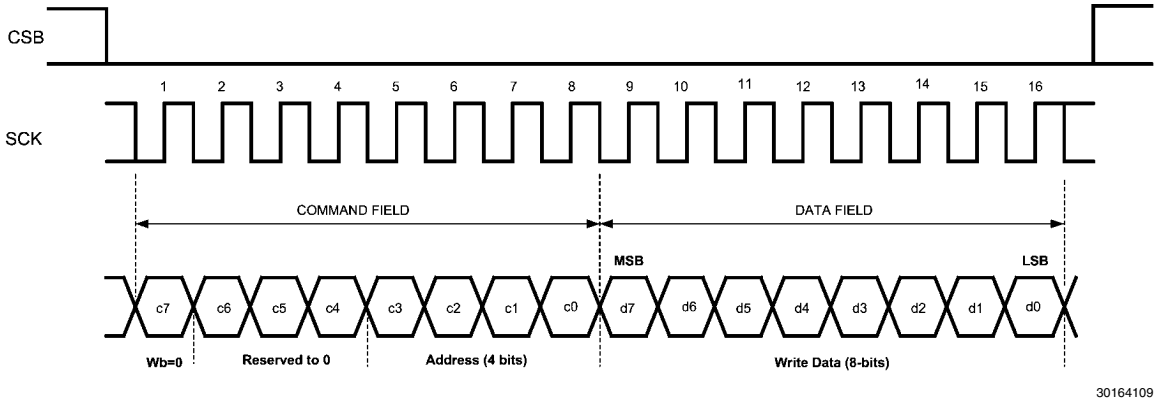
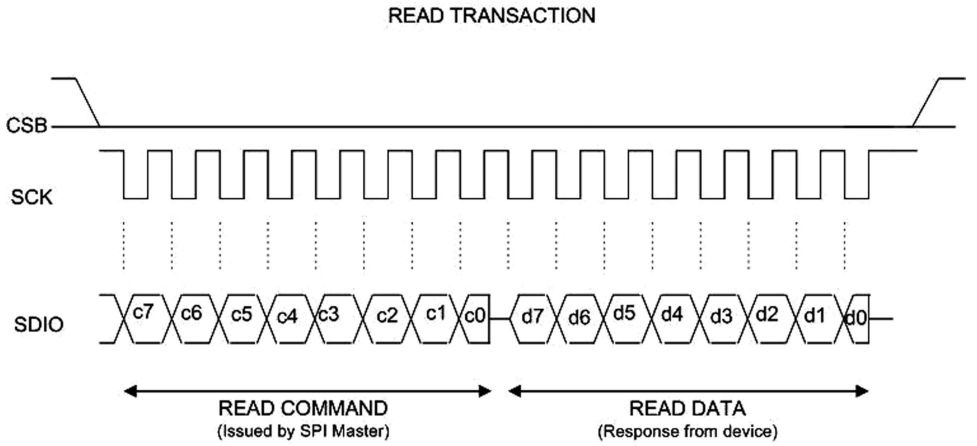


FIGURE 10. SPI Interface Protocol

For Read transactions, user first needs to write into a SDIO mode enable register for enabling the SPI read mode. Once the device is enabled for Reading, the data is driven out on the SDIO pin during the Data field of the Read Transaction. SDIO pin is designed as a bidirectional pin for this purpose. Figure 6 shows the Read transaction. The sequence of commands that need to be issued by the SPI Master to enable SPI read mode is illustrated in *Figure 12*.



Note: Read command is issued by the SPI Master, who after issuing the c0 (LSBit of the command byte) bit should relinquish the data line (high-Z) after meeting the hold timing(10ns) and stop SCK idling high.

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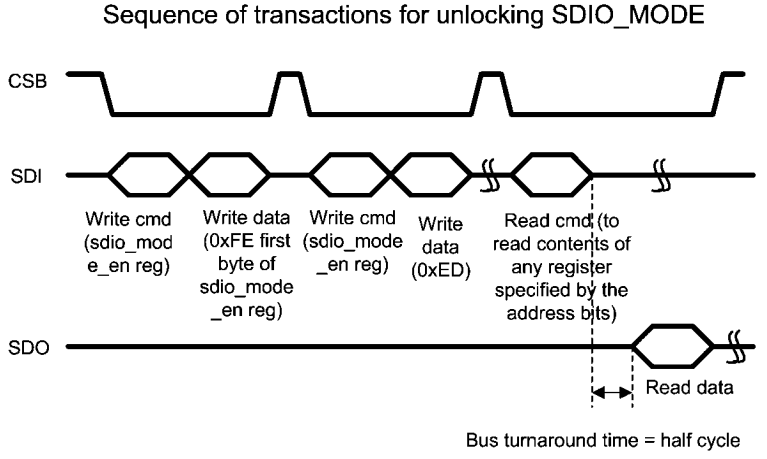
FIGURE 11. Read Transaction



Note:
1. Once the SDIO_mode is unlocked. The user can read as many registers as long as nothing else is written to sdio_mode_en register to disturb the state of SDIO_mode
2. The separate signals SDI and SDO are given in the figure for the sake of understanding. However, only one signal SDIO exists in the design

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FIGURE 12. Enable SDIO Mode for reading SPI registers

Registers Organization

Configuring the device is achieved using 'Write' of the designated registers in the device. All the registers are organized into individually addressable byte-long registers that have a unique address. The format of the Write/ Read instruction is as shown below.

TABLE 3. Write / Read Instruction Format

Bit[7]	Bit[6:4]	Bit[3:0]
0 : Write Instruction 1 : Read Instruction	Reserved to 0	Address

Note: Specifying any value other than zero in Bit[6:4] is prohibited.

REGISTERS

This section describes the programmable registers and the associated programming sequence, if any, for the device. The following table shows the summary listing of all the registers that are available to the user and their power-up values.

Title	Address (Hex)	Type	Power-up/Reset Value (Hex)
Device Configuration	0x0	Read-Write (Read allowed in SDIO Mode)	0x0
DAC Configuration	0x1	Read-Write (Read allowed in SDIO Mode)	0x80
SDIO Mode Enable	0xF	Write-only	0x0

Note: Recommended values must be programmed where they are indicated in order to avoid unexpected results. Avoid writing to addresses not mentioned in the document; this could cause unexpected results.

Device Configuration – Device Configuration Register (Address 0x0)

Bit	Bit Symbol	Description
7	RESERVED	Reserved to 0.
[6:5]	EN	**00: PGA1 OFF PGA2 OFF (default)** 01: PGA1 OFF, PGA2 ON 10: PGA1 ON, PGA2 OFF 11: PGA1 ON, PGA2 ON
4	EXT_FILT	**0: PGA1 to PGA2 direct (default)** 1: PGA1 to PGA2 via external filter
3	CMN_MODE	**0 : 1.15V (default)** 1 : 2.59V
[2:1]	GAIN2	**00: 4 (default)** 01: 8 10: 16 11: 32
0	GAIN1	**0: 250 (default)** 1: 42

DAC Configuration – DAC Configuration Register (Address 0x1)

The output DC level will shift according to the formula Vout_shift = -33.8mV * (NDAC - 128).

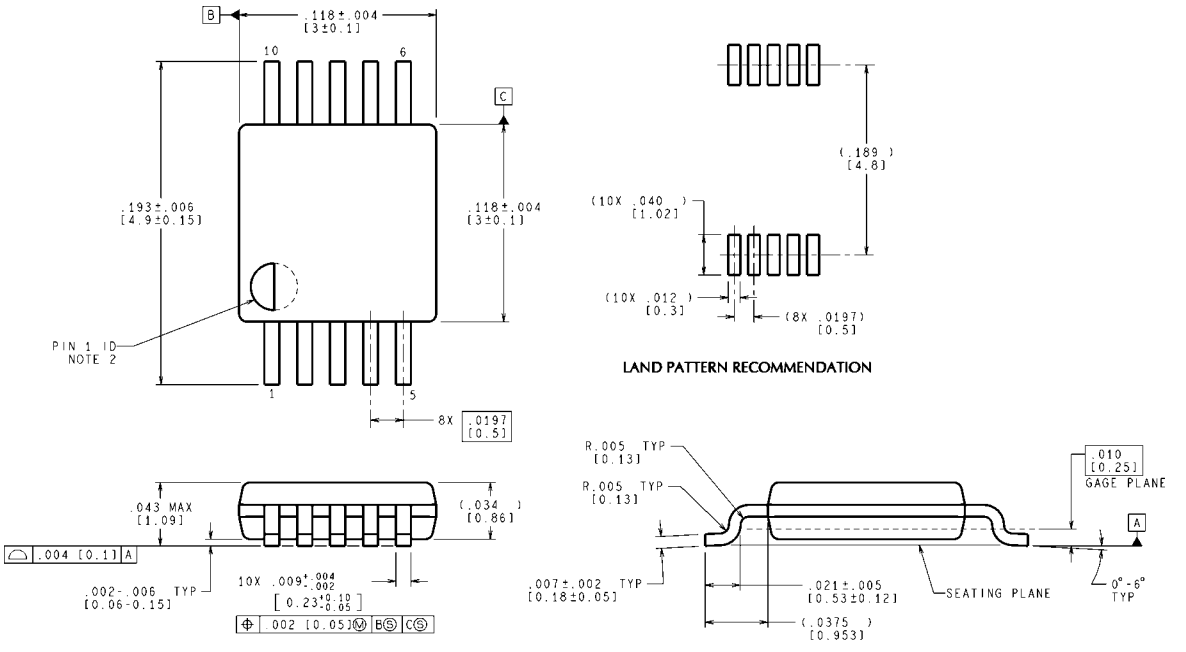
Bit	Bit Symbol	Description
[7:0]	NDAC	128 (0x80): Vout_shift = -33.8mV * (128 - 128) = 0mV (default)

SDIO Mode – SDIO Mode Enable Register (Address 0xf)

Write-only

Bit	Bit Symbol	Description
[7:0]	SDIO_MODE_EN	To enter SDIO Mode, write the successive sequence 0xFE and 0xED. Write anything other than this sequence to get out of mode.

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MUB10A (Rev B)

10–Lead MSOP
Order Numbers LMP91050MM/X
NS Package Number MUB10A

Notes

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