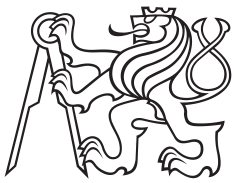
Master's thesis



Czech Technical University in Prague

F3

Faculty of Electrical Engineering
Katedra měření

Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač

Jakub Kákona

June 2014

http://petr.olsak.net/ctustyle.html

Draft: 28. 4. 2014

Acknowledgement / Declaration

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.

V Praze dne 13. 13. 2013

.....

Abstrakt / Abstract

.
Klíčová slova:

.
Keywords:

Contents

Chapter 1
Introduction

test

1.1 Typical Radio astronomy receiver

test

1.2 Requirements

test

1.2.1 Sensitivity

test

1.2.2 Dynamic range

test

1.2.3 Bandwidth

From requirements mentioned above

The system requires proper handling of huge amount of data.

1.3 Current radioastronomy problems

Professional radioostoronomers uses uses proprietary digitalisation units `http://arxiv.org/abs/1305.3550` or by multichannel sound cadrd on amateur levels `http://fringes.org/`

Chapter 2
Testing construction

Whole design of radioastronomy receiver digitalization unit shoud be constructed for the most universal application in signal digitalisation from radioastronomy receivers. Ilustrating problem for its use is signal digitalisation from multiple antenna arrays. This design will be used as part of MLAB Advanced Radio Astronomy System.

2.1 Required parameters

Wide dynamical range and high 3 intercept point are desired. The receiver must accept wide dynamic signals because classic radioastronomy signal in typically weak signal covered by strong man made noise signal.

- Dynamical range better than 80 dB
- Phase stability between channels
- Noise (all types)
- Sampling jitter better than 100 metres

2.2 Sampling frequency

Sampling frequency is limited by technical constrains in testing construction design. This parameter is especially limited by sampling frequencies of analog to digital conversion chips accessible on market. Combination of required parameters – dynamic range which needs 16bit at least and minimum sampling frequency of 1 MSPS, leads to high end ADC chips. Which does not support such low sampling frequencies at all. Its minimum sampling frequency is 5 MSPS.

2.3 System scalability

For analog channels scalability special parameters of ADC modules were needed. ADC module ideally needs separate output for each I/Q channel. ADC module must have

separate inputs for sampling and for data output clocks. This parameters allows conduction of relatively low digital data rates. And digital signal can be conducted on long wires.

Clock signal will be handled specially in this scalable design. Selected ADC chip guaranteed defined clock skew between sampling and data output clock. This allows taking data and frame clocks from first ADC module only. Other data and frame clocks from other ADC modules can be measured for diagnostic purposes. (Failure detection, jitter measurement etc.)

This system concept allows scalability technically limited by number of differential signals on host side, and its computational power. There is another advantage of scalable data acquisition system – economic reasons. Observatories or end user can pick choice how much money they are able to spent in radioastronomy receiver system. This option is especially useful for science sites without previous experience with radioastronomy observations.

2.3.1 Differential signalling

This concept of scalable design requires relatively long traces between ADC and digital unit which captures the data and performs computations. Distance of digital processing unit and analog to digital conversion unit has advantage in noise retention typically produced by digital circuits. Those digital circuits such as FPGA or other flip-flops block and traces usually works on high frequencies and emits wideband noise with relatively low power. In such case any distance increase between noise source and analog signal source increase S/N significantly. But this distance also brings problems with digital signal transmission between ADC and computational unit. But this obstruction should be resolved easier in free space than on board routing. The high quality differential signalling shielded cables should be used. This technology have two advantages on PCB signal routing. It can use two wire twisting for leak inductance suppression of signal path. And this twisted pair may be additionally shielded by uninterrupted metal foil.

2.3.2 Phase matching

For multiple antenna radioastronomy project, system phase stability is mandatory. It allows precise high resolution imaging of object.

High phase stability in this scalable design is achieved by centralised frequency generation and distribution with multi-output LVPECL hubs. These hubs have equiphased outputs for multiple devices.

This design ensures that all devices have access to defined phase and known frequency.

2.4 System description

In this section testing system will be described.

2.4.1 Frequency synthesis

Centralised topology was used for frequency synthesis. One precise high frequency and low jitter digital oscillator was used and other working frequencies are delivered by division from it. This central oscillator has software defined GPS disciplined control loop for frequency stabilisation.[1]) This method was used in order to meet modern requirements on radioastronomy equipment, which needs precise frequency and phase stability on wide area for effective radioastronomy imaging.

Every ADC module will be directly connected to CLKHUB02A module. This module takes sampling clock delevered by FPGA from main local oscillator. This signal should use high quality differential signaling cable – SATA cable should be used for this purpose.

2.4.2 Signal connectors

Several widely used and commercially easily accessible differential connectors were considered.

- HDMI
- SATA
- DisplayPort

[1]) `http://wiki.mlab.cz/doku.php?id=en:gpsdo` SDGPSDO design was developed in parallel to this diploma thesis construction as related project, but it is not explicitly required by specification.

- SAS/miniSAS

MiniSAS connector was chosen as the best for use in connection multiple ADC modules. This miniSAS connector is compatible with existing SATA cabling system and agregates multiple SATA cables to single connector. Translation between SATA and miniSAS is achieved by SAS to SATA adapter cable. This cable is used in servers to connecting SAS controller to multiple SATA hard disc in RAID systems thus is commercially available. One drawback is that miniSAS PCB connectors are mainufactured in SMT versions only. But outer metal housing of connector is standard trough hole type. This mechannical design should degrade durability of this connector type.

2.4.3 Design of ADC modules

This modules have MLAB standard construction with four mounting holes in corner aligned in defined raster.

Data serial data output of ADC module should be connected directly to FPGA for basic primary signal processing. Used ADC chip has selectable bit width of data output bus thus output SATA connectors has signals arranged to contain a single bit from every ADC channel. This signal concept enables selection of proper bus bitwidth according to sampling rate. (Higher bus bitwidth downgrades signaling speed and vice versa.)

For connection of this signaling layout, miniSAS to multiple SATA cable should be used.

For PCB layout KiCAD design suite was used. Used version has the CERN Push & Shove routing capability integrated but was slightly unstable and sometimes falls on exception during routing. Design must be often saved due to this stability issues. But Open-source KiCAD works well compared to commercial solutions as MentorGraphics PADS or Cadence Orcad. And much better than widely used Eagle software.

New PCB footprints have been designed for FMC, SATA a and miniSAS connectors. These new footprints were committed to KiCAD github library repository. And they are now publicly accessible from official KiCAD repository at GitHub.

2.4.4 ADC selection

Several ADC signaling formats currently exist for communication with FPGA.

- DDR LVDS
- JEDEC 204B
- JESD204A
- Paralel LVDS
- Serdes
- serial LVDS

Serial LVDS has been selected because uses lowest number of differencial pairs. This parameter is mandatory for construction complexity and reliability. `http://www.ti.com/lit/pdf/snaa110`

An ultrasound AFE chips should be ideal for this purpose – this chips has front-end amplifiers and filters integrated. But theirs drawback is incapability of handling differential input signal and relatively low dynamic range (consists 12bit ADC). This IO has many ADC channels thus scalling are possible in factor of 4 receivers (8 analog channels).

If we require separate output for every analog channel and 16bit deph. Only several ADCs currently exists which meet these requirements.

- [[http://www.linear.com/product/LTC2271—LTC2271]]
- [[http://www.linear.com/product/LTC2191—LTC2190-2195]].

All parts in this category are compatible with one board layout. Main differences are in sampling frequency and signal to noise ratio. The slowest one has maximal sampling frequency 20 MHz. But all types have minimal sampling frequency 5 MSPS. All types were configurable over serial interface (SPI). SPI seems to be a standard for high-end ADC chips from main manufacturers (Analog Devices, Linear technology, Texas instruments, Maxim integrated..).

2.4.5 ADC modules interface

All two ADCdual01A modules was connected to FPGA ML605 board trough FMC2DIFF01A adapter board. Construction of this adapter module suppose FMC

LPC connector. And this board is not MLAB compatible design. But this board is designed to meet VITA 57 standard specification for boards which uses zone 1 and zone 3. This specification guarantee compatibility with others FPGA board which has FMC LPC connector for mezzane cards. Schematic diagram of this adapter board is included in appendix.

Primary purpose of this PCB is to enable connection of ADC modules from space excluded from PC case. (In PC box analog circuits cannot be realised without using of massive RFI mitigation techniques). Differential signaling connectors should be used for conducting digital signal over relatively long cable. Signalintegrity sensitive links (clocks) are equiped by output driver and translator to LVPECL logic for better signal transmission quality.

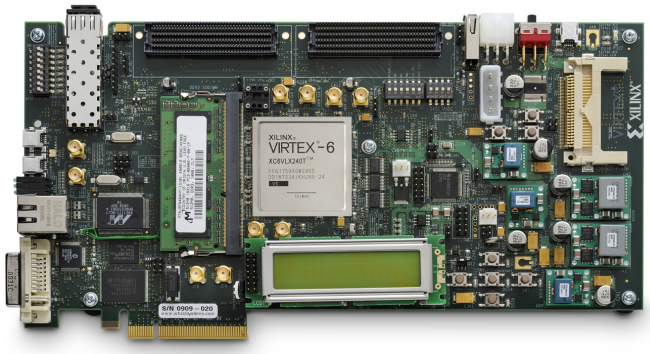


Figure 2.1. Used FPGA ML605 development board.

Several SATA connectors and two miniSAS connectors are populated on this board. This set of connectors allows connection of any number of ADC modules in range of 1 to 8. ADC data outputs should be connected to the miniSAS connectors. Other supporting signal should be routed directly to SATA connectors on adapter.

Signal configuration used in testing construction is described in tables.

2.4.6 Output data format

2.5 Achieved parameters

	160bit packet								
Data name	FRAME	ADC1 CH1		ADC1 CH2		ADC2 CH1		ADC2 CH2	
Data type	uint32	int16	int16	int16	int16	int16	int16	int16	int16
Content	saw signal	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}

Table 2.1. System device `/dev/xillybus_data2_r` data format

2.5.1 Data reading and recording

For reading data stream from ADC driver Gnuradio software was used. Gnuradio suite consist gnuradio-companion which is a graphical tool for creating signal flow graphs and generating flow-graph source code. This tool was used to create basic RAW data grabber to record and interactive wiev data stream output from ADC modules.

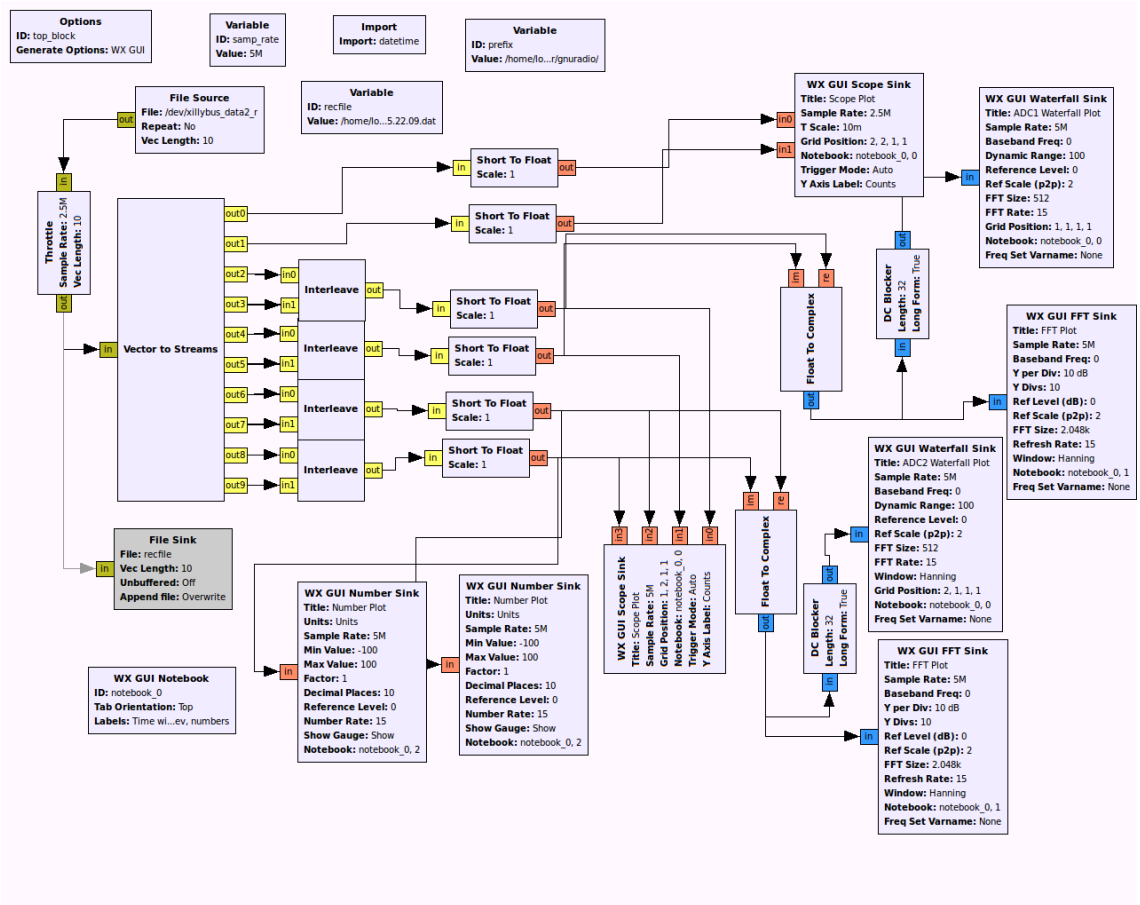


Figure 2.2. ADC recorder flow graph created in gnuradio-companion.

Interactive graber wiewer user interface shows live osciloscope-like time-value display for all data channels and live time-frequency scrolling display (waterfall wiev) for displaying frequency components of grabbed signal.

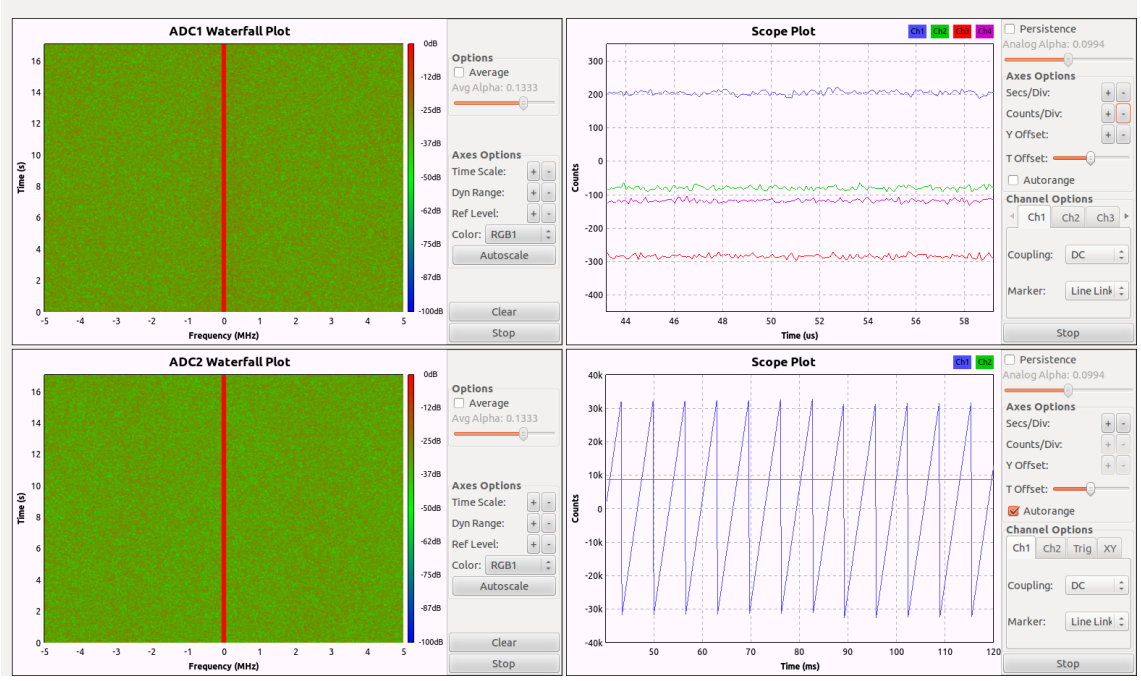


Figure 2.3. User interface window of running ADC grabber.

2.5.2 ADC module parameters

Two pieces of ADC module design were realised and tested first piece denoted as ADC1 has LTC21190 ADC chip populated with LT660015 front-end operational apmlifier. This ADC1 module has 1kOhm resistors populated on inputs which gives to module internal attenuation of input signal. Value of this attenuation is described by formula

T

ADC1 CH1 maximal input 705.7 mV

LTC2271 6600125 1k ADC2 CH1 maximal input 380 mV

Figure 2.4. Sine signal from ADC1 module with LTC21190 and LT6600-5 devices.

Figure 2.5. Sine signal from ADC1 module with LTC21190 and LT6600-5 devices.

Chapter 3
Proposed final system

Construction of final system which should be used for real radioastronomy observations will be described. This chapter is mainly theoretical analysis of systems which should be used for data handling.

3.1 Custom design of FPGA board

3.2 Parralella board computer

Parallella is gon

3.3 GPU based computational system

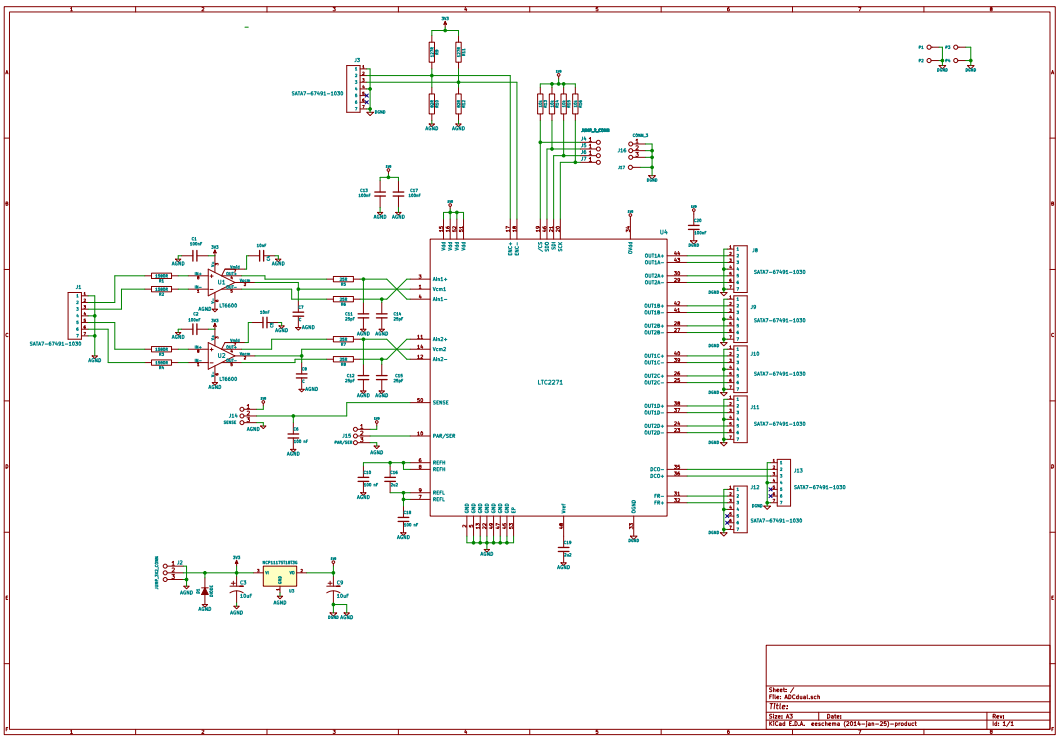
Chapter 4
Conclusion

Special design of scalable data-aquisition system was proposed. This system has parameters

4.1 Possible future improvements

Several ADC module imperfections such as useless separation of FRAME and DCO signal to two connectors should be mitigated. And this two signals should be merged to one SATA connector. This modification removes one redundant SATA cable between analog to digital converter nest and between computational unit nest.

Appendix A
Circuit diagram of ADCdual01A module



Appendix B
Circuit diagram of FMC2DIFF module