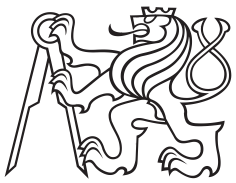
Master's thesis



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F3

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Fast multi-channel data acquisition system for radio-astronomy receiver

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June 2014
http://petr.olsak.net/ctustyle.html
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Draft: 4. 5. 2014

Acknowledgement / Declaration

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V Praze dne 12. 5. 2014

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Abstrakt / Abstract

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Klíčová slova:

Překlad titulu: Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač

.

Keywords:

Contents

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Chapter 1
Introduction

1.1 Current radioastronomy problems

From radioastronomer point of view its important radioastronomy has interest in primarily natural signals from surrounding universe. Radio astronomy do not have interest in terrestrial civilisation made signals.

Radioastronomy has a big problem at now. It is because many terrestrial transmitters are active at this moment. All terrestrial transceivers made dense signal mixture which can cause troubles not only to radioastronomers. In consequence, there exists attempts to control radiofrequency spectrum. As result of attempts to control the radiofrequency spectrum, the frequency allocation table was created. [1]) Radio-frequency allocation table table contain special bands allocated to radioastronomy use. But for many reasons this bands are not clean enough for directly use in radioastronomy observations. As result we cannot work by same way as radioastronomers in the beginning of radioastronomy. Many experiments namely, Cosmic microwave background detection and pulsar detection cannot be realised in its original form with acceptable results.

Supporting evidence of such effect is RadioJOVE project. NASA engineers which come with RadioJOVE project has great idea. RadioJOVE project brings opportunity for creating publicly available cheap radioastronomy receiver. But they used an old fashioned construction model which can work in desert, but it simply cannot work in modern civilisation as it is know in Europe. Origin of its dysfunction is presence of strong radiofrequency interferences. This interferences are orders of magnitude stronger than Jupiter decametric emissions. From practice about light pollution mitigation we also know that there are not much chance to improve this situation radically in radiofrequency spectrum.

There are not other ways that searching for new methods for radioastronomy observations. New methods which allows us to work without completely clear radiofrequency bands and which allow us to see surrounding universe trough man made radiofrequency interference mixture. One solution is use of already known natural radio frequency signals parameters. Natural signals usually have different signal properties from local interference. Natural object do not have a problem with transmitting in bandwidth of tens megahertz in sub 100 MHz bands. This object are usually far away and the same signal could be received at almost half of Earth without any significant differences. But it is also clear that signal parameters have drawbacks in reception power. The reception power of radioastronomy object is 1e9 smaller than signal power received from typical broadband radio transmitter.

From above mentioned facts about natural radio signals is clear one result. Modern requirements on radioastronomy receiver are complete different from requirements in history. Radioastronomy is not limited by access to electronic components today, but it is limited by presence of electronic everywhere.

[1]) `http://www.ukaranet.org.uk/basics/frequency_allocation.htm`

1.2 Modern Radio astronomy receiver

In beginning of radioastronomy receivers were constructed as simple station with single antenna or multi antenna array with fixed phasing. This approach were used due to limits of previous electronics components and technology. Main challenges were noise number and sensitivity due to poor characteristic of active electronic components such transistors and vacuum tubes.

Most of today operational radioastronomy equipments were constructed in this manner. They were constructed usually shortly after WWII or during The Cold War as parts of military technology.

But today we have access to components with quality, repeatability and price is completely district from components accessible for previous generation of radioastronomers. Then we could develop better radioastronomy equipment which will be powerful enough for make new astronomy discovery.[1])

We could develop a receiver which will have wide bandwidth, high Third-order intercept point and ideally has an option for phase and frequency locking to other receiver on another radioastronomy site of planet. Several receivers which have such parameters currently exists USRP2, USRP B210 or HackRF and are commercially available. But all of them lacks scalability and have high prices. However scalability and redundancy is main requirement which is requested by noise reduction algorithms.

New radio astronomy systems such LOFAR are explicit examples of scalability and redundancy approach. LOFAR has completely different and new structure to solve problems of radioastronomy signal reception. LOFAR exclusively uses multi antenna arrays and mathematical algorithms for signal handling. Radio signals recorded by LOFAR can be used by many ways. Radio image can be computed (if sufficient cover of u/v plane is achieved), radiation intensity can be measured, spectrum can be analysed for velocity measurement. etc.

1.2.1 Observation types

Today radioastronomy knows several observation types.

- Spectral observations
- Intensity observations
- Velocity observations

All of these observations ideally needs high frequency resolution and stability. Wide observation bandwidth in hundreds of MHz is usually desirable for easier differentiation of source types.

1.3 Required receiver parameters

New approach of receiver construction described above has new requirements on receiver parameters. No additional attempts for signal to noise ratio on single antenna are performed. But other parameters are requested at now.

[1]) Most of astronomy related discoveries in last fifty years came from radioastronomy.

1.3.1 Sensitivity and noise number

These parameters are are tied together, but multi antenna and multi receiver arrays requires to keep price of receiver at minimal values. This implicates that sensitivity and noise number must be least as good to detect (signal /noise ¿ 1) observed object on majority of receivers connected to observation network.

1.3.2 Dynamic range

Dynamic range is huge problem of current radioastronomy receivers. This parameter is enforced by anywhere present humans made EMI radiation on RF frequencies. The modern radio astronomy receiver must not be saturated by this high levels of signals but still needs to have enough sensitivity to see faint signals from natural sources. Dynamic range should be limited by construction of analogue circuitry in receiver or by digitalisation unit. Maximal theoretical dynamic range of ADC could be estimated from ADC bit depth according to formula ??

$$D.R.(dB) = 20 * log(2^n)$$

Formula ?? gives values shown in table 1.1.

[ADC-dynamic-range]

ADC Bits	Dynamic range [dB]
8	48
10	60
12	72
14	84
16	96
24	144

Table 1.1. Standard bit depths of ADC and its theoretical dynamic range.

1.3.3 Bandwidth

Historically bandwidth parameter of radioastronomy receiver was in kilohertz range. Small bandwidth was acceptable because observations were processed directly by listening or by paper chart intensity recorder. Chart recorder integrate energy of signal over defined small bandwidth which was suitable for detection of intensity variance in microwave background. No wideband transmitters exist in this era (except of TV transmitters) and eventually tuning to other neighbour silent frequency was easy. Parallel observations from several places was unnecessary because conditions were nearly same at all locations.

The system requires proper handling of huge amount of data.

Professional astronomers uses uses proprietary digitalisation units `http://arxiv.org/abs/1305.3550` or by multichannel sound cadrd on amateur levels `http://fringes.org/`

Chapter 2
Trial design

The whole design of radioastronomy receiver digitalization unit is constructed to be used in a wide range of applications and tasks related to digitalisation of signal from radioastronomy receivers. A good illustrating problem for its use is a signal digitalisation from multiple antenna arrays. This design will eventually become a part of MLAB Advanced Radio Astronomy System.

2.1 Required parameters

Wide dynamical range and high 3 intercept points are desired. The receiver must accept wide dynamic signals because a typical radioastronomical signal has a form of a weak signal covered by a strong man-made noise.

- Dynamical range better than 80 dB
- Phase stability between channels
- Noise (all types)
- Sampling jitter better than 100 metres

2.2 Sampling frequency

Sampling frequency is limited by the technical constrains in the trial design. This parameter is especially limited by the sampling frequencies of analog-to-digital conversion chips available on the market. Combination of the required parameters – dynamic range requiring at least 16bit and a minimum sampling frequency of 1 MSPS leads to need of high end ADC chips which does not support such low sampling frequencies at all. Their minimum sampling frequency is 5 MSPS.

2.3 System scalability

For analogue channels scalability, special parameters of ADC modules are required. Ideally, there should be a separate output for each I/Q channel in ADC module. ADC module must also have separate inputs for sampling and data output clocks. These parameters allow for conduction at relatively low digital data rates. As a result, the digital signal can be conducted even through long wires.

Clock signal will be handled distinctively in our scalable design. Selected ADC chip are guaranteed to have defined clock skew between sampling and data output clock. This allows taking data and frame clocks from the first ADC module only. The rest of the data and frame clocks from other ADC modules can be measured for diagnostic purposes (failure detection, jitter measurement etc.).

This system concept allows for scalability, that is technically limited by a number of differential signals on host side and its computational power. There is another advantage of scalable data acquisition system – an economic one. Observatories or end users can

make a choice of how much money are they willing to spent on radioastronomy receiver system. This freedom of choice is especially useful for science sites without previous experience in radioastronomy observations.

2.3.1 Differential signalling

The concept of scalable design requires relatively long circuit traces between ADC and digital unit which captures the data and performs the computations. The long distance between the digital processing unit and the analog-to-digital conversion unit has an advantage in noise retention typically produced by digital circuits. Those digital circuits, such as FPGA or other flip-flops block and circuit traces, usually work at high frequencies and emit wide-band noise with relatively low power. In such cases any increase in a distance between the noise source and analog signal source increase S/N significantly. However, at the same time a long distance brings problems with the digital signal transmission between ADC and computational unit. This obstacle should be resolved more easily in free-space than on board routing. The high-quality differential signalling shielded cables should be used. This technology has two advantages over PCB signal routing. First, it can use twisted pair of wires for leak inductance suppression in signal path and second, the twisted pair may additionally be shielded by uninterrupted metal foil.

2.3.2 Phase matching

For multiple antenna radioastronomy projects, system phase stability is a mandatory condition. It allows precise high resolution imaging of objects.

High phase stability in our scalable design is achieved through centralised frequency generation and distribution with multi-output LVPECL hubs, that have equiphased outputs for multiple devices.

This design ensures that all devices have access to the defined phase and known frequency.

2.4 System description

In this section testing system will be described.

2.4.1 Frequency synthesis

We have used a centralised topology as a basis for frequency synthesis. One precise high-frequency and low-jitter digital oscillator has been used, while other working frequencies have been derived from it by the division of its signal. This central oscillator has a software defined GPS disciplined control loop for frequency stabilisation.[1]) We have used methods of frequency monitoring compensation in order to meet modern requirements on radioastronomy equipment which needs precise frequency and phase stability over a wide scale for effective radioastronomy imaging.

Every ADC module will be directly connected to CLKHUB02A module which takes sampling clock signal delivered by FPGA from main local oscillator. This signal should use high quality differential signalling cable – we should use SATA cable for this purpose.

[1]) `http://wiki.mlab.cz/doku.php?id=en:gpsdo` SDGPSDO design has been developed in parallel to this diploma thesis as a related project, but it is not explicitly required by the diploma thesis.

2.4.2 Signal cable connectors

Several widely used and commercially easily accessible differential connectors were considered to be use in our design.

- HDMI
- SATA
- DisplayPort
- SAS/miniSAS

At the end, MiniSAS connector was chosen as the best option to be used in connecting together multiple ADC modules. It is compatible with existing SATA cabling systems and aggregates multiple SATA cables to a single connector. It can be seen on the following picture 2.1. A transition between SATA and miniSAS is achieved by SAS to SATA adapter cable which is commonly used in servers to connect SAS controller to multiple SATA hard disc in RAID systems and thus is commercially easily available. The main drawback of miniSAS PCB connectors lies in the fact, that they are manufactured in SMT versions only. The outer metal housing of connector is designed to be mounted using a standard through-hole mounting scheme, a design that unfortunately decreases the durability of the connector.

[img-miniSAS-cable]

Figure 2.1. A type of miniSAS cable similar to used.

2.4.3 Signal integrity requirements

We use ADC modules that have DATA clock frequency eight times higher than sampling frequency in single line output mode, implying a 40 MHz output bit rate.

2.4.4 ADC modules design

The ADC modules have a standard MLAB construction scheme with four mounting holes in corners aligned in defined raster.

Data serial data outputs of ADC modules should be connected directly to FPGAs for the basic primary signal processing. The ADC chip used in the modules has a selectable bit width of data output bus and thus the output SATA connectors have signals arranged to contain a single bit from every ADC channel. This creates a signal concept enabling a selection of a proper bus bit-width according to the sampling rate (higher bus bit-width downgrades signalling speed and vice versa.)

In order to connect the above mentioned signalling layout, miniSAS to multiple SATA cable should be used.

A KiCAD design suite had been chosen for PCB layout. However, the version is, despite having integrated CERN Push & Shove routing capability, slightly unstable as it sometimes crushes due to an exception during routing. On the basis of these stability issues, the design had to be saved quite often. On the other hand, compared to commercially available solutions, such as MentorGraphics PADS or Cadence Orcad, the Open-source KiCAD provides an acceptable option and it easily surpasses a widely used Eagle software.

As a part of work on the thesis, new PCB footprints for FMC, SATA a and miniSAS connectors have been designed and were committed to KiCAD github library repository. They are now publicly available on the official KiCAD repository at GitHub.

2.4.5 ADC selection

There exist several ADC signalling formats currently used in communication with FPGA.

- DDR LVDS
- JEDEC 204B
- JESD204A
- Paralel LVDS
- Serdes
- serial LVDS

Because it uses the smallest number of differential pairs, the choice fell on the serial LVDS format. Small number of differential pairs is an important parameter determining the construction complexity and reliability. `http://www.ti.com/lit/pdf/snaa110`

An ultrasound AFE chip seems to be ideal for this purpose – the chip has integrated both front-end amplifiers and filters. It has a drawback though - it is incapable of handling differential input signal and has a relatively low dynamic range (as it consists only of 12bit ADC). Because this IO has many ADC channels the scaling is possible only by a factor of 4 receivers (making 8 analogue channels).

If we require a separate output for every analogue channel and a 16bit depth we find that there are only a few 2-Channel simultaneous sampling ADCs currently existing which meet these requirements. We have summarised the ADCs in the following table ??

All parts in this category are compatible with one board layout. Main differences lay in the sampling frequency and signal to noise ratio, with the slowest having a maximum sampling frequency of 20 MHz. However all of them have a minimal sampling frequency of 5 MSPS and all are configurable over a serial interface (SPI). SPI seems to be a standard interface used in high-end ADC chips made by the largest manufacturers (Analog Devices, Linear technology, Texas instruments, Maxim integrated..).

ADC Type	LTC2271	LTC2190	LTC2191	LTC2192	LTC2193	LTC2194	LTC2195
SNR [dB]	84.1	77	77	77	76.8	76.8	76.8
SFDR [dB]	99	90	90	90	90	90	90
S/H Bandwidth [MHz]	200			550			
Sampling rate [MSPS]	20	25	40	65	80	105	125
Configuration				SPI			
Package	52-Lead		(7mm	■	8mm)	QFN	

[ADC-types]

Table 2.1. The summary of available ADC types and theirs characteristics.

2.4.6 ADC modules interface

Both of the ADCdual01A modules were connected to FPGA ML605 board trough FMC2DIFF01A adapter board. The design of this adapter module expects the presence of FMC LPC connector and the board is, at the same time, not compatible with MLAB. It is, on the other hand, designed to meet the VITA 57 standard specifications for boards which support region 1 and region 3. VITA 57 regions are explained in the picture 2.3. This industry standard guarantees the compatibility with other FPGA boards that have FMC LPC connectors for Mezzanine Card. Schematic diagram of this adapter board is included in the appendix.

The primary purpose of the PCB is to enable the connection of ADC modules located outside the PC case. (In PC box analog circuits cannot be realised without the use of massive RFI mitigation techniques). Differential signalling connectors should be used for conducting digital signal over relatively long cables. The signal integrity sensitive links (clocks) are equipped with output driver and translator to LVPECL logic for better signal transmission quality.

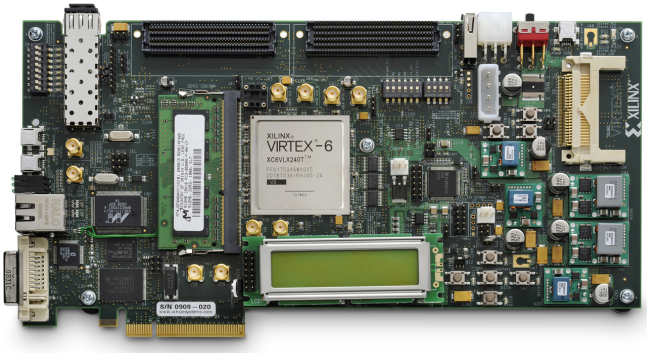
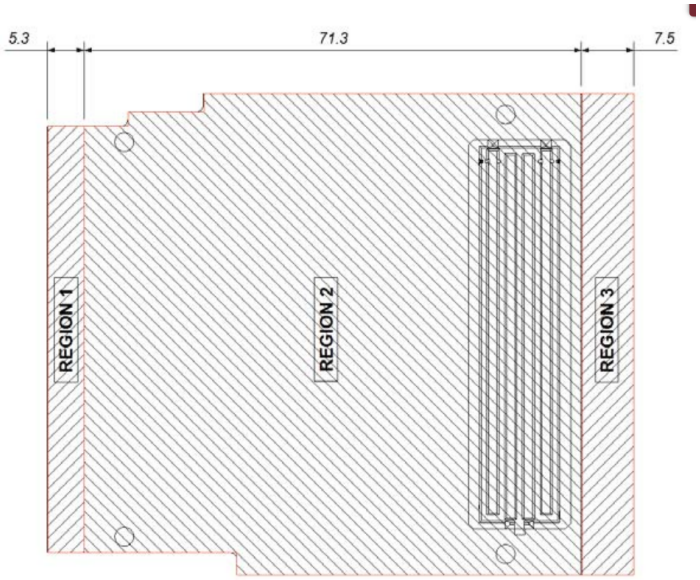


Figure 2.2. FPGA ML605 development board.

Several SATA connectors and two miniSAS connectors are populated on this board. This set of connectors allows a connection of any number of ADC modules within the range of 1 to 8. ADC data outputs should be connected to the miniSAS connectors, while other supporting signals should be routed directly to SATA connectors on adapter.

Signal configuration used in our trial design is described in the following tables.

2.4.7 Output data format



[VITA57-regions]

Figure 2.3. Definition of VITA57 regions.

	160bit packet								
Data name	FRAME	ADC1 CH1		ADC1 CH2		ADC2 CH1		ADC2 CH2	
Data type	uint32	int16	int16	int16	int16	int16	int16	int16	int16
Content	saw signal	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}

Table 2.2. System device `/dev/xillybus_data2_r` data format

2.5 Achieved parameters

2.5.1 Data reading and recording

We use Gnuradio software to read the data stream from the ADC drive. Gnuradio suite consist of gnuradio-companion which is a graphical tool for creating signal-flow graphs and generating flow-graph source code. This tool was used to create a basic RAW data grabber to record and interactively view the data stream output from ADC modules.

Interactive grabber viewer user interface shows live oscilloscope-like time-value display for all data channels and live time-frequency scrolling display (a waterfall view) for displaying the frequency components of the grabbed signal.

2.5.2 ADC module parameters

Two pieces of ADC modules were completed and tested. The first piece, labeled ADC1, has LTC21190 ADC chip populated with LT660015 front-end operational amplifier. It also has a 1kOhm resistors populated on inputs which gives it an ability of an internal attenuation of input signal. The value of this attenuation A is described by the following formula

$$A = \frac{1580 \times R_1}{R_1 + R_2}$$

ADC1 CH1 maximal input 705.7 mV
LTC2271 6600125 1k ADC2 CH1 maximal input 380 mV

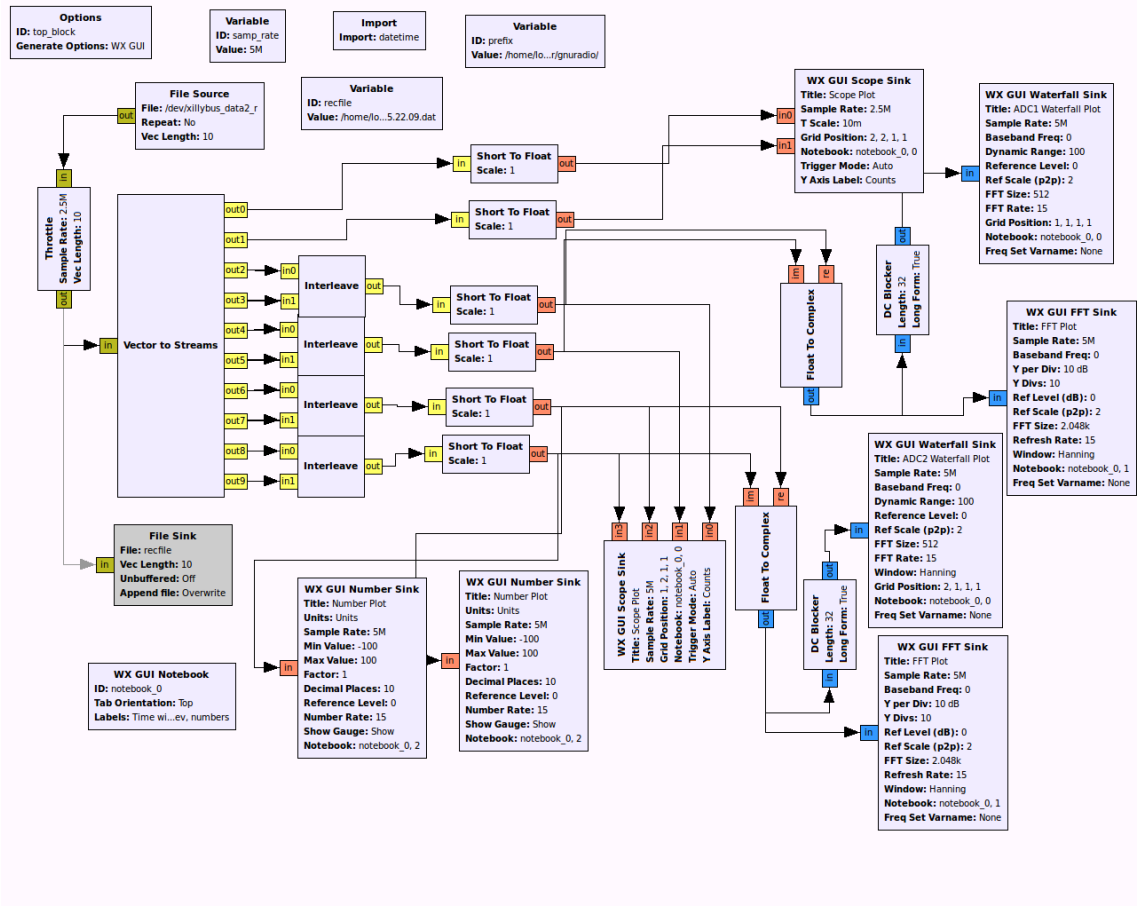


Figure 2.4. An ADC recorder flow graph created in gnuradio-companion.

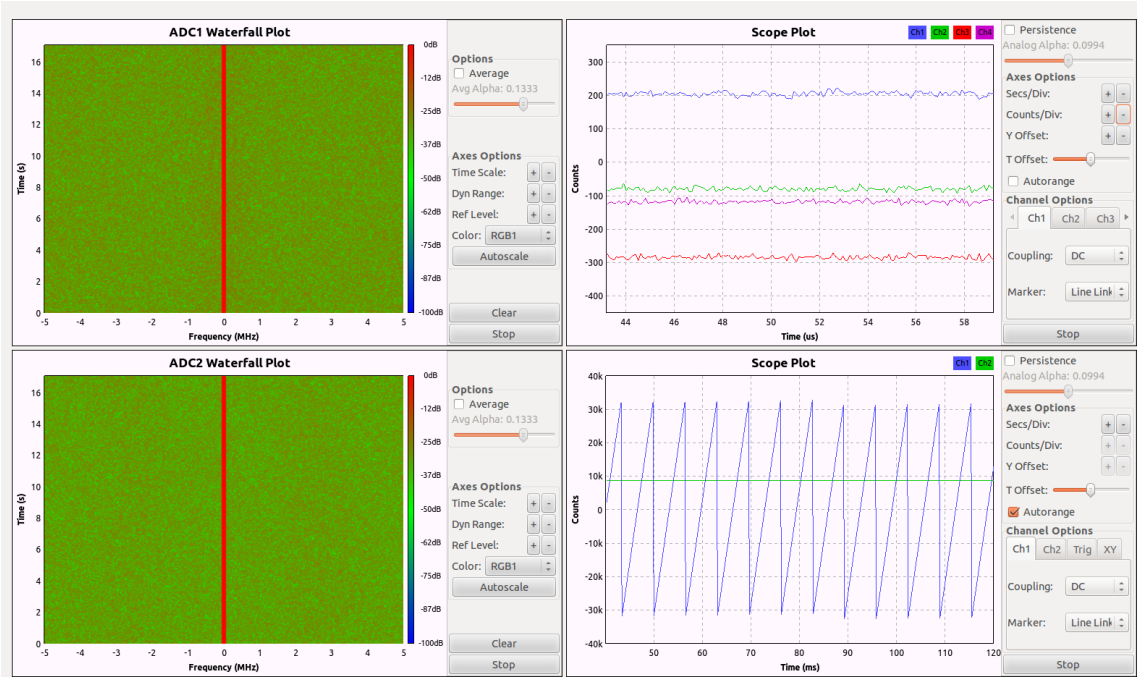


Figure 2.5. User interface window of a running ADC grabber.

Figure 2.6. Sine signal from ADC1 module with LTC21190 and LT6600-5 devices.

Figure 2.7. Sine signal from ADC1 module with LTC21190 and LT6600-5 devices.

Chapter 3
Proposed final system

Construction of a final system which is supposed to be employed for real radioastronomy observations will be described. This chapter is mainly a theoretical analysis of data handling systems. Realisation of these ideas might be possible as a part of our future development after we fully evaluate and test the current trial design.

3.1 Custom design of FPGA board

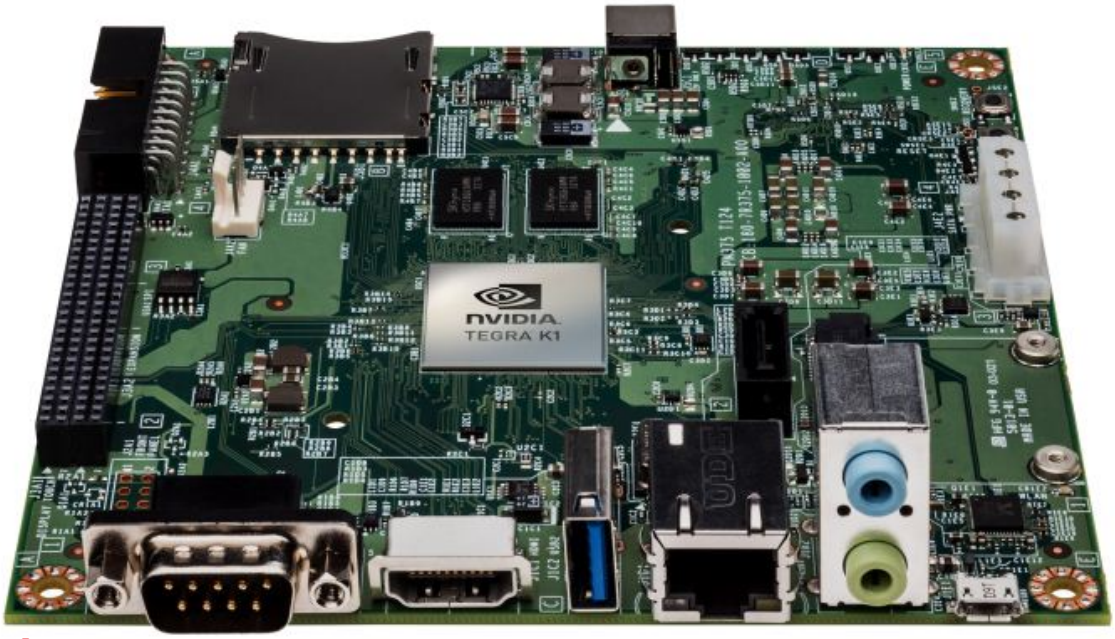
In the beginning of the project, a custom design of FPGA interface board had been considered. This FPGA board should include PCI express interface and should sell at lower price than trial design. It should be compatible with MLAB which is further backward compatible with the existing or improved design of ADC modules. For a connection of this board to another adapter board with PCIe we expect a use of a host interface. Thunderbolt technology standard was expected to be used in this PC to PCIe -¿ FPGA module. Thunderbolt chips are currently available on the market for reasonable prices. However, a problem lies in the accessibility to their specifications, as they are only available for licensed users and Intel has a mass market oriented licensing policy, that makes this technology inaccessible for low quantity production. As a consequence, an external PCI Express cabling and expansion slots should be considered as a better solution.

However, these systems and cables are still very expensive. Take (http://www.opalkelly.com/products/xe as an example, with its price tag reaching 995 USD at time of writing of thesis. Therefore, a better solution probably needs to be found.

3.2 Parralella board computer

3.3 GPU based computational system

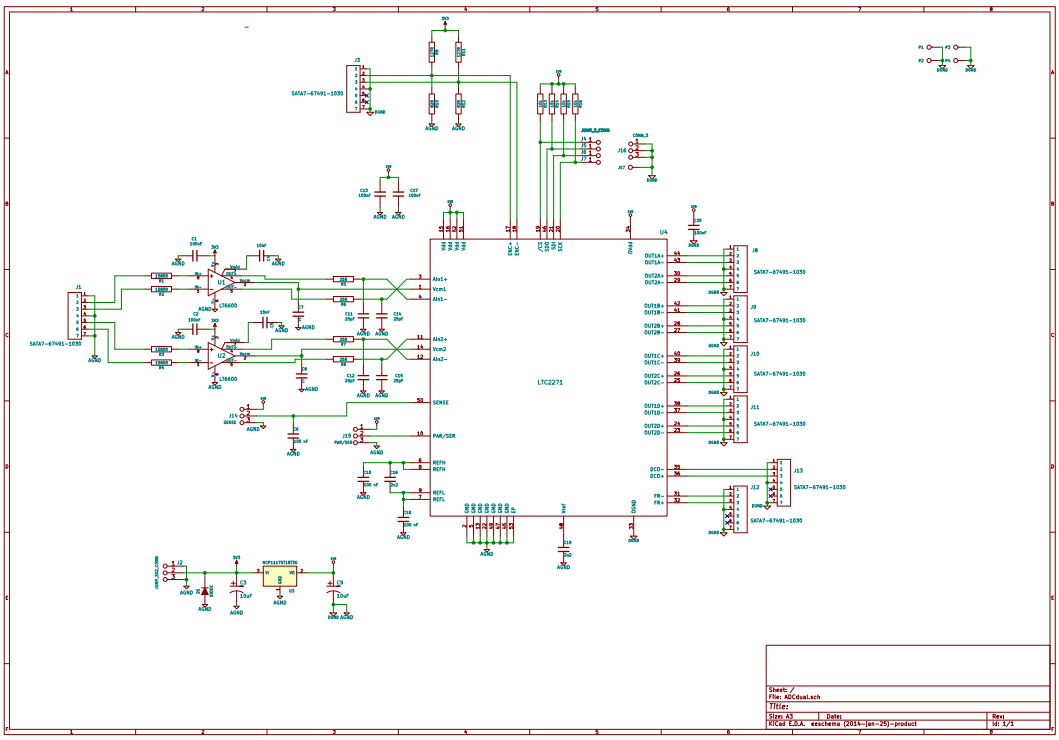
A new GPU development board NVIDIA K1, shown in the following picture 3.1, has recently been released. These boards are intended to be used in fields including computer vision, robotics, medicine, security or automotive industry. They have ideal parameters for signal processing for a relatively low price of 192 USD. Unfortunately, they are currently only in pre-order release stage (in April 2014).



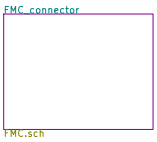
[img-NVIDIA-K1]

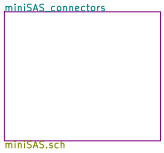
Figure 3.1. The NVIDIA Jetson TK1 Development Kit `https://developer.nvidia.com/jetson-tk1`.

Appendix A
Circuit diagram of ADCdual01A module



Appendix B
Circuit diagram of FMC2DIFF module





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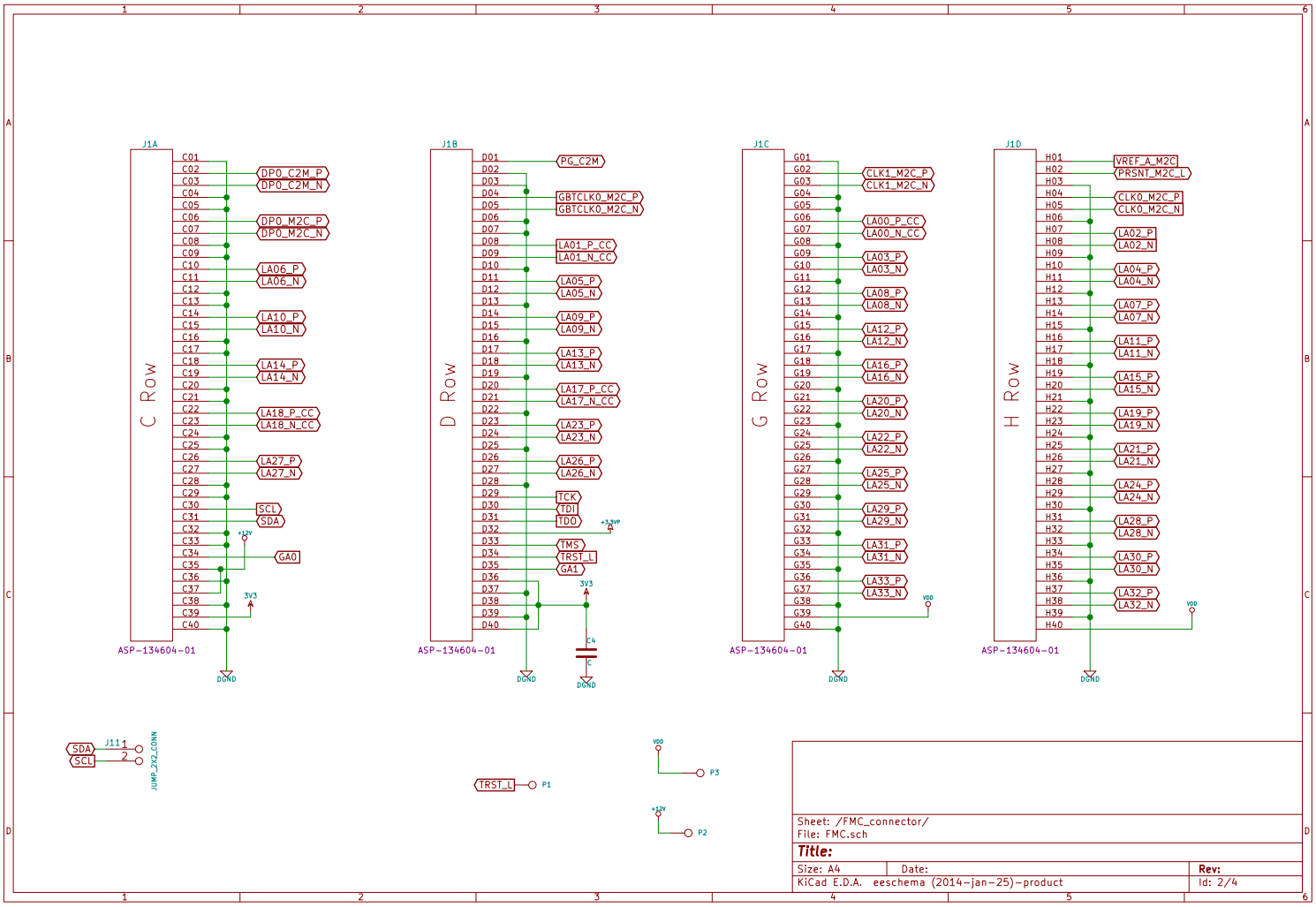
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C Row
C01 C02 C03 C04 C05 C06 C07 C08 C09 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40
DP0_C2M_P
DP0_C2M_N
DP0_M2C_P
DP0_M2C_N
LA06_P
LA06_N
LA10_P
LA10_N
LA14_P
LA14_N
LA18_P_CC
LA18_N_CC
LA27_P
LA27_N
SCL
SDA
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D Row
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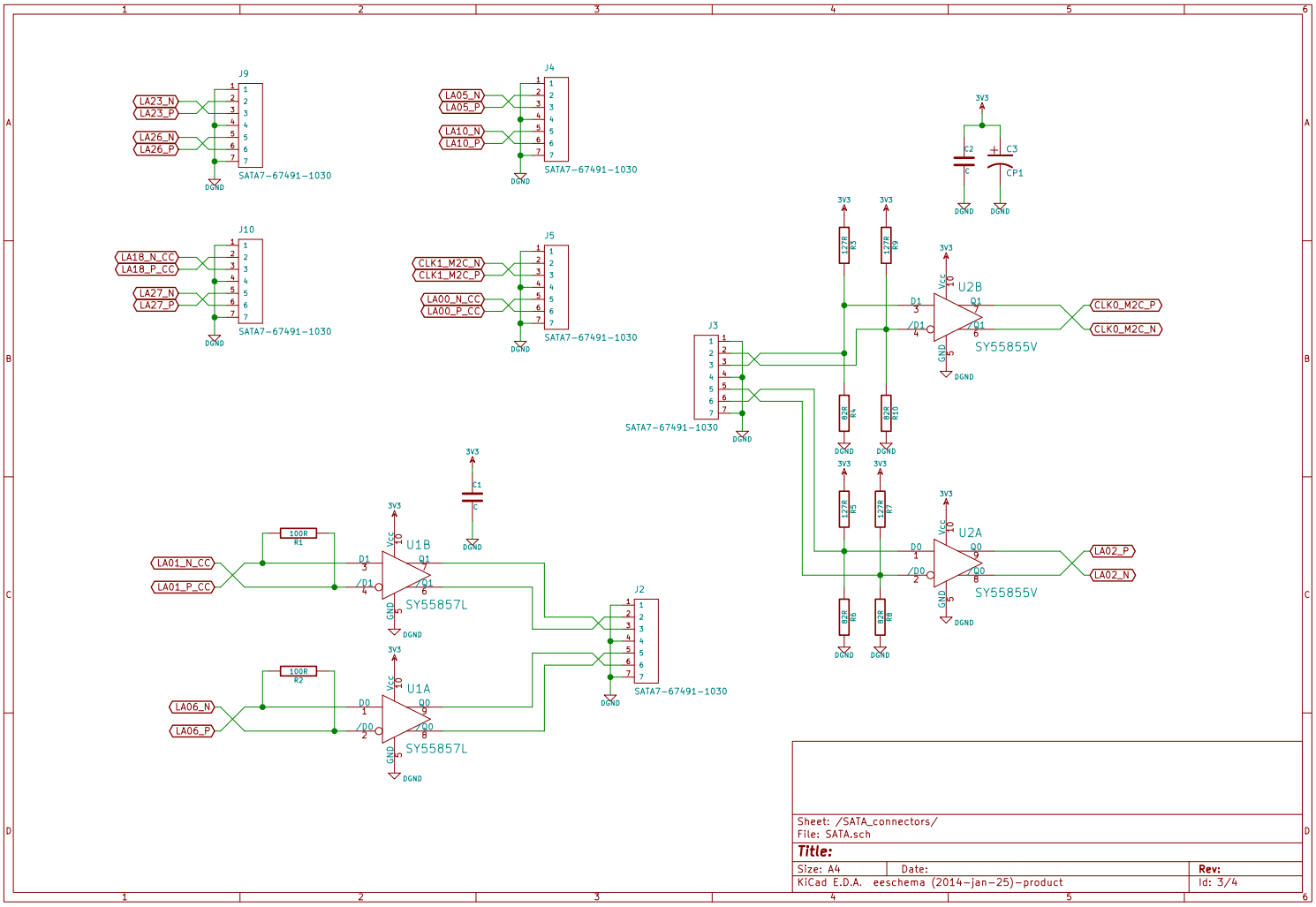
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3V3
C2
C3
CP1
DGND
J10
LA18_N_CC
LA18_P_CC
LA27_N
LA27_P
SATA7-67491-1030
DGND
J5
CLK1_M2C_N
CLK1_M2C_P
LA00_N_CC
LA00_P_CC
SATA7-67491-1030
DGND
J3
SATA7-67491-1030
DGND
127R
R3
R9
82R
R4
R10
U2B
SY55855V
CLK0_M2C_P
CLK0_M2C_N
U2A
LA02_P
LA02_N
R5
R7
R6
R8
C1
100R
R1
R2
U1B
U1A
SY55857L
LA01_N_CC
LA01_P_CC
LA06_N
LA06_P
J2
SATA7-67491-1030
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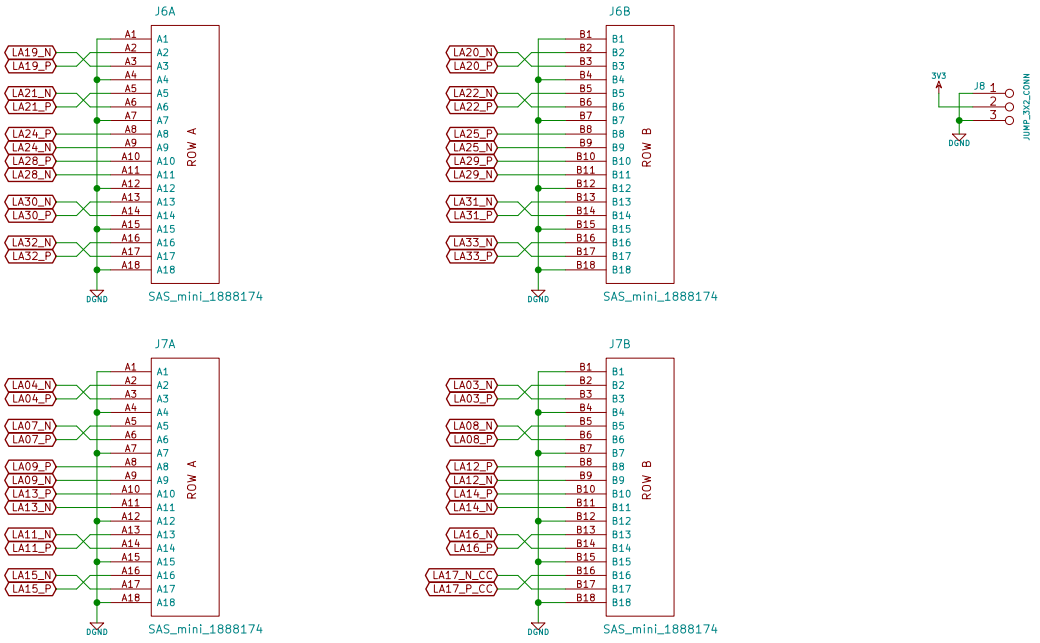

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