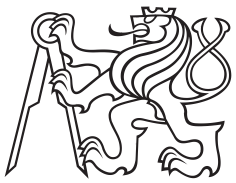
Master's thesis



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F3

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Fast multi-channel data acquisition system for radio-astronomy receiver

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Acknowledgement / Declaration

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V Praze dne 12. 5. 2014

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Abstrakt / Abstract

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Klíčová slova: Radioastronomie, digitalizace signálu, A/D konverze

Překlad titulu: Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač

.

Keywords: ADC interface, radioastronomy, signal digitalisation

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Chapter 1
Introduction

1.1 Current radioastronomy problems

From a radioastronomer's point of view it is important that radioastronomy focuses its interest primarily on natural signals originating in the surrounding universe. It does not pay much attention to the man-made signals created by our civilisation.

However, it is due to these artificial signals, that the current radioastronomy faces a disturbing problem. The problem arises from the fact, that there are so many terrestrial transmitters currently active and all of them are sources of a dense signal mixture which can cause trouble not only to radioastronomers.

As a consequence, there already exist effort to control the radiofrequency spectrum. As result of attempts to control the radiofrequency spectrum, the frequency allocation table was created [1]. Radio-frequency allocation table table contains special bands allocated to radioastronomy use. However, for many reasons these bands are not clean enough to be used directly in radioastronomy observations. As a result, we cannot work in the same way as had the radioastronomers in the very beginnings of radioastronomy. Many experiments, namely Cosmic microwave background detection or pulsar detection, cannot be nowadays realised in their original forms with satisfactory results.

Supporting evidence of such effect is RadioJOVE project. NASA engineers who originally created the RadioJOVE project had a great idea. The RadioJOVE project brought an opportunity for creating a publicly available, cheap radioastronomy receiver. However, they used an old-fashioned construction design which, on one hand, can operate in unoccupied harsh environments like deserts, but on the other it simply did not meet the criteria that would make it possible to be used in modern civilisation, as we know it in Europe [2]. The source of its dysfunction is a presence of strong radiofrequency interferences. These interferences are orders of magnitude stronger than Jupiter decametric emissions, whose detection was the main aim of the RadioJOVE project. From what we have already seen in the light pollution mitigation pursuit, there is only a small chance to radically improve the situation in radiofrequency spectrum.

The only way to overcome this problem is to search for new methods of radioastronomy observations. New methods which allows us to work without completely clear radiofrequency bands and which allow us to see the surrounding universe even despite the existence of man-made radiofrequency interference mixture. One solution is to use already known natural radio frequency signals parameters. Natural signals usually have different signal properties than local interference. Natural objects do not have problems with transmission in bandwidths of tens of megahertz in sub 100 MHz bands. These objects are usually far away and the same signal could be received at almost half of the Earth globe without any significant differences. On the other hand, it is obvious that signals with such parameters have some drawbacks, namely in the reception power. The reception power of radioastronomical object is $1 \cdot 10^9$ smaller than signal power received from a typical broadband radio transmitter.

From the above mentioned facts concerning the natural radio signals we can conclude that modern requirements imposed on a radioastronomy receiver are completely different from the requirements existing back in the history. Radioastronomy is no longer limited by an access to electronic components, today it is rather limited by the everywhere presence of electronic.

1.2 Modern Radio astronomy receiver

In the beginnings of radioastronomy, the receivers were constructed as simple stations with single antenna or multi antenna array with fixed phasing. This approach was used because of the existing limits of electronic components and technologies. The main challenges of those times were the problem of noise number and low sensitivity, both present due to the poor characteristics of active electronic components such as transistors and vacuum tubes.

Most of the present-day operating radioastronomy equipment has been constructed in similar manner. It was produced usually shortly after the WWII or during The Cold War as a part of military technology.

Today we have an access to components having quality, repeatability and price completely different from the components accessible by previous generation of radioastronomers. That is why we can develop better radioastronomical equipment, powerful enough to make new astronomical discoveries possible.[1])

We have the capacities necessary to develop a receiver which will have wide bandwidth, high Third-order intercept point and preferably an option for phase and frequency locking to other receivers located at another radioastronomical site at Earth. Currently there exist several receivers with the above-mentioned parameters, for example USRP2, USRP B210 or HackRF and all are commercially available. However all of them lack scalability and have high prices. It is exactly the scalability and redundancy that are the main requirements of noise reduction algorithms.

New radio astronomy systems such LOFAR are explicit examples of the scalability and redundancy approach. LOFAR has completely different and novel structure developed to solve the problems of radioastronomy signal reception. It exclusively uses multi antenna arrays and mathematical algorithms for signal handling. Radio signals recorded by LOFAR can be used in multiple ways: radio images can be computed (if sufficient cover of u/v plane is achieved), radiation intensity can be measured, spectrum can be analysed for velocity measurement, etc.

1.2.1 Observation types

Current radioastronomy knows several types of observations.

- Spectral observations
- Intensity observations
- Velocity observations

All of them prefer high frequency resolution and stability. Wide observation bandwidth in hundreds of MHz is usually desirable for easier differentiation of source types.

[1]) Most of astronomy-related discoveries in the last fifty years came from radioastronomy.

1.3 Required receiver parameters

The novel approach of receiver construction described above goes hand-in-hand with new requirements on receiver parameters as well. Currently no additional attempts to improve the signal-to-noise ratio on single antenna are performed. There are however other parameters requested nowadays.

1.3.1 Sensitivity and noise number

Sensitivity and noise number are parameters that are tied together, but multi antenna and multi-receiver arrays force the price of receiver to be kept at minimal value. This implies that the sensitivity and noise number have to be at least so good in the detection (signal / noise > 1) of an observed object, that it would be detected on the majority of receivers connected to an observation network.

1.3.2 Dynamic range

Dynamic range represents a huge problem of current radioastronomical receivers. This parameter is enforced by everywhere present humans made EMI radiation on RF frequencies. The modern radio astronomy receiver must not be saturated by this high levels of signals but still needs to have enough sensitivity to see faint signals from natural sources. Dynamic range is limited either by the construction of analogue circuitry in receiver or by the digitalisation unit. The maximal theoretical dynamic range of ADC could be estimated from ADC bit depth using a following formula (1)

[dynamic-range]

$$D.R.[dB] = 20 \cdot \log(2^n) \tag{1}$$

The formula (1) gives values shown in table below 1.1.

[ADC-dynamic-range]

ADC Bits	Dynamic range [dB]
8	48
10	60
12	72
14	84
16	96
24	144

Table 1.1. Standard bit depths of ADC and its theoretical dynamic range.

If we look at actual spectrum occupancy in Europe (measured in power spectral density) we see that signal dynamic range in spectra easily reaches more than 80 dB above natural noise levels [3]. If we don't want to deal with receiver saturation or poor sensitivity we need a receiver and digitalization unit which has comparable dynamical range of with received signals. This imply use of least 14 bit ADC without any spare of range. But 16 bit range should be optimal as we have spare range for strongest RF signals. Two bytes sample range has in addition a good efficiency in use standard power of 2 data types length. We lock for use 16bit digital range as optimal for our design.

1.3.3 Bandwidth

Historically, the parameter of bandwidth in radioastronomical receiver used to be within the kilohertz range. Small bandwidth was acceptable because observations were processed directly by listening or by paper chart intensity recorder. Chart recorder integrated energy of signal over defined small bandwidth which was suitable for detecting

the intensity variance of microwave background. No wide-band transmitters existed in that era (except for TV transmitters) and tuning to other neighbouring frequency was easy as they were mostly vacant. Parallel observations from several places were unnecessary as well because the electromagnetic conditions were nearly same at all locations.

1.4 Current status of receivers digitalization units

Only few digitalization systems dedicated for radioastronomy currently exists. Currently existing systems uses either custom design of whole receiver or they are constructed from commercially available components. Open-source principle attempts are very rare in radioastronomy field.

1.4.1 Custom digitalization system

Custom designs usually uses non-recurring engineering for development specific solution for observation project thus costs of this instruments are very high if developed instrument are not reproduced many times. Typical example of instrument developed and manufactured in one piece with enormous founding resources draws is Arecibo ALFA survey multi beam feed Array. Another opposite example for custom receiver and digitalization unit design is LOFAR system developed by Astron in Netherlands [4].

LOFAR is innovative radioastronomy system which uses the phased antenna array approach in enormous scale and thousands (around $2{\cdot}10^4$) of antennas are manufactured an deployed on field. The centrer of LOFAR system is situated in Netherlands and peripheral antennas and connection network are extended to other European countries.

[lofar-antenna]

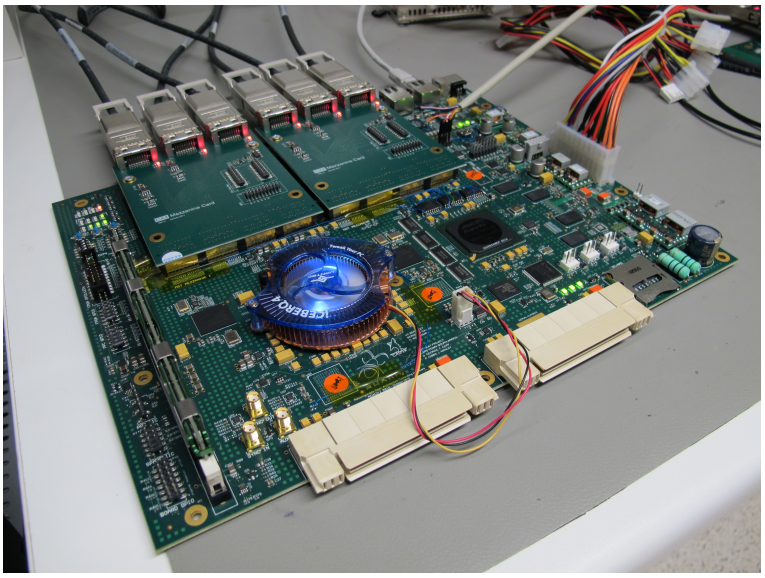
Figure 1.1. One LOFAR LBA antenna element.

LOFAR project must use low cost hardware due to systems scale. Special construction techniques are used to keep overall project budget at acceptable levels (specially designed polystyrene supporting blocks for HBA antennas for example). Many of used components are manufactured in mass scale for other than scientific use LBA antennas masts are made from standard PVC plastic waste pipes and LOFAR uses low cost direct

sampling receiver. Whole project has been designed by Netherlands Institute for Radio Astronomy, which produces many similarly sophisticated devices[5].

1.4.2 Modular digitalization systems

Due to cost restrictions in science and astronomy instruments development, an reuse of engineering work should be useful. One modular digitalization and data processing system currently exit. It is being developed at Berkley[6]. CASPER is in development from around 2005. CASPER's designers an engineers remarkably noticed a lack of such hardware in radioastronomy science, theirs ideas are summarised in paper [7]. Unfortunately they use proprietary connector standard and technology and develops modular system based purely on Tyco Z-DOK+ connectors family. CASPER data processing board with Z-DOK connectors is shown in picture 1.2. Z-DOK connectors have relatively high pricing (around 40 USD) [8]. Z-DOK connectors are high quality differential pairs connectors, but price of these connectors is comparable with value of one ADC channel in our design described in following part of document.



[casper-roach]

Figure 1.2. CASPER project ROACH-2 data processing board. White Z-DOK connectors for daughter ADC Boards can be easily seen in front.

In opposite to professional astronomers which uses proprietary digitalization units, amateur radioastronomers currently uses multichannel sound cards [9] or self designed digitalisation units. Devices constructed by amateurs are usually non reproducible [10] . It is evident that current radioastronomy lacks of proper hardware which could be used on both communities - professionals and amateurs. Optimal solution for this situation should be open-source hardware.

Chapter 2
Trial design

The whole design of radioastronomy receiver digitalization unit is constructed to be used in a wide range of applications and tasks related to digitalization of signal from radioastronomy receivers. A good illustrating problem for its use is a signal digitalisation from multiple antenna arrays.

2.1 Required parameters

We require following technical parameter, to supersede existing digitalization units solutions. Primarily, we need wide dynamical range and high IP3. The receiver must accept wide dynamic signals because a typical radioastronomical signal has a form of a weak signal covered by a strong man-made noise or other undesired noises as lighting, Sun emissions etc.

Summary of other additional required parameters follows

- Dynamical range better than 80 dB see section ?? for explanation
- Phase stability between channels
- Low noise (all types)
- Sampling jitter better than 100 metres
- Support for any number of receivers in range 1 to 8

Now we analyzes several parameters more precisely.

2.2 Sampling frequency

Sampling frequency is not limited by the technical constrains in the trial design. This parameter is especially limited by the sampling frequencies of analog-to-digital conversion chips available on the market and interface bandwidth. Combination of the required parameters – dynamic range requiring at least 16bit and a minimum sampling frequency of 1 MSPS leads to need of high end ADC chips which does not support such low sampling frequencies at all. Their minimum sampling frequency is 5 MSPS.

We calculate minimum data bandwidth data rate for eight receivers, 2 bytes per sample and 5 MSPS as $8 \cdot 2 \cdot 5 \cdot 10^6 = 80$ MB/s. Such data rate is at the limit of real writing speed o classical HDD and it is almost double of real bandwidth of USB 2.0 interface. As result of this facts we must use faster interface. Faster interface is especially needed in case where we need faster sampling rates than ADC minimal 5 MSPS sample rate. Most perspective interfaces for use in our type of application is USB 3.0 or PCI Express interface. Although USB 3.0 is new technology without availability of good development tools. We used PCI Express interface as simplest and most reliable solution.

2.3 System scalability

For analogue channels scalability, special parameters of ADC modules are required. Ideally, there should be a separate output for each analogue channel in ADC module. ADC module must also have separate outputs for frames and data output clocks. These parameters allow for conduction at relatively low digital data rates. As a result, the digital signal can be conducted even through long wires. Modular concept allows separation from central logic which support optimization of number analogue channels.

Clock and data signals will be then handled distinctively in our modular scalable design. Selected ADC chip are guaranteed to have defined clock skew between sampling and data output clock. This allows taking data and frame clocks from the first ADC module only. The rest of the data and frame clocks from other ADC modules can be measured for diagnostic purposes (failure detection, jitter measurement etc.) but these redundant signals are not used for data sampling. If more robustness is required in final application, DCO and FR signal may be collected from other modules and routed through an voting logic which will correct possible signal defects.

This system concept allows for scalability, that is technically limited by a number of differential signals on host side and its computational power. There is another advantage of scalable data acquisition system – an economic one. Observatories or end users can make a choice of how much money are they willing to spent on radioastronomy receiver system. This freedom of choice is especially useful for science sites without previous experience in radioastronomy observations.

2.3.1 Differential signaling

The above mentioned concept of scalable design requires relatively long circuit traces between ADC and digital unit which captures the data and performs the computations. The long distance between the digital processing unit and the analog-to-digital conversion unit has an advantage in noise retention typically produced by digital circuits. Those digital circuits, such as FPGA, Ethernet or other flip-flops blocks and circuit traces, usually work at high frequencies and emit wide-band noise with relatively low power. In such cases any increase in a distance between the noise source and analog signal source increase S/N significantly. However, at the same time a long distance brings problems with the digital signal transmission between ADC and computational unit. But this obstacle should be resolved more easily in free-space than on board routing. The high-quality differential signalling shielded cables should be used such as massively produced and cheap SATA cables. This technology has two advantages over PCB signal routing. First, it can use twisted pair of wires for leak inductance suppression in signal path and second, the twisted pair may additionally be shielded by uninterrupted metal foil.

2.3.2 Phase matching

For multiple antenna radioastronomy projects, system phase stability is a mandatory condition. It allows precise high resolution imaging of objects, increases signal to noise ratios in several observation methods and allows use of advanced algorithms for signal processing.

High phase stability in our scalable design is achieved through centralized frequency generation and distribution with multi-output LVPECL hubs (CLKHUB02A), that have equiphased outputs for multiple devices. LVPECL logic is used on every system critical clock signal distribution hub. LVPECL logic has advantage over LVDS in signal

integrity robustness. LVPECL uses higher logical levels and higher signalling currents. Power consumption of LVPECL logic are near constant over operating frequency range due to use of bipolar transistors this minimizes voltage glitches which are typical for CMOS logic. One drawbacks of that parameters is high power consumption of LVPECL logic which easily reach tens of milliamperes per device.

This design ensures that all system devices have access to the defined phase and known frequency.

2.4 System description

In this section testing system based on Xilinx ML605 development board 2.5 will be described. This board was used in previous finished project and was unused until now, but FPGA parrameters are more than enough we need in fast data aquisition system.

2.4.1 Frequency synthesis

We have used a centralized topology as a basis for frequency synthesis. One precise high-frequency and low-jitter digital oscillator has been used [11], while other working frequencies have been derived from it by the division of its signal. This central oscillator has a software defined GPS disciplined control loop for frequency stabilization.[1]) We have used new methods of software frequency monitoring and compensation in order to meet modern requirements on radioastronomy equipment which needs precise frequency and phase stability over a wide baseline scales for effective radioastronomy imaging.

GPSDO device consists the Si570 chip with LVPECL output. Phase jitter of GPSDO is determined mainly by Si570 phase noise. Parameters of used Si570 from source [12] are summarized in table 2.1.

GPSDO design included in data acquisition system has special feature – generates time marks for precise time-stamping of received signal. Timestamps are created by disabling of local oscillator outputs connected to SDRX01B receivers for 100 us. As result rectangle click in ADC input signal is created which appears as horizontal line in spectrogram. Timestamps should be seen in image 3.2 (above and below meteor reflection).

Time-marking should be improved in future by digitalization of GPS signal received by antenna on observational station. GPS signal can be then directly sampled by dedicated receiver and one separate ADC module. Datafile then consists samples from channels of radio-astronomy receivers along with GPS signal containing precise time information.

Every ADC module will be directly connected to CLKHUB02A module which takes sampling clock signal delivered by FPGA from main local oscillator. This signal should use high quality differential signaling cable – we should use SATA cable for this purpose. FPGA may slightly affect clock signal quality by additive noise, but has negligible effect in application where developed system will be used.

2.4.2 Signal cable connectors

Several widely used and commercially easily accessible differential connectors were considered to be use in our design.

- HDMI

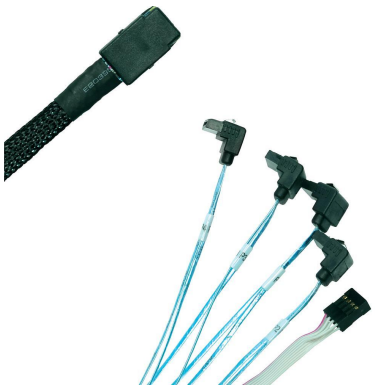
[1]) SDGPSDO design has been developed in parallel to this diploma thesis as a related project, but it is not explicitly required by the diploma thesis. Thus is described in separate document

	Phase Noise [dBc/Hz]	
Offset Frequency	F_{out} 156.25 MHz	F_{out} 622.08 MHz
100 [Hz]	–105	–97
1 [kHz]	–122	–107
10 [kHz]	–128	–116
100 [kHz]	–135	–121
1 [MHz]	–144	–134
10 [MHz]	–147	–146
[LO-noise] 100 [MHz]	n/a	–148

Table 2.1. Phase noise of used Silicon Laboratories Si570 chip. Offset frequency is measured from carrier frequency. Values are tabled for two district carrier frequencies.

- SATA
- DisplayPort
- SAS/miniSAS

At the end, MiniSAS connector was chosen as the best option to be used in connecting together multiple ADC modules. A transition between SATA and miniSAS is achieved by SAS to SATA adapter cable which is commonly used in servers to connect SAS controller to multiple SATA hard disc in RAID systems and thus is commercially easily available. It is compatible with existing SATA cabling systems and aggregates multiple SATA cables to a single connector, it has SPI configuration lines which can be seen on the following picture 2.1 as standard pinheader connector. The main drawback of miniSAS PCB connectors lies in the fact, that they are manufactured in SMT versions only, SMT design may eventually decrease the durability of the connector even if outer metal housing of connector is designed to be mounted using a standard through-hole mounting method.



[img-miniSAS-cable]

Figure 2.1. An example of miniSAS cable similar to used.

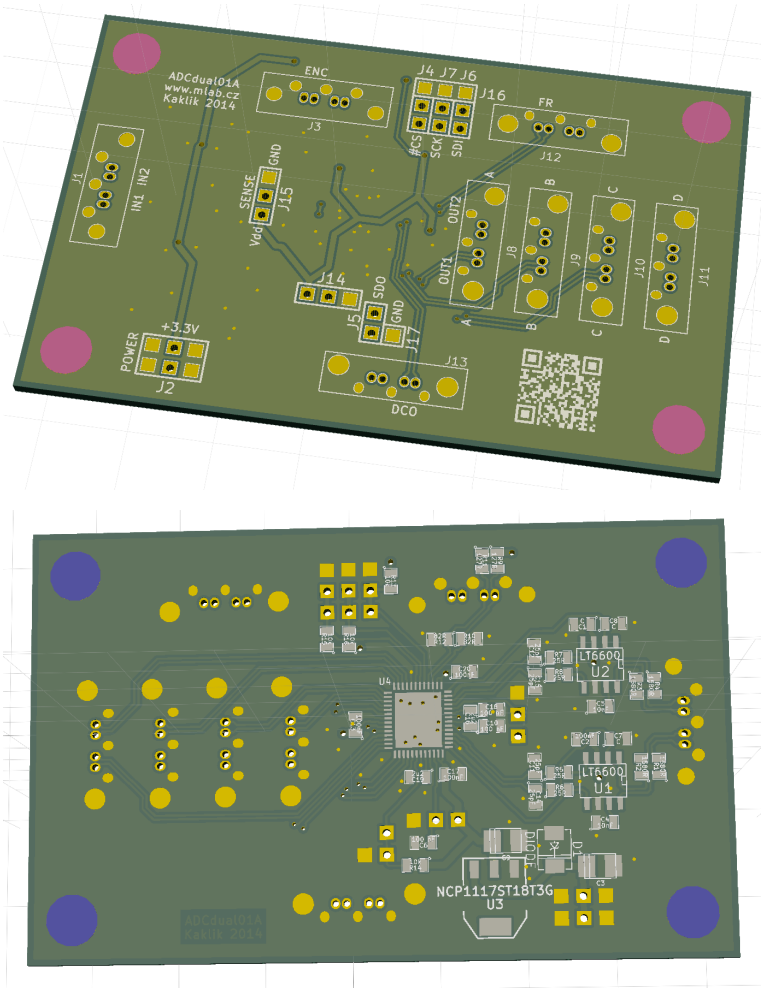
2.4.3 Signal integrity requirements

We use ADC devices that have DATA clock frequency eight times higher than sampling frequency in single line output mode, implying a 40 MHz output bit rate. This imply $1/4 \cdot 10^7 = 25$ ns time length of data bit, which is equivalent to 7.5m light path in free space. If we use copper PCB with FR4 substrate layer or coaxial/twinax cable, we could obtain velocity factor of 0.66 at worst condition. Then the light path for the same bit rate t_s will be 4.95 m. Although we do not have any cables in system with comparable lengths, worst data bit skew described by data sheets of used components is $0.3 \cdot t_s$, which is 1.485 m. Therefore length matching is not critical in our current

design operated on lowest sampling speed. Length matching becomes critical in future version with higher sampling rates, then cable length must be matched. However SATA cabling technology is prepared for that case and matched SATA cables are standard merchandise.

[diff-signaling]

2.4.4 ADC modules design



[adcdual-preview]

Figure 2.2. Modelled previews of designed and realised PCB of ADCdual01A modules. Differential pairs routing are clearly visible.

2.4.5 ADC selection

There exist several standard ADC signaling formats currently used in communication with FPGA.

- DDR LVDS
- JEDEC 204B
- JESD204A
- Paralel LVDS
- Serdes
- serial LVDS

Because we need to use the smallest number of cables, the choice fell on the serial LVDS format. Small number of differential pairs is an important parameter determining

the construction complexity and reliability[13]. No much many currently existing ADC devices have this kind of digital interface. An ultrasound AFE device chips seems to be ideal for this purpose – the chip has integrated both front-end amplifiers and filters. It has a drawback though - it is incapable of handling differential input signal and has a relatively low dynamic range (as it consists only of 12bit ADC) and has many single ended ADC channels. Consequently scaling is possible only by a factor of 4 receivers (making 8 analogue single ended channels).

If we add a requirement of separate output for every analogue channel and a 16bit depth we find that there are only a few 2-Channel simultaneous sampling ADCs currently existing which meet these requirements. We have summarized those ADCs in the following table 2.2

ADC Type	LTC2271	LTC2190	LTC2191	LTC2192	LTC2193	LTC2194	LTC2195
SNR [dB]	84.1	77	77	77	76.8	76.8	76.8
SFDR [dB]	99	90	90	90	90	90	90
S/H Bandwidth [MHz]	200			550			
Sampling rate [MSPS]	20	25	40	65	80	105	125
Configuration				SPI			
[ADC-Typeset] Package				52-Lead (7mm × 8mm) QFN			

Table 2.2. The summary of available ADC types and theirs characteristics.

All parts in this category are compatible with one board layout. Main differences lay in the sampling frequency and signal to noise ratio, with the slowest having a maximum sampling frequency of 20 MHz. However all of them have a minimal sampling frequency of 5 MSPS and all are configurable over a serial interface (SPI). SPI seems to be a standard interface used in high-end ADC chips made by the largest manufacturers (Analog Devices, Linear technology, Texas instruments, Maxim integrated..). We selected two slowest types for our evaluation design. Then PCB for this part have been designed. We decided that ADCdual01A modules have a standard MLAB construction layout with four mounting holes in corners aligned in defined raster of 400 mils.

Data serial data outputs of ADC modules should be connected directly by LVDS signalling levels conducted by SATA cables to FPGAs for the basic primary signal processing. The ADC chips used in the modules has a selectable bit width of data output bus and thus the output SATA connectors have signals arranged to contain a single bit from every ADC channel. This creates a signal concept enabling a selection of a proper bus bit-width according to the sampling rate (higher bus bit-width downgrades signalling speed and vice versa.)

In order to connect the above mentioned signalling layout, miniSAS to multiple SATA cable should be used as described in section ??.

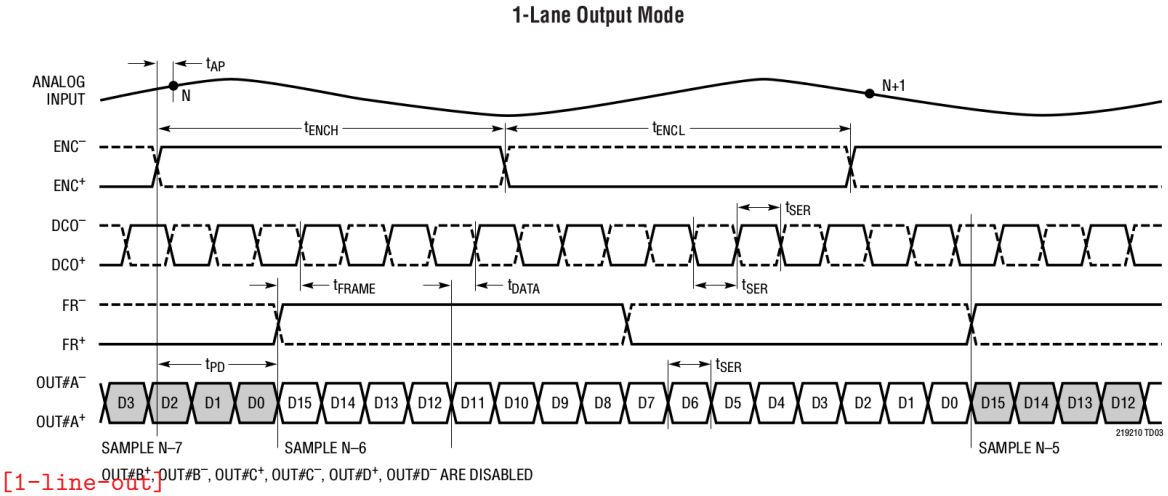
A KiCAD design suite had been chosen for PCB layout. However, the version is, despite having integrated CERN Push & Shove routing capability, slightly unstable as it sometimes crushes due to an exception during routing. On the basis of these stability issues, the design had to be saved quite often. On the other hand, compared to commercially available solutions, such as MentorGraphics PADS or Cadence Orcad, the Open-source KiCAD provides an acceptable option and it easily surpasses a widely used Eagle software.

As a part of work on the thesis, new PCB footprints for FMC, SATA, ADCs a and miniSAS connectors have been designed and were committed to KiCAD github library repository. They are now publicly available on the official KiCAD repository at GitHub.

ADCdual01A module has several digital data output formats. Difference between these modes lays in the number of differential pairs used.

- 1-lane mode
- 2-lane mode
- 4-lane mode

All of the above-mentioned modes are supported by the module design. For the discussed data acquisition system, the 1-lane mode was selected. 1-lane mode allows a minimal number of differential pairs between ADCdual01A and FPGA. Digital signalling scheme used in 1-lane mode is shown in the following image 2.3.



[1-line-out]

Figure 2.3. Digital signalling schema for 1-line ADC digital output mode.

ADCdual01A parameters can be set either by jumper setup (referred to as a parallel programming in the device's data sheet) or by SPI interface. SPI interface has been selected for our system, because of the parallel programming lack of options (test pattern output setup for example).

Complete schematic diagram of ADCdual01A module board is included in the appendix.

2.4.6 ADC modules interface

Both of the ADCdual01A modules were connected to FPGA ML605 board trough FMC2DIFF01A adapter board. The design of this adapter expects the presence of FMC LPC connector on host side and the board is, at the same time, not compatible with MLAB. It is, on the other hand, designed to meet the VITA 57 standard specifications for boards which support region 1 and region 3. VITA 57 regions are explained in the picture 2.6. This industry standard guarantees the compatibility with other FPGA boards that have FMC LPC connectors for Mezzanine Card. Schematic diagram of designed adapter board is included in the appendix.

The primary purpose of the PCB is to enable the connection of ADC modules located outside the PC case with ML605 development board. (In PC box analog circuits cannot be realized without the use of massive RFI mitigation techniques). Differential signaling connectors should be used for conducting digital signal over relatively long cables. The signal integrity sensitive links (clocks) are equipped with output driver and translator to LVPECL logic for better signal transmission quality.

LVPECL level signal connectors on FMC2DIFF01A board are dedicated for clock signals. We selected the SY55855V and SY55857L dual translators. Dual configuration in useful due to fact that SATA cable contains two differential pairs.

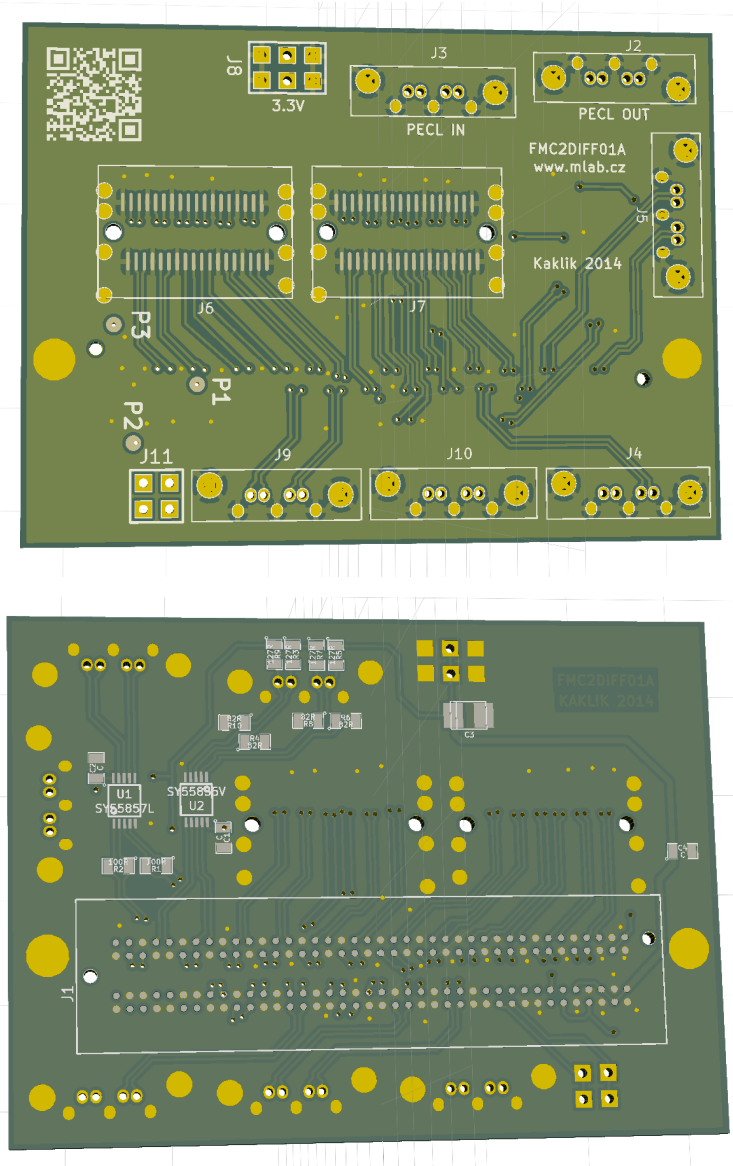
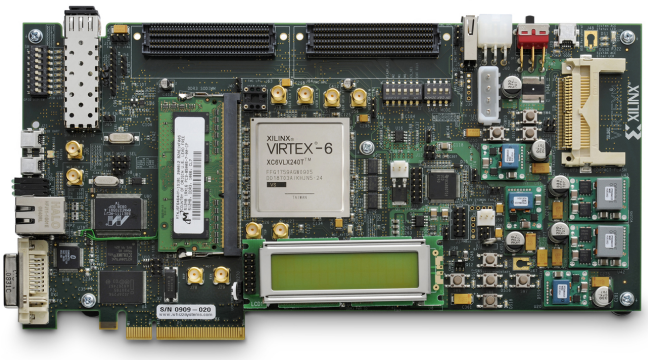


Figure 2.4. Modelled prewievs of designed and realised PCB of FMC2DIFF01A module.

The SY55855V is a fully differential, CML/PECL/LVPECL-to-LVDS translator. It achieves LVDS signaling up to 1.5Gbps, depending on the distance and the characteristics of the media and noise coupling sources. LVDS is intended to drive 50 Ω impedance transmission line media such as PCB traces, backplanes, or cables. SY55855V inputs can be terminated with a single resistor between the true and the complement pins of a given input [14].

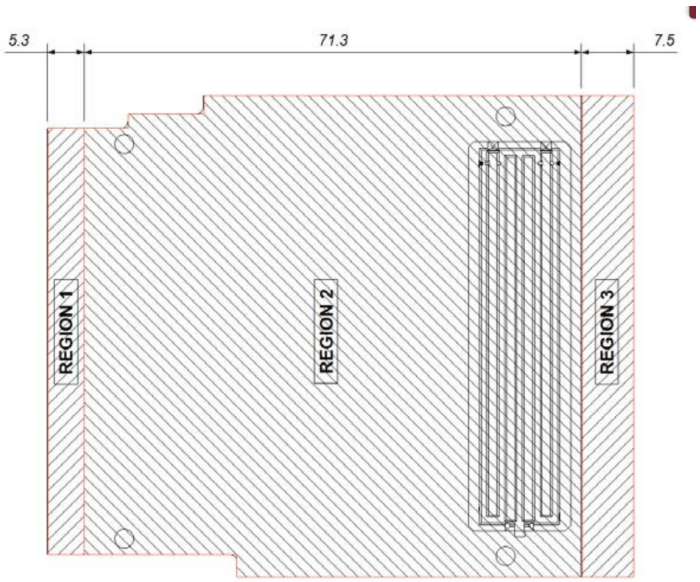
The SY55857L is a fully differential, high-speed dual translator optimized to accept any logic standard from single-ended TTL/CMOS to differential LVDS, HSTL, or CML and translate it to LVPECL. Translation is guaranteed for speeds up to 2.5Gbps (2.5GHz toggle frequency). The SY55857L does not internally terminate its inputs, as different interfacing standards have different termination requirements[15].

Inputs of both used chips are terminated accordingly to used logic. The LVDS input is terminated differentially by 100 Ω resistor between positive and negative inputs. PECL input is terminated by Thevenin resistor network. Thevenin termination method was selected as optimal due to absence of proper power voltage (1,3 V) for direct termination



[ML605-development-board]

Figure 2.5. FPGA ML605 development board.



[VITA57-regions]

Figure 2.6. Definition of VITA57 regions.

by 50 Ω resistors. Termination on FPGA side is realized directly by settings proper digital logic type on input pins.

Several SATA connectors and two miniSAS connectors are populated on this board. This set of connectors allows a connection of any number of ADC modules within the range of 1 to 8. ADC data outputs should be connected to the miniSAS connectors, while other supporting signals should be routed directly to SATA connectors on adapter.

Lengths of differential pairs routed on PCB of the module are not matched between the pairs. Length variation of differential pairs is not critical in our design according to facts discussed in paragraph 2.4.4. Nevertheless, signals within differential pairs themselves are matched for length. Internal signal trace length matching of differential pairs is mandatory in order to minimize jitter and avoid a dynamic logic hazard conditions on digital signals in worst case. Thus clocks signals are routed in the most precise way on all designed boards.

miniSAS	SATA pair	FMC signal	Used as
P0	1	LA03	not used
P0	2	LA04	not used
P1	1	LA08	not used
P1	2	LA07	not used
P2	1	LA16	ADC1 CH1 (LTC2190)
P2	2	LA11	ADC1 CH2 (LTC2190)
P3	1	LA17	ADC2 CH1 (LTC2271)
P3	2	LA15	ADC2 CH2 (LTC2271)

[minisas-interface]

Table 2.3. miniSAS (FMC2DIFF01A J7) signal connections between modules.

SPI connection J7	FMC signal	Connected to
SAS-AUX1	LA14_N	SPI DOUT
SAS-AUX2	LA14_P	SPI CLK
SAS-AUX3	LA12_N	CE ADC1
SAS-AUX4	LA12_P	CE ADC2
SAS-AUX5	LA13_N	soldered to GND
SAS-AUX6	LA13_P	not used
SAS-AUX7	LA09_N	not used
SAS-AUX8	LA09_P	soldered to GND

[SPI-system]

Table 2.4. SPI system interconnections

Signal configuration used in our trial design is described in the following tables 2.3, 2.4 and 2.5.

SPI interface is used in an unusual way in this design. SPI Data outputs from ADCs are not connected anywhere and read back is not possible, thus the configuration written to registers in ADC module cannot be validated. We have not observed any problems with this system, but it may be a possible source of failures.

Signal	FMC signal	FMC2DIFF01A	ADCdual01A
DCO	CLK1_M2C	J5-1	J13-1
FR	LA18_CC	J10-1	J12-1
ENC	LA01_CC	J2-1(PECL OUT)	J3-1
SDCPSDO01A_LO	CLK0_M2C	J3-1 (PECL IN)	N/A

[clock-interconnections]

Table 2.5. Clock system interconnections

2.4.7 FPGA function

Several tasks in separate FPGA blocks are performed by FPGA. In first block FPGA prepares sampling clock for ADCdual01A modules by division of main local oscillator. This task is separate block in FPGA and runs asynchronously to other logical circuits. Second block is SPI configuration module, which sends configuration words to ADC modules it is activated by opening of Xillybus interface file. Third block represents the main module, which resolves ADC - PC communication itself it communicates via PCIe, collect data from ADC hardware and creates data packet 2.6. Last block is activated after ADC configuration via SPI.

Communication over PCIe is managed by proprietary IP Core and Xillybus driver, which transfers data from FPGA registers to host PC. Data appear in system device

	160bit packet							
Data name	FRAME	ADC1 CH1		ADC1 CH2		ADC2 CH1		ADC2 CH2	
Data type	uint32	int16	int16	int16	int16	int16	int16	int16	int16
Content	saw signal	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}

[xillybus-interface]

Table 2.6. System device `/dev/xillybus_data2_r` data format

file named `/dev/xillybus_data2_r` on the host computer. Binary data which appear in this file after its opening are described in the table below 2.6.

Data packet block which is carried on PCI Express is described by table 2.6. The data packet consist several 32bit words. First word contain FRAME number and it is filled by saw signal for now, with increment step of every data packet transmission. Following data words contains samples from ADCs for first and second channel. Samples from every channel is transmitted in pairs of two samples. Number of ADC channels is expandable according to number of physically connected channels. An CRC word may be added in future at end of transmission packet for data integrity validation.

FRAME word at beginning of data packet now filled with incrementing and overflowing saw signal is used for ensure that no data samples ale lost during data transfers from FPGA. FRAME signal may be used in future for pairing the ADC samples data packet with another data packet in future. This new additional data packet should carry metadata information about sample time jitter, current accuracy of local oscillator frequency etc.

Detailed description of currently implemented FPGA functions can be found in separate paper [16]. HDL source codes for FPGA at state which was used are included on enclosed CD. Future development versions are publicly available from MLAB sources repository.

2.4.8 Data reading and recording

In order to read the data stream from the ADC drive, we use Gnuradio software. Gnuradio suite consists of gnuradio-companion package which is a graphical tool for creating signal-flow graphs and generating Python flow-graph source code. This tool was used to create a basic RAW data grabber to record and interactively view waterfall plots the data streams output from ADC modules.

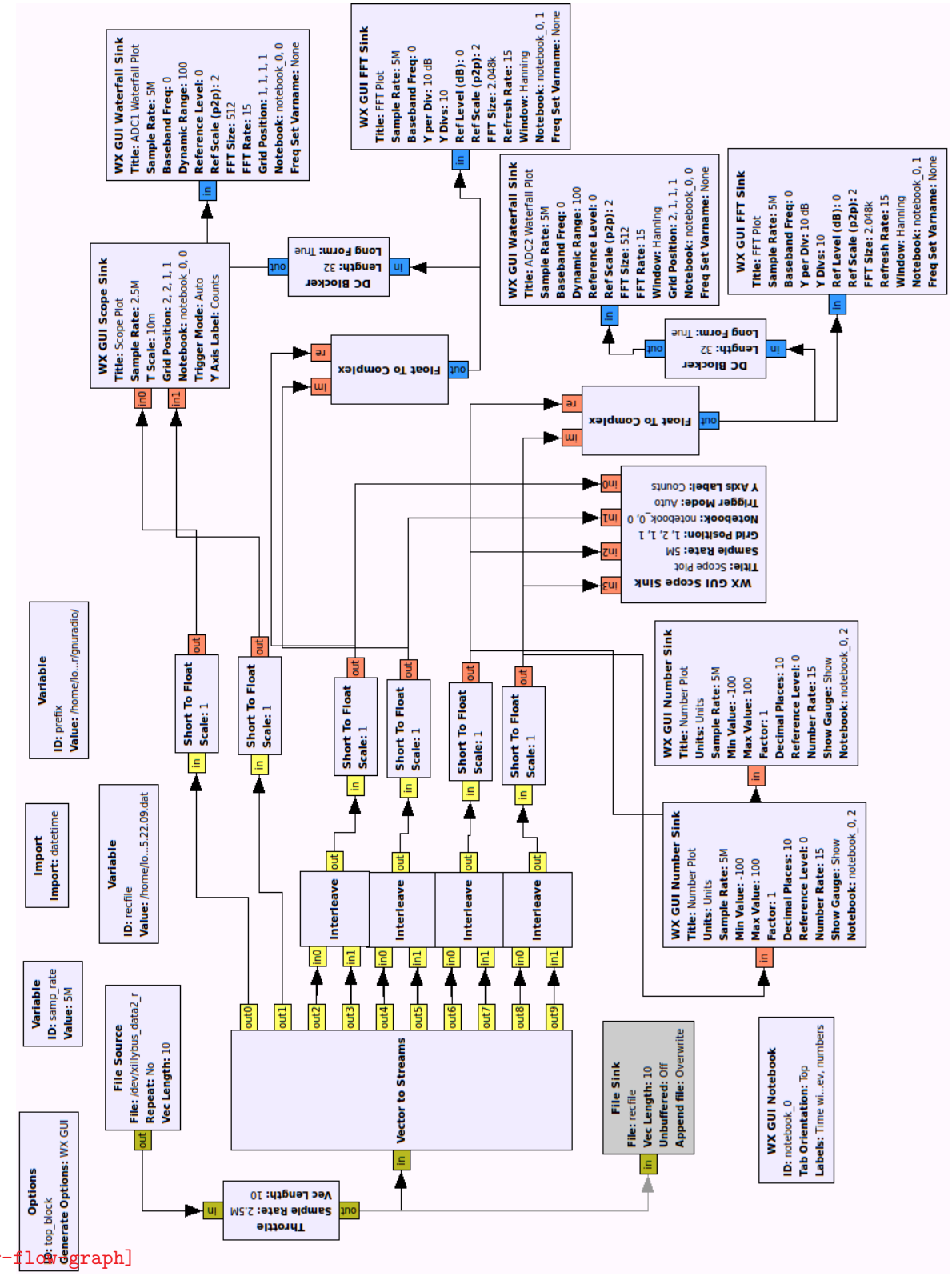
The interactive grabber-viewer user interface shows live oscilloscope-like time-value display for all data channels and live time-frequency scrolling display (a waterfall view) for displaying the frequency components of the grabbed signal. Signal is grabbed to file with exactly the same format, as it is described in table 2.6.

2.5 Achieved parameters

Trial design construction was tested for proper handling of sampling rates in range of 5 MSPS to 15 MSPS it should work above this limit. System works on i7 8 cores computer with Ubuntu 12.04 LTS operating system. Data recording of input signal is impossible above sampling rates around 7 MSPS due to bottleneck at HDD speed limits, it should be resolved by use of SSD disk drive. But it is not tested in our setup.

2.5.1 ADC module parameters

Two prototypes of ADC modules were assembled and tested. The first prototype, labeled ADC1, has LTC2190 ADC chip populated with LT6600-5 front-end operational



[grabber-flowgraph]

Figure 2.7. The ADC recorder flow graph created in gnuradio-companion.

amplifier. It also has a 1kOhm resistors populated on inputs which give it an ability of an internal attenuation of the input signal. The value of this attenuation A is described by the following formula (1)

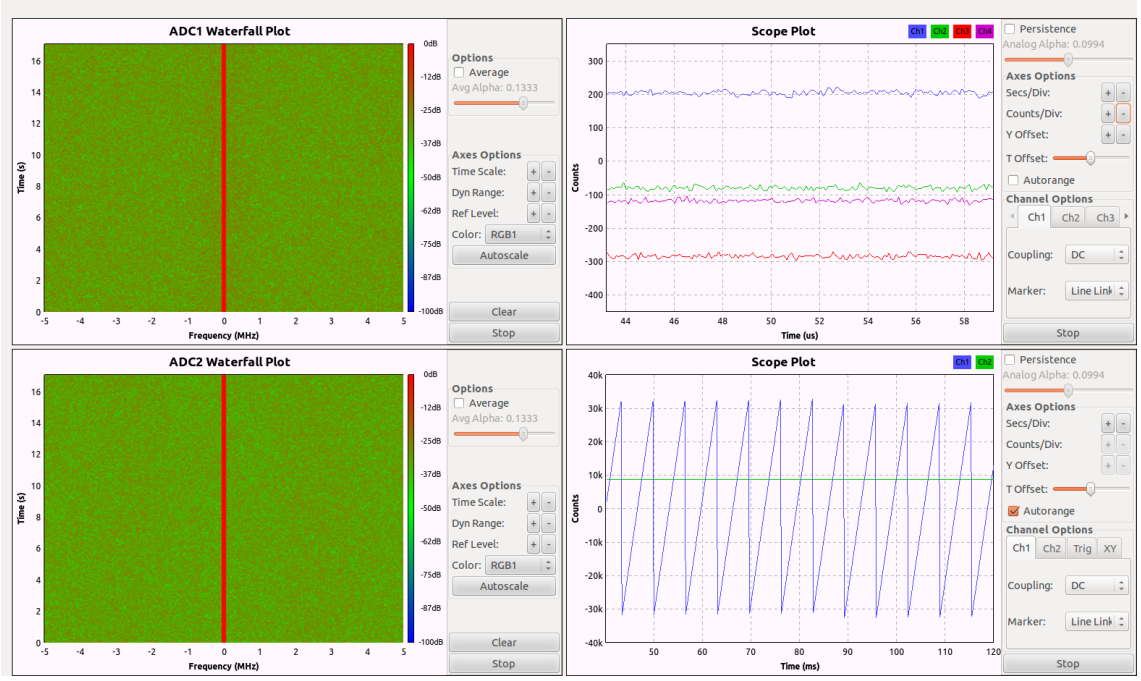


Figure 2.8. User interface window of a running ADC grabber.

[ADC1-gain]

$$A = \frac{806 \cdot R_1}{R_1 + R_2} \tag{1}$$

Where the letters stand for:

- A - Gain of an input amplifier.
- R_1 - Output impedance of signal source (usually 50 Ohm).
- R_2 - Value of serial resistors at operational amplifier inputs.

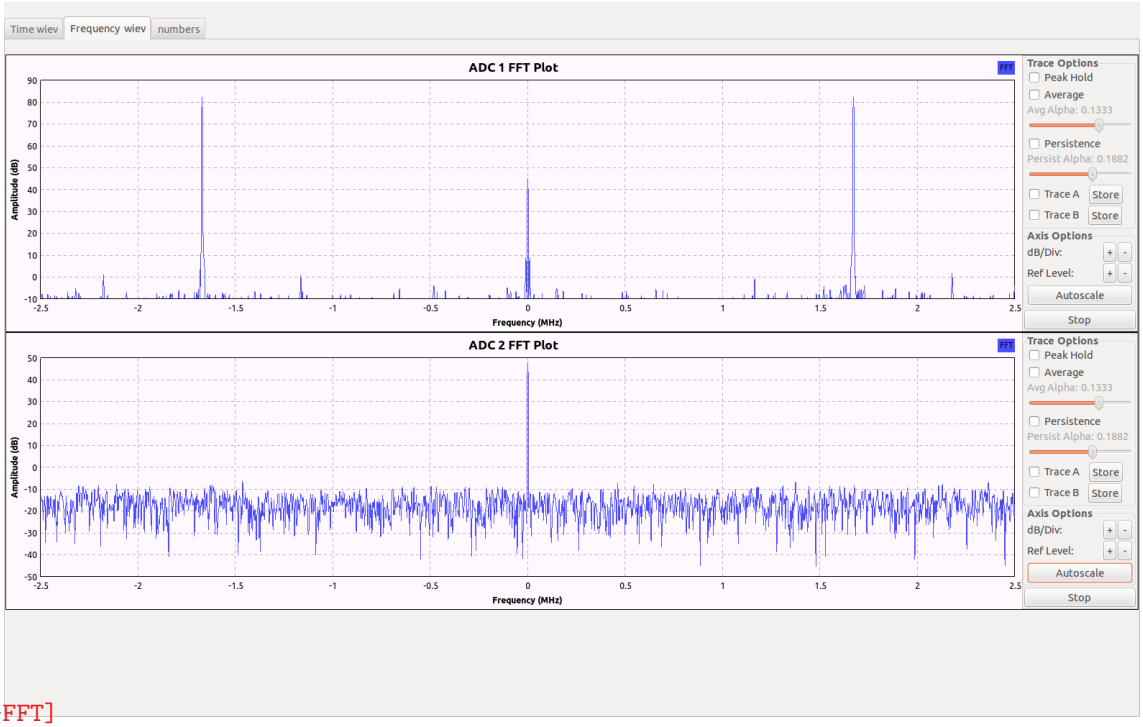
We have $R_2 = 1000\Omega$ and $R_1 = 50\Omega$ which imply that $A = 0.815$. That value of A is further confirmed by the measurement. In our measurement setup we have H1012 Ethernet transformer connected to inputs of ADC. We have used this transformer for signal symetrization from BNC connector at Agilent 33220A signal generator. Circuit diagram of used transformer circuit is shown in picture and circuit realization in photograph 2.11.

Used signal generator Agilent 33220A has not optimal parameters for this type of dynamic range measurement. Signal distortion and spurious levels are only -70 dBc according to Agilent datasheet [17]. Although, we measured ADC saturation voltage of 705.7 mV (generator output) in this setup due to impedance mismatch and uncalibrated measurement setup and 1V ADC range selected by sense pin. This is relatively high error, but main result from this measurement is FFT plot shown in image 2.9, which confirms >80 dB dynamic range at ADC module input.

Similar test we performed at ADC2 module. For ADC2 we have to use formula with a different constant (1). The ADC2 module has LT6600-2.5 amplifiers populated on it with gain equal to $A = 2.457$ and uses the same R_2 resistors. We measured saturation voltage of 380 mV (generator output) at channel 1 on this ADC. It is well in parameter tolerances of used setup.

[ADC2-gain]

$$A = \frac{1580 \cdot R_1}{R_1 + R_2} \tag{2}$$

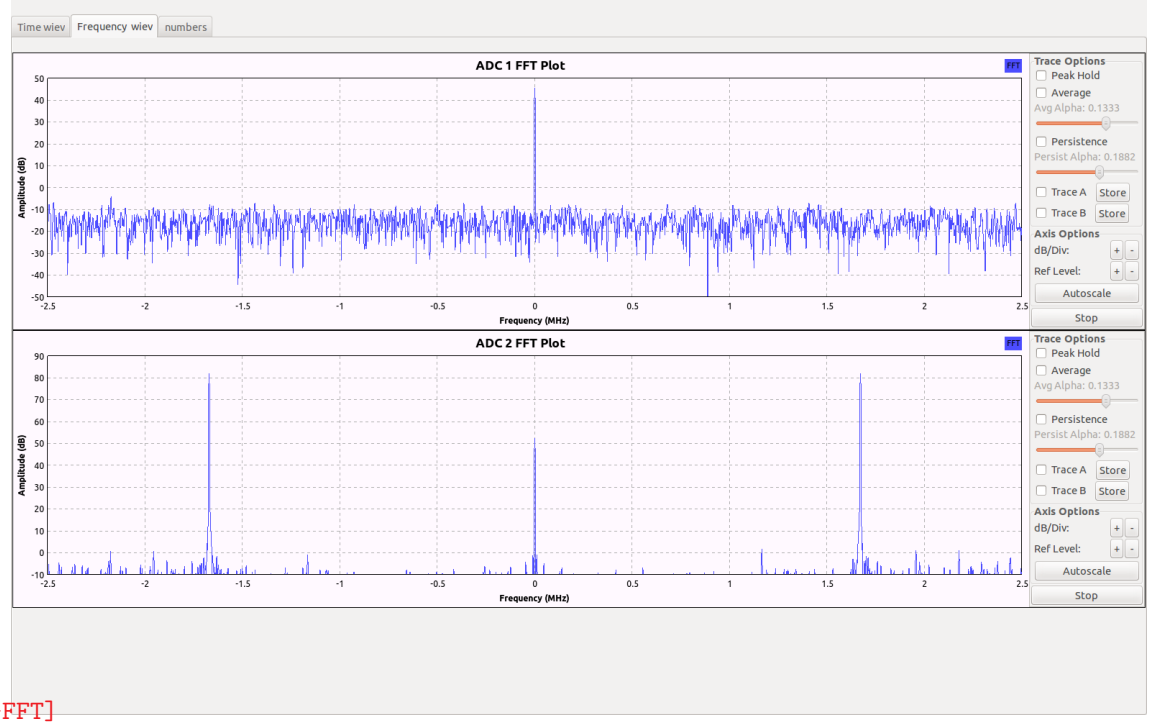


[ADC1-FFT]

Figure 2.9. Sine signal sampled by ADC1 module with LTC2190 and LT6600-5 devices.

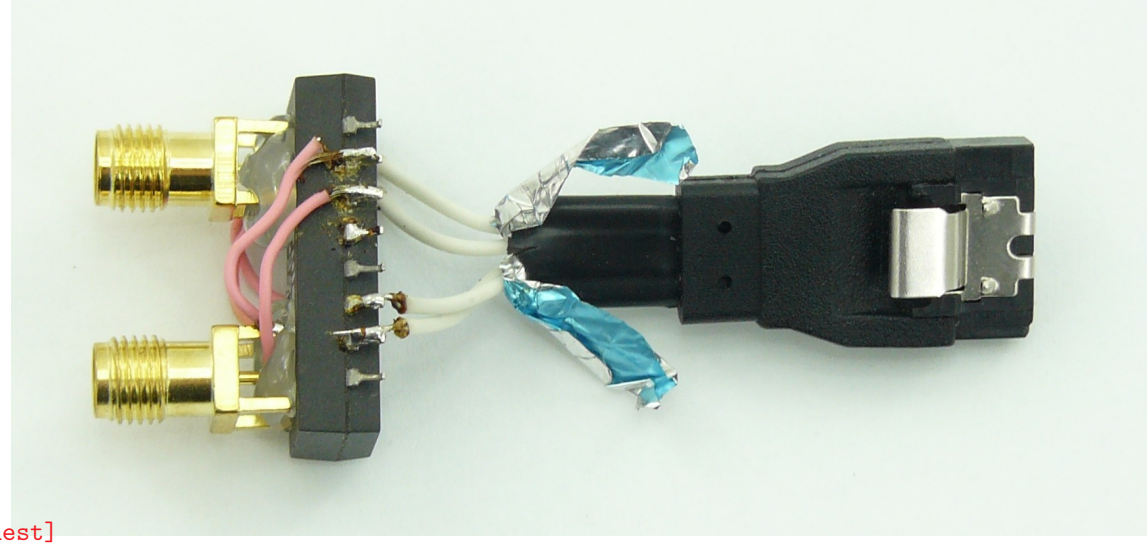
Where the letters stand for:

- A - Gain of an input amplifier.
- R_1 - Output impedance of signal source (usually 50 Ohm).
- R_2 - Value of serial resistors at operational amplifier inputs.



[ADC2-FFT]

Figure 2.10. Sine signal sampled by ADC2 module with LTC2271 and LT6600-2.5 devices.



[SMA2SATA-nest]

Figure 2.11. Balun transformer circuit used for ADC parameters measurement. It is constructed from H1012 transformer salvaged from an old Ethernet card.

Computed FFT spectra for measured signal are shown in the images 2.10 and 2.9. Both images confirm that ADCdual01A modules have input dynamical range of 80 dB at least.

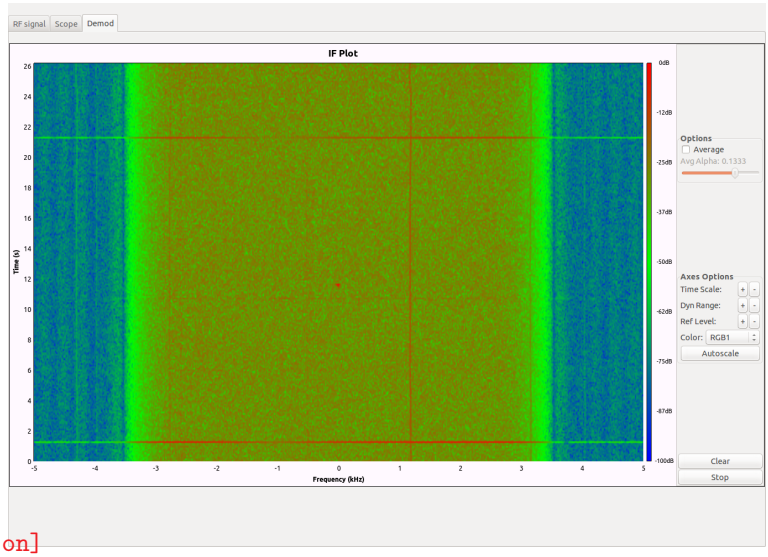
Chapter 3
Example of usage

For additional validation of system characteristics a receiver setup has been constructed.

3.1 Basic interferometric station

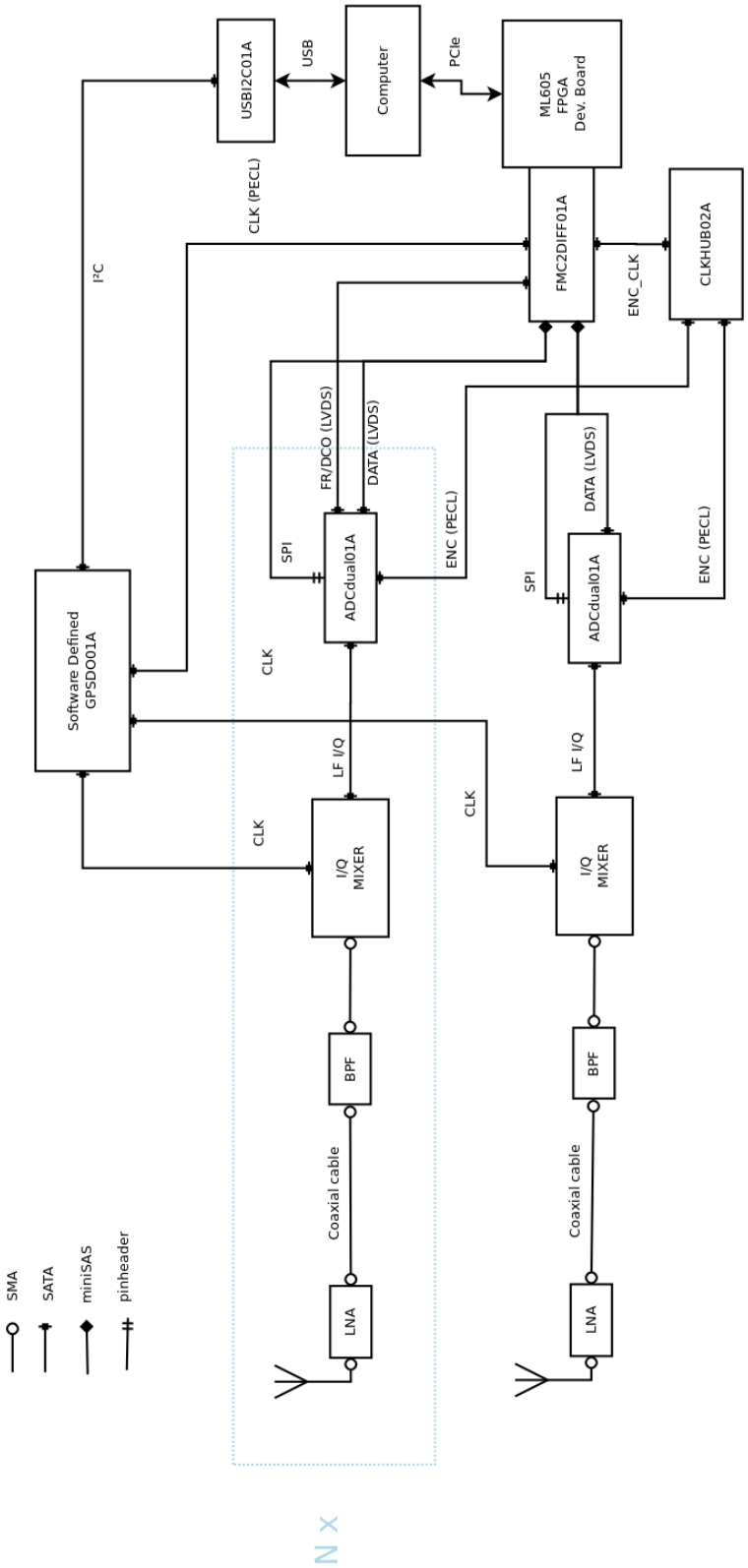
Interferometry station was chosen to serve as the most basic experimental setup. We connected the new data acquisition system to two SDRX01B receivers. Block schematics of the setup used is shown in image 3.1. Two ground-plane antennae were used and mounted outside the balcony at CTU building at location 50° 4' 36.102" N, 14° 25' 4.170" E. Antennae were equipped by LNA01A amplifiers. All coaxial cables have the same length of 5 meters. Antennae were isolated by common mode ferrite bead mounted on cable to minimise the signal coupling between antennas. Evaluation system consists of SDGPSDO local oscillator subsystem used to tune the local oscillator frequency.

Despite of schematic diagram proposed on beginning of system description.... We used two separate oscillators – one oscillator drives encode signal to ADCs still through FPGA based divider and other one drives SDRX01B mixer. Reason for this modification is simplification of frequency tuning during experiment. It is because single oscillator may be used only with proper setting of FPGA divider, this divider may be modified only by recompilation of FPGA code and loading/flashing new FPGA schema. Due to fact that FPGA was connected to PCI express and kernel drivers and hardware must be reinitialized, reboot of PC is required. Instead of this procedure, we set the FPGA divider to constant division of factor 30 and used another district oscillator for ADCdual01 sampling modules and for SDRX01B receiver. We use ACOUNT02A MLAB instrument for frequency checking of correct setup on both local oscillators.



[meteor-reflection]

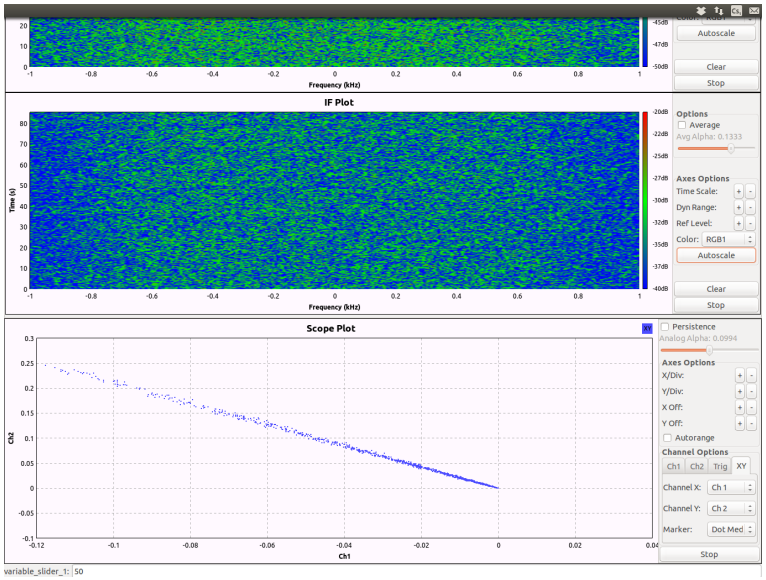
Figure 3.2. Meteor reflection received by evaluation setup.



[block-schematic]

Figure 3.1. Complete receiver block schematic of dual antenna interferometric station.

For simplest demonstration of phase difference between antennas, we analyse part of signal by complex conjugate multiplication between channels. Result of this analysis



[phase-difference]

Figure 3.3. Demonstration of phase difference between antennas.

can be seen on picture 3.3. Points of selected part of signal creates clear vector, which illustrates the presence of phase difference.

Chapter 4
Proposed final system

Construction of a final system which is supposed to be employed for real radioastronomy observations will be described. This chapter is mainly a theoretical analysis of data handling systems. Realization of these ideas might be possible as a part of our future development after we fully evaluate and test the current trial design.

The system requires proper handling of huge amounts of data and either huge and fast storage capacity is needed for store captured signal data, or enormous computational power is required for online data processing and filtering. Several hardware approach currently exist and are in use for data processing problem handling. Either powerful multi gigahertz CPUs, GPUs, FPGAs, or specially constructed ASICs are used for this task.

4.1 Custom design of FPGA board

In the beginning of the project, a custom design of FPGA interface board had been considered. This FPGA board should include PCI express interface and should sell at lower price than trial design. It should be compatible with MLAB internal standards which is further backward compatible with the existing or improved design of ADC modules. For a connection of FPGA board to another adapter board with PCIe we expect a use of a PCIe host interface. Thunderbolt technology standard was expected to be used in this PC to PCIe module which further communicate with MLAB compatible FPGA module. Thunderbolt chips are currently available on the market for reasonable prices [18]. However, a problem lies in the accessibility to their specifications, as specification is only available for licensed users and Intel has a mass market oriented licensing policy, that makes this technology inaccessible for low quantity production. As a consequence, an external PCI Express cabling and expansion slots should be considered as a better solution, if we need preserve standard PC as main computational platform.

However, these PCI express external systems and cables are still very expensive. Take Opal Kelly XEM6110 [19] as an example, with its price tag reaching 995 USD at time of writing of thesis. Therefore, a better solution probably needs to be found.

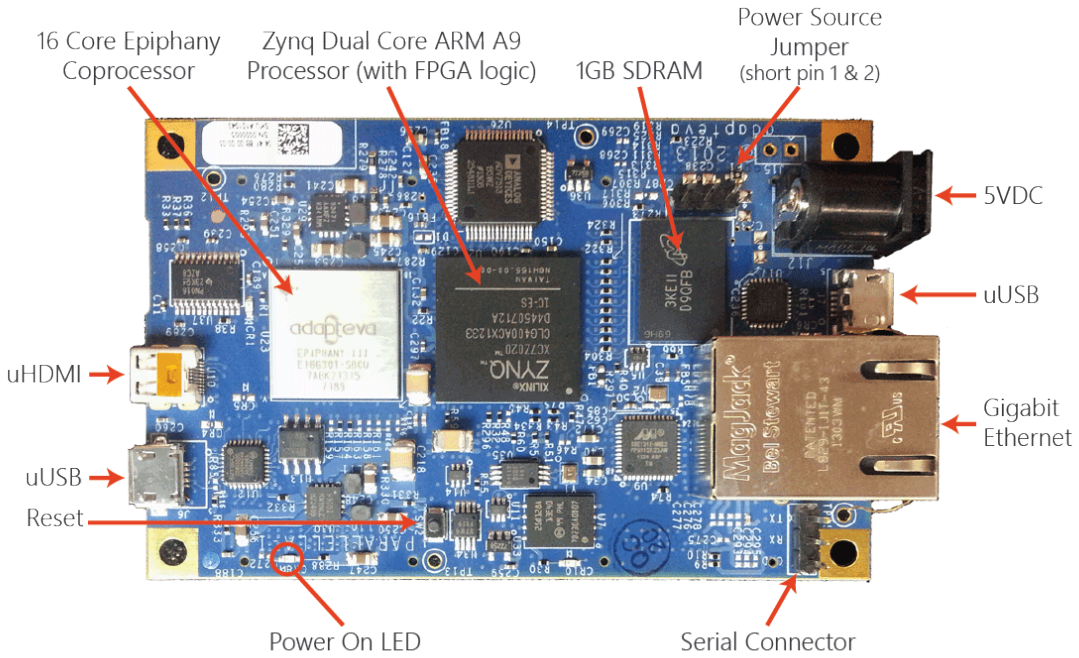
An interfacing problem will by probably resolved by other than Intel ix86 architecture. Many ARM computers have risen on market due to increased demand of embedded technologies, which requires high computation capacity, low power consumption and small size – especially smart phones. Many of those ARM based systems has interesting parameters for signal processing. This facts makes Intel's ix86 architecture unattractive for future project.

4.2 Parralella board computer

Parallella is new product from Adapteva, Inc. [20], this small supercomputer have been in development almost two years and only testing series of boards have been produced

until now (first single-board computers with 16-core Epiphany chip were shipped December 2013) [20]. This board have near ideal parameters for signal processing (provides around 50 GFLOPS of computational power). The board is equipped by Epiphany coprocessor which has 16 High Performance RISC CPU Cores, Zynq-7020 FPGA with Dual ARM® Cortex™-A9 MPCore™ and 866 MHz operating frequency, 1GB RAM, 85K Logic Cells, 10/100/1000 Ethernet and OpenCL support [21]. In addition of that this board consume only 3 Watts of power if both Zynq and Epiphany cores are running.

Main disadvantage of Parralella board is is unknown lead time and absence of SATA interface or other interface for data storage connection. Fast data storage interface would be useful and allows bulk processing of captured data. Then a result from data processing will be sent over the Ethernet interface to data storage server.



[img-parallella-board]

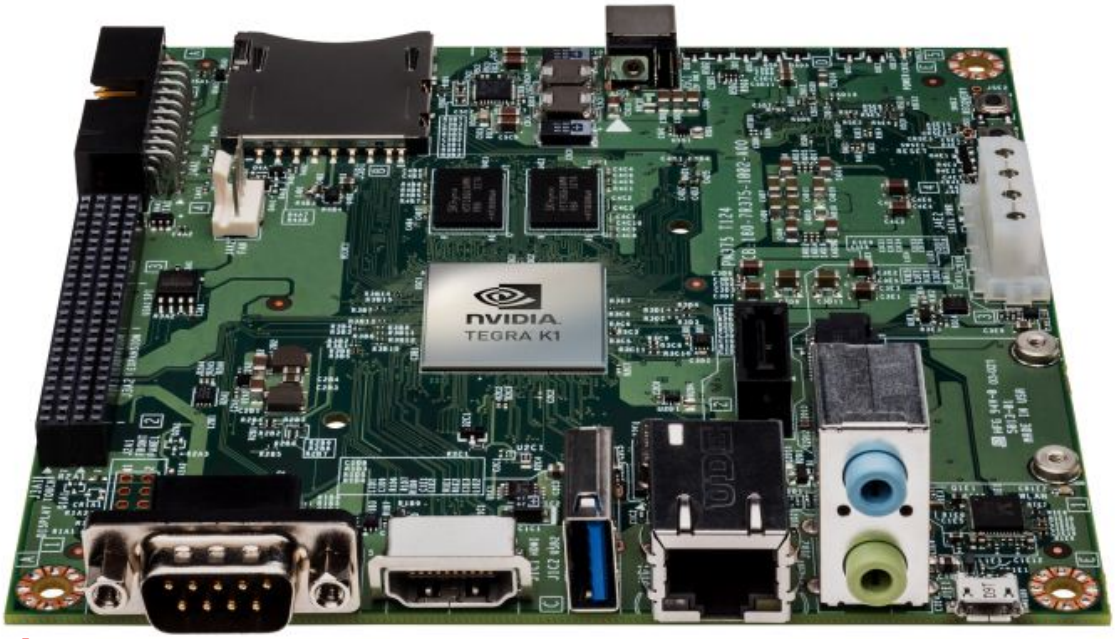
Figure 4.1. Top view on Parallella-16 board [21].

If Parallella board will be used as radioastronomy data interface a new ADC interface module should be designed. Interfacing module will use four PEC connectors mounted on bottom of Parallella board. This doughter module should have MLAB compatible design and preferably constructed as separable modules for every Parallella's PEC connectors.

4.3 GPU based computational system

A new GPU development board NVIDIA K1, shown in the following picture 4.2, has recently been released. These boards are intended to be used in fields including computer vision, robotics, medicine, security or automotive industry. They have good parameters for signal processing for a relatively low price of 192 USD. Unfortunately, they are currently only in pre-order release stage (in April 2014).

NVIDIA board is discrict by presence of PCI Experess connector. This connector should be used for FPGA connection, if we decide to use this development board in our



[img-NVIDIA-K1]

Figure 4.2. The NVIDIA Jetson TK1 Development Kit `https://developer.nvidia.com/jetson-tk1`.

radio astronomy digitalisation system. A new FPGA board with PCI Express direct PCB connector

4.4 Other ARM based computation systems

Other embeded ARM based computers for example ODROID-XU, lack of suitable high speed interface. Theirs highest speed interface is USB 3.0 which has currently unsettled development support and needs commercial software tools for evaluation and testing.

From summary analysis mentioned above the Parrallella board should be the best candidate for computational board in radioastronomy data aquisition system. Parralella board is optimised for high data flow processing. Parallella has not much memory to cache processing data but instead of this it has wide bandwidth data channels. Other boards provides much more computational power – 300 GFLOPS in case of NVIDIA K1, but these boards are optimised for computational heavy tasks on limited amount of data. This is typical problem in computer graphics. But in our application we do not need such extreme computation power at data aquisition system level. As result we should wait until Parallella becomes widely available. Then new ADCdual interfacing board should be designed ad prepared for use in new scalable radio astronomy data aquisition system. In meen time before suitable computing hardware become accessible. Required applications and algorithms should be optimised on proposed trial design with FPGA development board on standard PC host computer with PCI Express interface to development board.

Chapter 5
Conclusion

Special design of scalable data-aquisition system was proposed. This system has parameters

The final design will eventually become a part of MLAB Advanced Radio Astronomy System.

5.1 Possible hardware improvements

PCB design of used modules might need more precise high speed optimization of differential pairs. Improvement in high-speed routing allows possible use of fastest ADC from Linear Technology devices family. Use of faster ADCs even improve range of possible usage.

5.1.1 ADC modules weakness

Several ADC module imperfections, such as useless separation of FRAME and DCO signal to two connectors, should be mitigated. And this two signals should be merged to one SATA connector. This modification removes one redundant SATA cable between analog to digital converter nest and between computational unit nest.

5.2 Possible software improvements

In future versions of device, the Xillybus IP core and interface should be swapped with an open-source alternative PCIe interfacing module or PCIe may be completely avoided.

SPI configuration data read back should be implemented.

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Appendix A
Thesis specification

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

Fakulta elektrotechnická
Katedra měření

Akademický rok **2013-2014**

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student:	**Bc. Jakub Kákona**
Studijní program:	**Kybernetika a robotika**
Obor:	**Letecké a kosmické systémy**
Název tématu česky:	**Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač**
Název tématu anglicky:	**Fast multi-channel data acquisition system for radio-astronomy receiver**

Pokyny pro vypracování:

Proveďte rešerši a analyzujte stávající řešení vhodná pro danou aplikaci.

Navrhněte A/D modul pro digitalizaci radioastronomických dat založených na příjmu odražených pozemních signálů, ke konstrukci použijte dostupné ADC obvody. Jako datový koncentrátor pro přenos dat do PC využijte FPGA. Navrhněte připojení ADC modulů k FPGA a specifikujte požadavky na funkcionalitu implementovanou v FPGA. Výsledný VHDL design bude poskytnut.

Parametry: vzorkovací frekvence 1 MHz, možnost připojení 1 až 8 přijímačů (každý dva analogové kanály), rozlišení alespoň 12 bitů.

Návrh koncipujte škálovatelný, HW nechť sestává ze společné části a částí pro každý přijímač. Zkonstruujte funkční vzor zařízení. Využijte vývojovou desku ML605 s FPGA Virtex 6.

Převodník otestujte alespoň s jedním přijímačem a demonstrujte záznam dat a jejich zpracování.

Na základě otestování prototypu navrhněte (bez realizace) vlastní desku s FPGA a podpůrnými moduly.

Seznam odborné literatury:

[1] Vedral, J., Fischer, J.: Elektronické obvody pro měřicí techniku. Vydavatelství ČVUT, Praha 2004, ISBN 80-01-02966-2

[2] Richards, M.A., Scheer, J. A., Holm, W. A.: Principles of modern radar. Sci Tech Publishing, 2010, ISBN 978-1891121-52-4

Vedoucí diplomové práce:	Ing. Martin Matoušek, Ph.D. (K13133)
Datum zadání diplomové práce:	14. ledna 2014
Platnost zadání do[1]:	31. srpna 2015

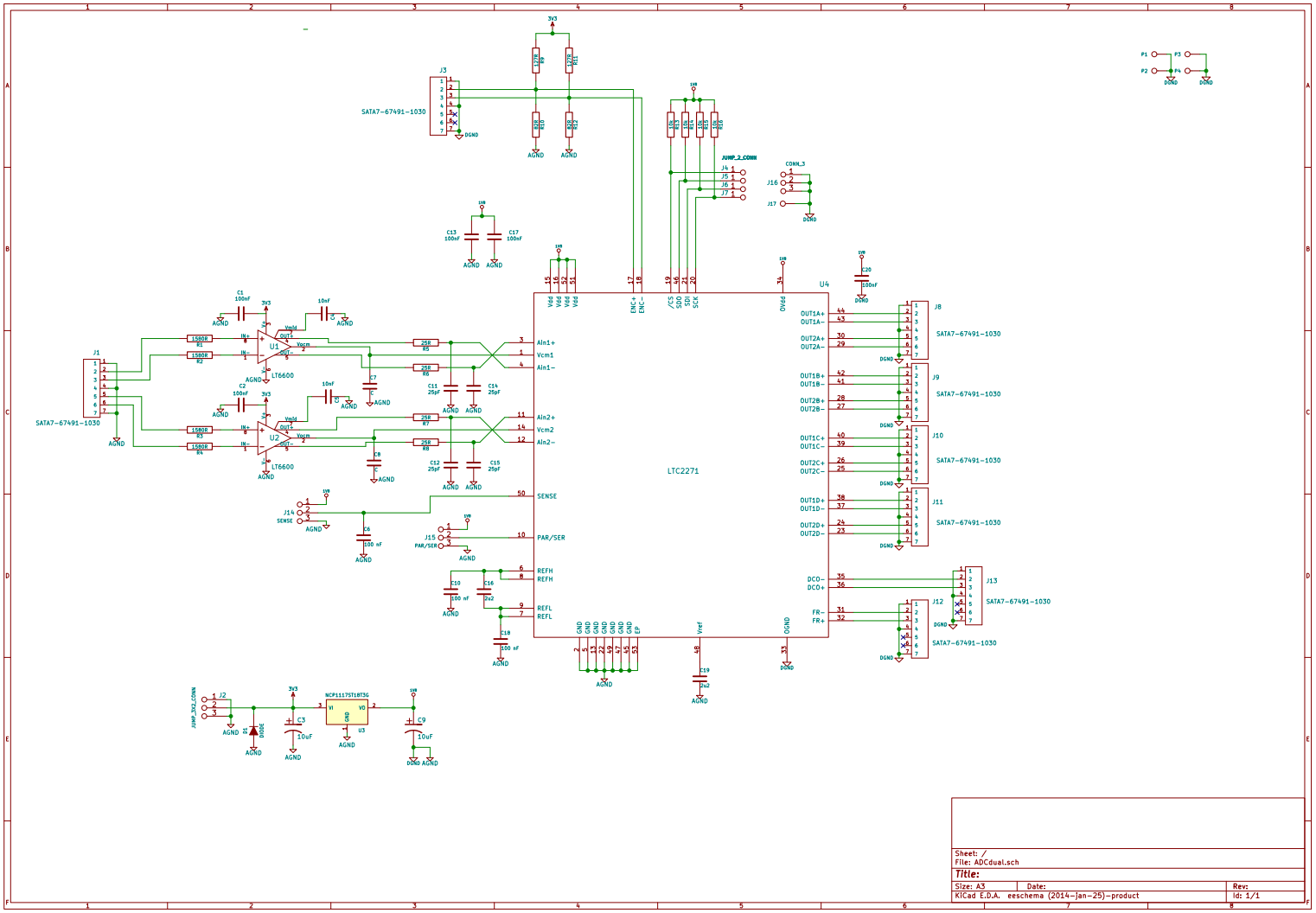
Prof. Ing. Vladimír Haasz, CSc.
vedoucí katedry

Prof. Ing. Pavel Ripka, CSc.
děkan

V Praze dne 14. 1. 2014

[1] Platnost zadání je omezena na dobu tří následujících semestrů.

Appendix B
Circuit diagram of ADCdual01A module



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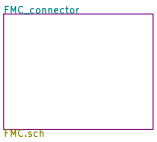
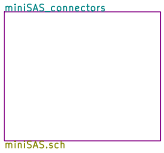
Appendix C
Circuit diagram of FMC2DIFF module





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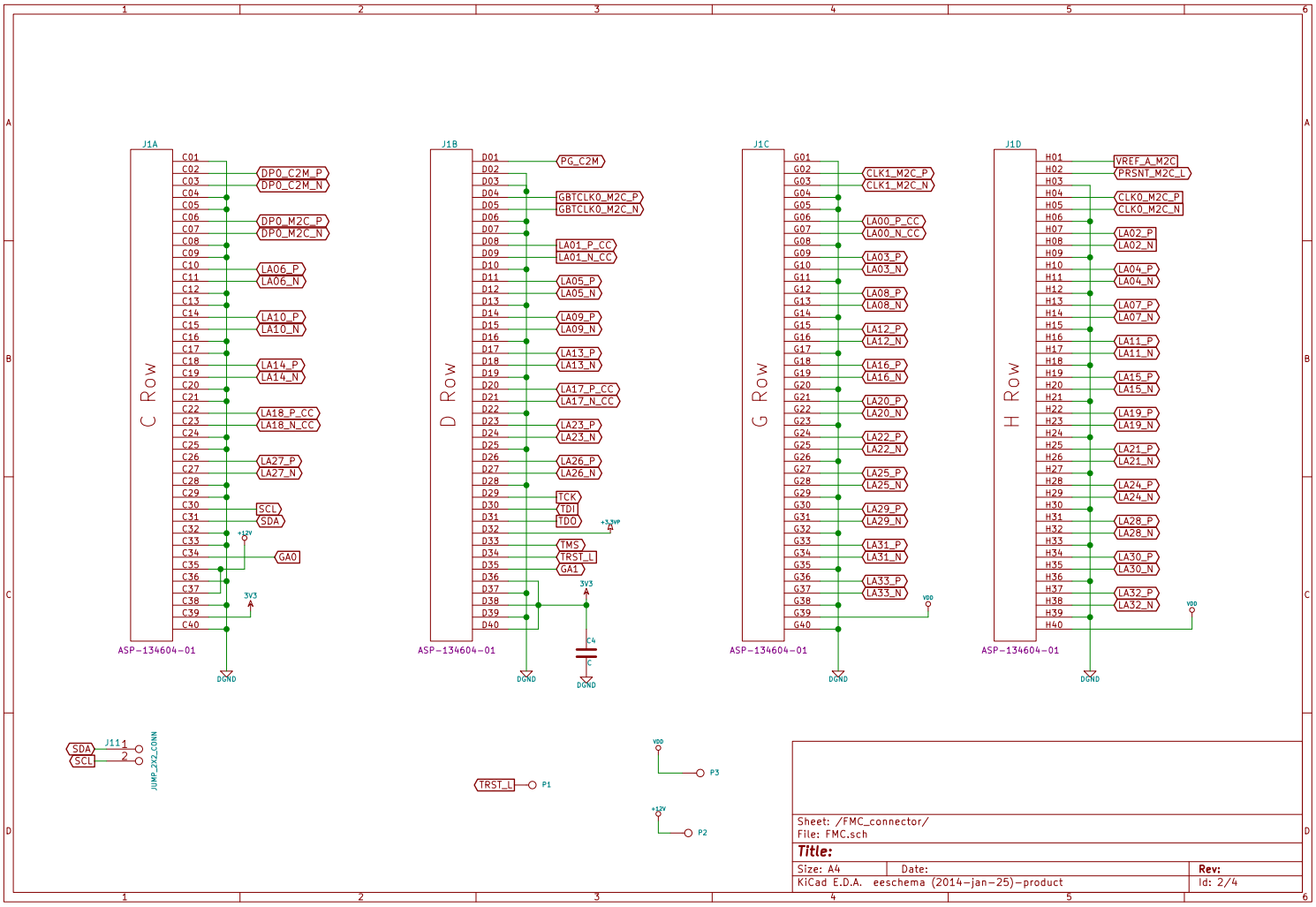
J1A
C Row
C01 C02 C03 C04 C05 C06 C07 C08 C09 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40
DP0_C2M_P
DP0_C2M_N
DP0_M2C_P
DP0_M2C_N
LA06_P
LA06_N
LA10_P
LA10_N
LA14_P
LA14_N
LA18_P_CC
LA18_N_CC
LA27_P
LA27_N
SCL
SDA
GA0
+12V
3V3
DGND
ASP-134604-01
J1B
D Row
D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 D36 D37 D38 D39 D40
PG_C2M
GBTCLK0_M2C_P
GBTCLK0_M2C_N
LA01_P_CC
LA01_N_CC
LA05_P
LA05_N
LA09_P
LA09_N
LA13_P
LA13_N
LA17_P_CC
LA17_N_CC
LA23_P
LA23_N
LA26_P
LA26_N
TCK
TDI
TDO
+3.3VP
TMS
TRST_L
GA1
3V3
C4
C
DGND
ASP-134604-01
J1C
G Row
G01 G02 G03 G04 G05 G06 G07 G08 G09 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 G25 G26 G27 G28 G29 G30 G31 G32 G33 G34 G35 G36 G37 G38 G39 G40
CLK1_M2C_P
CLK1_M2C_N
LA00_P_CC
LA00_N_CC
LA03_P
LA03_N
LA08_P
LA08_N
LA12_P
LA12_N
LA16_P
LA16_N
LA20_P
LA20_N
LA22_P
LA22_N
LA25_P
LA25_N
LA29_P
LA29_N
LA31_P
LA31_N
LA33_P
LA33_N
VDD
DGND
ASP-134604-01
J1D
H Row
H01 H02 H03 H04 H05 H06 H07 H08 H09 H10 H11 H12 H13 H14 H15 H16 H17 H18 H19 H20 H21 H22 H23 H24 H25 H26 H27 H28 H29 H30 H31 H32 H33 H34 H35 H36 H37 H38 H39 H40
VREF_A_M2C
PRSNT_M2C_L
CLK0_M2C_P
CLK0_M2C_N
LA02_P
LA02_N
LA04_P
LA04_N
LA07_P
LA07_N
LA11_P
LA11_N
LA15_P
LA15_N
LA19_P
LA19_N
LA21_P
LA21_N
LA24_P
LA24_N
LA28_P
LA28_N
LA30_P
LA30_N
LA32_P
LA32_N
VDD
DGND
ASP-134604-01
SDA
SCL
J11
1
2
JUMP_2X2_CONN
TRST_L
P1
VDD
P3
+12V
P2
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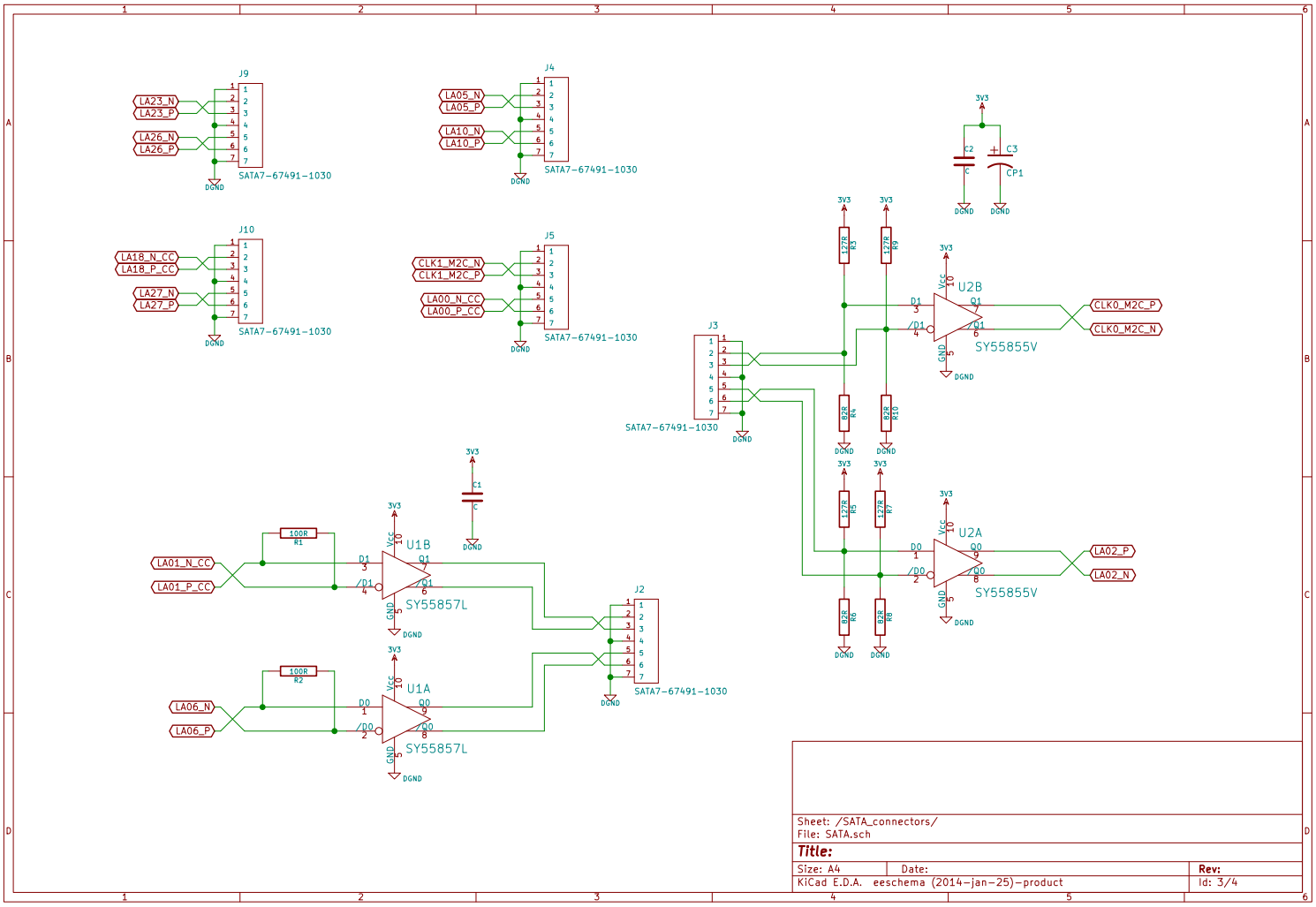

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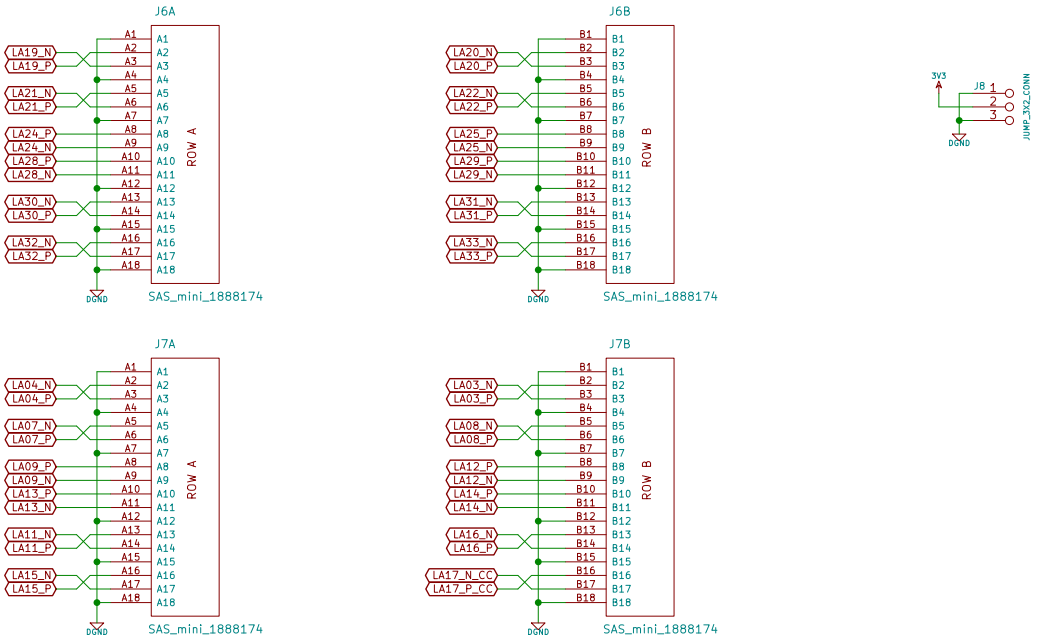

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Appendix D
Content of enclosed CD