

Master's thesis



Czech  
Technical  
University  
in Prague

**F3**

Faculty of Electrical Engineering  
Department of Measurement

# Fast multi-channel data acquisition system for radio-astronomy receiver

**Jakub Kákona**  
Aircraft and Space Systems

June 2014

<http://petr.olsak.net/ctustyle.html>

Supervisor: Ing. Martin Matoušek, Ph.D.

Draft: 3. 5. 2014



## Acknowledgement / Declaration

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.

V Praze dne 12. 5. 2014

.....

## Abstrakt / Abstract

**Klíčová slova:**

**Překlad titulu:** Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač

**Keywords:**

# / Contents

<b>1 Introduction</b> .....	1
1.1 Current radioastronomy problems.....	1
1.2 Modern Radio astronomy receiver .....	2
1.2.1 Observation types.....	3
1.3 Required receiver parameters ...	3
1.3.1 Sensitivity and noise number .....	3
1.3.2 Dynamic range.....	3
1.3.3 Bandwidth .....	3
<b>2 Trial design</b> .....	4
2.1 Required parameters.....	4
2.2 Sampling frequency .....	4
2.3 System scalability.....	4
2.3.1 Differential signalling .....	5
2.3.2 Phase matching .....	5
2.4 System description .....	5
2.4.1 Frequency synthesis.....	5
2.4.2 Signal cable connectors ....	6
2.4.3 Signal integrity re- quirements .....	6
2.4.4 Design of ADC modules ...	6
2.4.5 ADC selection.....	7
2.4.6 ADC modules interface ....	8
2.4.7 Output data format .....	8
2.5 Achieved parameters.....	9
2.5.1 Data reading and recording .....	9
2.5.2 ADC module parameters ..	9
<b>3 Proposed final system</b> .....	12
3.1 Custom design of FPGA board .....	12
3.2 Prralella board computer.....	12
3.3 GPU based computational system .....	12
<b>A Circuit diagram of ADCdu- al01A module</b> .....	15
<b>B Circuit diagram of FMC2DIFF   module</b> .....	16

## Tables / Figures

<b>2.1.</b> Available ADC types.....7	<b>2.1.</b> Used miniSAS cable.....6
	<b>3.1.</b> NVIDIA Jetson TK1 Development Kit ..... 13

# Chapter 1

## Introduction

### 1.1 Current radioastronomy problems

Nejprve z pohledu radioastronoma je podstatné, že jej v převážné většině zajímají signály přírodního charakteru, přicházející z okolního vesmíru. Tedy většinou ani nechce, aby měly nějakou spojitost s naší civilizací.

From radioastronomer point of view its important radioastronomy has interest in natural signals from surrounding universe. Radio astronomy do not have interest in terrestrial civilisation made signals.

To je často velký problém, neboť na Zemi touto dobou existuje velké množství vysílačů, které pokrývají prakticky celé dostupné elektromagnetické spektrum a vytvářejí tak nepřehlednou směs signálů, která se nejenom pro radioastronoma může stát nepřekonatelným problémem. Z tohoto důvodu byla již od počátků rádiového vysílání snaha udržet nad obsazením spektra určitou kontrolu a jedním z důsledků této snahy je například ja href=[http://www.ukaranet.org.uk/basics/frequency\\_allocation.htm](http://www.ukaranet.org.uk/basics/frequency_allocation.htm) tabulka přidělených kmitočtů pro radioastronomii; a. Bohužel z mnoha důvodů nelze říci, že by tyto kmitočty byly dostatečně kvalitně čisté pro seriózní pozorování. Z toho vyplývá důležité zjištění, že v současné době nelze postupovat stejně jako v počátcích radioastronomie. A tedy i experimenty, vedoucí například k objevu reliktního záření nebo pulzarů, nelze v původní podobě zopakovat s uspokojivým výsledkem.

This is big problem because at this moment many terrestrial transmitters are active and all this transceivers made desnsse signal mictrure which can cause troubles not only to radioastronomers. In consequence of this, there exist a tendence to control radiofrequency spectrum. As result of this controlling the radiofrequency allocation table was created [http://www.ukaranet.org.uk/basics/frequency\\_allocation.htm](http://www.ukaranet.org.uk/basics/frequency_allocation.htm) This table consist special bands allocated to radioastronomy use. But from many ... this bands are not clean enough for directly use in radioastronomy observations. As resul of this we cannot work by same way as radioastronomers in beginnig of radioastronomy. Many experiments namely, reliktive radiation detection and pulsar detection cant be realised in original form with satisfactive results.

Důkazem může být například projekt RadioJOVE, který přes svojí správnou ideu v dnešním civilizovaném světě jednoduše nefunguje. Důvodem jeho nefunkčnosti je právě přítomnost elektromagnetického smogu, který je řádově silnější, než Jupiter. A z praxe například i okolo světelného znečištění nelze očekávat nějakou radikální změnu k lepšímu.

This RadioJOVE project has good idea in creating publicly available cheap radioastronomy receiver. But in old fashioned construction which can work in centers of desert. But it simply cant work in modern civilisation as it is know in Europe. Origin of its disfuncion is presence of strong radiofrequency interferences. This interferences are orders of magnitude stronger than Jupiter decametric emmissions. From praqtice about light pollution we also know that there aro not much chance to improve this situation radically.

Nezbývá proto než hledat metody, jak se při radioastronomickém pozorování obejít bez úplně čistých pásem a prohlédnout skrze směs terestrického elektromagnetického rušení. Jednou z možností je využít zatím známých vlastností přírodních signálů, a to jejich relativně velké spektrální širokopásmovosti a zároveň velmi velkého plošného pokrytí vzhledem k pozemským vysílačům, protože pro přírodní objekty není problém vyzařovat v šířce pásma desítek MHz a přitom pokrýt plochu poloviny zeměkoule. Je ale ovšem jasné, že tyto parametry jsou na úkor dopadajícího výkonu a ten je tedy řádově miliardkrát menší, než výkon přijímaný z rozhlasového vysílače.

There are not other ways that searching for new methods in radioastronomy observations. New methods which allows us to work without completely clear radiofrequency bands and allow us to see surrounding universe through man made radiofrequency interference mixture. One of solutions is use of already known natural signals parameters. Natural signals usually have different signal properties from local interference. Natural objects do not have a problem with transmission bandwidth of tens megahertz in sub 100 MHz bands. This object also transmit the same signal for almost half of Earth without any difficulties. But it is also clear that signal parameters have drawbacks in reception power. The reception power of radioastronomy object is  $10^9$  smaller than signal power received from typical broadband radio transmitter.

Z těchto faktů je jasné, že nynější požadavky na radioastronomický přijímač jsou odlišné od těch v minulosti. Zejména jde o šířku přijímaného pásma. Tento parametr dříve dosahoval řádově jednotek až desítek kHz, což stačilo, neboť velká část pozorování se zpracovávala buď poslechem, a nebo pomocí zapisovače, který integroval signál přes definovanou oblast, a tím bylo možné zaznamenávat intenzitu a změny v přírodním kontinuu. Tou dobou ale neexistovaly žádné pozemské širokopásmové vysílače, snad kromě televizních, takže nebyl problém přijímač odladit do čisté oblasti. Dříve také nebylo nutné pozorovat paralelně z více míst planety, protože podmínky byly všude téměř totožné.

From this fact is clear one result. Modern requirements on

## 1.2 Modern Radio astronomy receiver

In beginning of radioastronomy receivers were constructed as simple station with single antenna or multi antenna array with fixed phasing. This approach were used due to limits of previous electronics. Main challenges were noise number and sensitivity due to poor characteristic of active electronic components such transistors and vacuum tubes.

Řešením je pravděpodobně použít přijímač, který bude mít velkou šířku pásma, nejlépe řádu MHz, a vysokou vstupní odolnost. A pokud možno půjde sfázovat s nějakým dalším na jiném místě planety. Existuje několik zařízení, které tyto požadavky splňují. V naprosté většině jde o takzvané [SDR](http://en.wikipedia.org/wiki/SDR) přijímače, jako například USRP, USRP2, SDR-IQ a SSRP. Tato zařízení ale mají většinou zásadní nevýhodu, že jejich pořizovací cena je více jak 1000 USD a jsou velmi univerzální. Takže se moc nehodí na nějaké kontinuální pozorování, kde nebudou využity všechny jejich drahé zaplacené vlastnosti. Poslední z uvedených je [SSRP](http://en.wikipedia.org/wiki/SSRP), je ale jednoduchá konstrukce 16bit AD převodníku připojeného k USB řadiči, který hrne všechna navzorkovaná data do PC. Je to velmi zajímavé zařízení s řádově nižší pořizovací cenou. Avšak v této podobě je omezené datovým tokem USB, které omezuje vzorkovací frekvenci na zhruba 30MSPS. Z čehož vyplývá, že v prvním Nyquistově pásmu není možné zpracovávat signály o frekvenci vyšší než 15MHz. To je pro radioastronomické účely poměrně nízko. Řešením by byl přechod do vyšších Nyquistových



zón, kde ale začne vznikat problém s vhodnou konštrukcií antialiasing filtru a omezením sample-hold obvodu na vstupe ADC.

Many of today radioastronomy equipments were constructed in this manner. They were constructed usually shortly after WWII or during The Cold War as parts of military technology. These systems are slowly modernised and complete new systems are constructed. ALMA, SKA..

This new radio astronomy receivers have completely different approach to solve the problem of radioastronomy signal reception. They almost exclusive uses multi antenna arrays and mathematical algorithms for signal handling. Radio signal recorded by this method can be used by many ways. Radio image can be computed (if sufficient cover of u/v plane is achieved), radiation intensity can be measured, spectrum can be analysed for velocity measurement. etc.

### ■ 1.2.1 Observation types

Today radioastronomy knows several observation types.

- Spectral observations
- Intensity observations
- Velocity observations

All of these observations ideally needs high frequency resolution and stability. Wide observation bandwidth in hundreds of MHz is usually desirable for easier discrimination of source types.

## ■ 1.3 Required receiver parameters

This new approach of receiver construction has different requirement on receiver parameters. No signal to noise ratio on single antenna is improved. But other parameters are requested at now.

### ■ 1.3.1 Sensitivity and noise number

These parameters are are tied together, but multi antenna and multi receiver arrays requires to keep price of receiver at minimal values. This implicates that sensitivity and noise number must be least as good to detect (signal /noise  $\geq 1$  ) observed object on majority of receivers connected to observation network.

### ■ 1.3.2 Dynamic range

Dynamic range is huge problem of current radioastronomy receivers. This parameter is enforced by anywhere present humans made EMI radiation on RF frequencies. The modern radio astronomy receiver must not be saturated by this high levels of signals.

### ■ 1.3.3 Bandwidth

From requirements mentioned above

The system requires proper handling of huge amount of data.

Professional radioastronomers uses uses proprietary digitalisation units <http://arxiv.org/abs/1305.3550> or by multichannel sound cadrd on amateur levels <http://fringes.org/>

# Chapter 2

## Trial design

The whole design of radioastronomy receiver digitalization unit is constructed to be used in a wide range of applications and tasks related to digitalisation of signal from radioastronomy receivers. A good illustrating problem for its use is a signal digitalisation from multiple antenna arrays. This design will eventually become a part of MLAB Advanced Radio Astronomy System.

### 2.1 Required parameters

Wide dynamical range and high 3 intercept points are desired. The receiver must accept wide dynamic signals because a typical radioastronomy signal has a form of a weak signal covered by a strong man-made noise signal.

- Dynamical range better than 80 dB
- Phase stability between channels
- Noise (all types)
- Sampling jitter better than 100 metres

### 2.2 Sampling frequency

Sampling frequency is limited by the technical constrains in the trial design. This parameter is especially limited by the sampling frequencies of analog-to-digital conversion chips available on the market. Combination of the required parameters – dynamic range which needs at least 16bit and a minimum sampling frequency of 1 MSPS, leads to high end ADC chips which does not support such low sampling frequencies at all. Their minimum sampling frequency is 5 MSPS.

### 2.3 System scalability

For analogue channels scalability, special parameters of ADC modules are required. Ideally, there should be a separate output for each I/Q channel in ADC module. ADC module must also have separate inputs for sampling and data output clocks. These parameters allow for conduction at relatively low digital data rates. Then the digital signal can be conducted even through long wires.

Clock signal will be handled distinctively in our scalable design. Selected ADC chip are guaranteed to have defined clock skew between sampling and data output clock. This allows taking data and frame clocks from the first ADC module only. The rest of the data and frame clocks from other ADC modules can be measured for diagnostic purposes. (Failure detection, jitter measurement etc.)

This system concept allows for scalability, that is technically limited by a number of differential signals on host side and its computational power. There is another advantage of scalable data acquisition system – economic one. Observatories or end users can

make a choice of how much money are they willing to spent on radioastronomy receiver system. This freedom of choice is especially useful for science sites without previous experience in radioastronomy observations.

### ■ 2.3.1 Differential signalling

The concept of scalable design requires relatively long circuit traces between ADC and digital unit which captures the data and performs the computations. The long distance between the digital processing unit and the analog-to-digital conversion unit has an advantage in noise retention typically produced by digital circuits. Those digital circuits, such as FPGA or other flip-flops block and circuit traces, usually work at high frequencies and emit wide-band noise with relatively low power. In such case any increase in a distance between the noise source and analog signal source increase S/N significantly. However, at the same time a long distance brings problems with the digital signal transmission between ADC and computational unit. This obstacle should be resolved more easily in free-space than on board routing. The high-quality differential signalling shielded cables should be used. This technology have two advantages over PCB signal routing. First, it can use twisted pair of wires for leak inductance suppression in signal path. Moreover, the twisted pair may additionally be shielded by uninterrupted metal foil.

### ■ 2.3.2 Phase matching

For multiple antenna radioastronomy projects, system phase stability is mandatory. It allows precise high resolution imaging of objects.

High phase stability in our scalable design is achieved by centralised frequency generation and distribution with multi-output LVPECL hubs, that have equiphased outputs for multiple devices.

This design ensures that all devices have access to defined phase and known frequency.

## ■ 2.4 System description

In this section testing system will be described.

### ■ 2.4.1 Frequency synthesis

We have used centralised topology as a basis for frequency synthesis. One precise high-frequency and low-jitter digital oscillator has been used while other working frequencies have been derived by its division. This central oscillator has a software defined GPS disciplined control loop for frequency stabilisation.<sup>1)</sup> Frequency monitoring compensation method has been used in order to meet modern requirements on radioastronomy equipment which needs precise frequency and phase stability on wide area for effective radioastronomy imaging.

Every ADC module will be directly connected to CLKHUB02A module which takes sampling clock delivered by FPGA from main local oscillator. This signal should use high quality differential signalling cable – SATA cable should be used for this purpose.

<sup>1)</sup> <http://wiki.mlab.cz/doku.php?id=en:gpsdo> SDGPSDO design has been developed in parallel to this diploma thesis as a related project, but it is not explicitly required by specification.

## ■ 2.4.2 Signal cable connectors

Several widely used and commercially easily accessible differential connectors were considered.

- HDMI
- SATA
- DisplayPort
- SAS/miniSAS

MiniSAS connector was chosen as the best to be used in connecting multiple ADC modules. The miniSAS connector is compatible with existing SATA cabling system and aggregates multiple SATA cables to a single connector this cable type is shown on image 2.1. Translation between SATA and miniSAS is achieved by SAS to SATA adapter cable which is used in servers to connecting SAS controller to multiple SATA hard disc in RAID systems thus is commercially available. One drawback is that miniSAS PCB connectors are manufactured in SMT versions only. But outer metal housing of connector is standard trough hole type. This mechanical design should degrade durability of this connector type.



[img-miniSAS-cable]

Figure 2.1. A type of miniSAS cable similar to used.

## ■ 2.4.3 Signal integrity requirements

Used ADC modules has DATA clock frequency eight times higher than sampling frequency in single line output mode. This implicates 40 MHz output bit rate.

## ■ 2.4.4 Design of ADC modules

This modules have MLAB standard construction with four mounting holes in corner aligned in defined raster.

Data serial data output of ADC module should be connected directly to FPGA for basic primary signal processing. Used ADC chip has selectable bit width of data output bus thus output SATA connectors has signals arranged to contain a single bit from every ADC channel. This signal concept enables selection of proper bus bit-width according to sampling rate. (Higher bus bit-width downgrades signalling speed and vice versa.)

For connection of this signalling layout, miniSAS to multiple SATA cable should be used.

For PCB layout KiCAD design suite was used. Used version has the CERN Push & Shove routing capability integrated but was slightly unstable and sometimes falls on exception during routing. Design must be often saved due to this stability issues. But Open-source KiCAD works well compared to commercial solutions as MentorGraphics PADS or Cadence Orcad. And much better than widely used Eagle software.

New PCB footprints have been designed for FMC, SATA a and miniSAS connectors. These new footprints were committed to KiCAD github library repository. And they are now publicly accessible from official KiCAD repository at GitHub.

## 2.4.5 ADC selection

Several ADC signalling formats currently exist for communication with FPGA.

- DDR LVDS
- JEDEC 204B
- JESD204A
- Paralel LVDS
- Serdes
- serial LVDS

Serial LVDS has been selected because uses lowest number of differential pairs. This parameter is mandatory for construction complexity and reliability. <http://www.ti.com/lit/pdf/snua110>

An ultrasound AFE chips should be ideal for this purpose – this chips has front-end amplifiers and filters integrated. But theirs drawback is incapability of handling differential input signal and relatively low dynamic range (consists 12bit ADC). This IO has many ADC channels thus scaling are possible in factor of 4 receivers (8 analogue channels).

If we require separate output for every analogue channel and 16bit deph. Only several 2-Channel simultaneous sampling ADCs currently exists which meet these requirements. These ADCs parameters are summarised in table ??

ADC Type	LTC2271	LTC2190	LTC2191	LTC2192	LTC2193	LTC2194	LTC2195
SNR [dB]	84.1	77	77	77	76.8	76.8	76.8
SFDR [dB]	99	90	90	90	90	90	90
S/H Bandwidth [MHz]	200			550			
Sampling rate [MSPS]	20	25	40	65	80	105	125
Configuration				SPI			
Package	[ADC-types]	52-Lead	(7mm	■	8mm)		QFN

**Table 2.1.** Summary of available ADC types and theirs parameters.

All parts in this category are compatible with one board layout. Main differences are in sampling frequency and signal to noise ratio. The slowest one has maximal sampling frequency 20 MHz. But all types have minimal sampling frequency 5 MSPS.

All types were configurable over serial interface (SPI). SPI seems to be a standard for high-end ADC chips from main manufacturers (Analog Devices, Linear technology, Texas instruments, Maxim integrated..).

### 2.4.6 ADC modules interface

All two ADCdual01A modules was connected to FPGA ML605 board trough FMC2DIFF01A adapter board. Construction of this adapter module suppose FMC LPC connector. And this board is not MLAB compatible design. But this board is designed to meet VITA 57 standard specification for boards which uses zone 1 and zone 3. This specification guarantee compatibility with others FPGA board which has FMC LPC connector for Mezzanine Card. Schematic diagram of this adapter board is included in appendix.

Primary purpose of this PCB is to enable connection of ADC modules from space excluded from PC case. (In PC box analog circuits cannot be realised without using of massive RFI mitigation techniques). Differential signaling connectors should be used for conducting digital signal over relatively long cable. Signalintegrity sensitive links (clocks) are equipped by output driver and translator to LVPECL logic for better signal transmission quality.

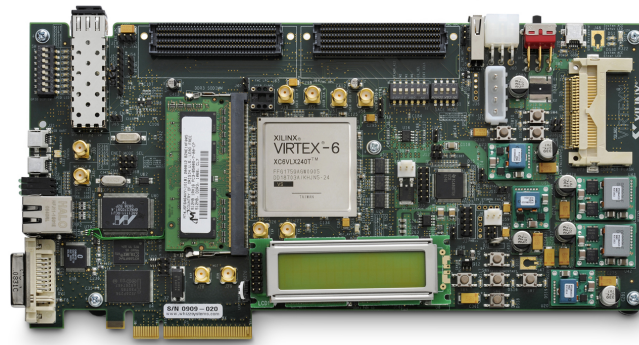


Figure 2.2. Used FPGA ML605 development board.

Several SATA connectors and two miniSAS connectors are populated on this board. This set of connectors allows connection of any number of ADC modules in range of 1 to 8. ADC data outputs should be connected to the miniSAS connectors. Other supporting signal should be routed directly to SATA connectors on adapter.

Signal configuration used in testing construction is described in tables.

### 2.4.7 Output data format

	160bit packet								
Data name	FRAME	ADC1 CH1	ADC1 CH2	ADC2 CH1	ADC2 CH2	ADC2 CH1	ADC2 CH2	ADC2 CH1	ADC2 CH2
Data type	uint32	int16	int16	int16	int16	int16	int16	int16	int16
Content	saw signal	$t_1$	$t_{1+1}$	$t_1$	$t_{1+1}$	$t_1$	$t_{1+1}$	$t_1$	$t_{1+1}$

Table 2.2. System device /dev/xillybus\_data2\_r data format

## 2.5 Achieved parameters

### 2.5.1 Data reading and recording

For reading data stream from ADC driver Gnuradio software was used. Gnuradio suite consist gnuradio-companion which is a graphical tool for creating signal flow graphs and generating flow-graph source code. This tool was used to create basic RAW data grabber to record and interactive view data stream output from ADC modules.

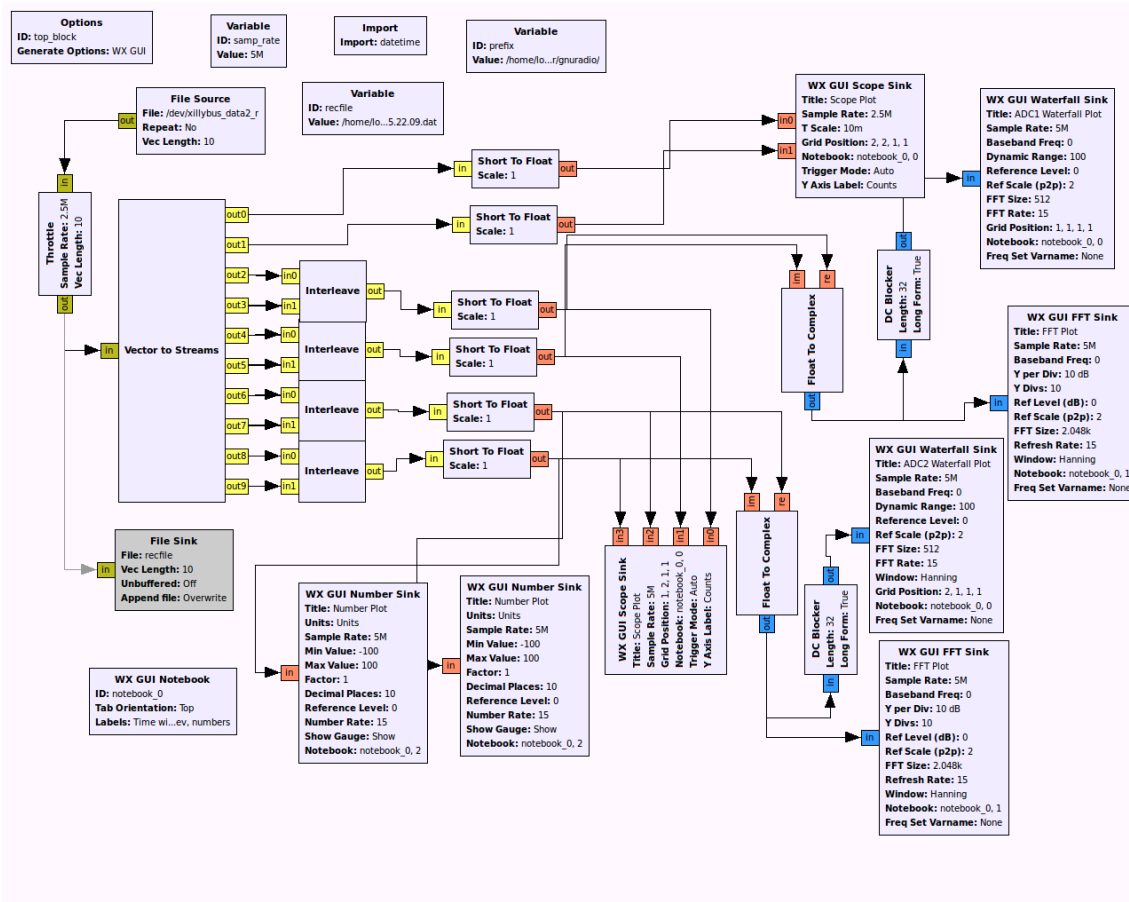


Figure 2.3. ADC recorder flow graph created in gnuradio-companion.

Interactive grabber viewer user interface shows live oscilloscope-like time-value display for all data channels and live time-frequency scrolling display (waterfall view) for displaying frequency components of grabbed signal.

### 2.5.2 ADC module parameters

Two pieces of ADC module design were realised and tested first piece denoted as ADC1 has LTC21190 ADC chip populated with LT660015 front-end operational amplifier. This ADC1 module has 1kOhm resistors populated on inputs which gives to module internal attenuation of input signal. Value of this attenuation  $A$  is described by formula

$$A = \frac{1580 \times R_1}{R_1 + R_2}$$

ADC1 CH1 maximal input 705.7 mV

LTC2271 6600125 1k ADC2 CH1 maximal input 380 mV

## 2. Trial design

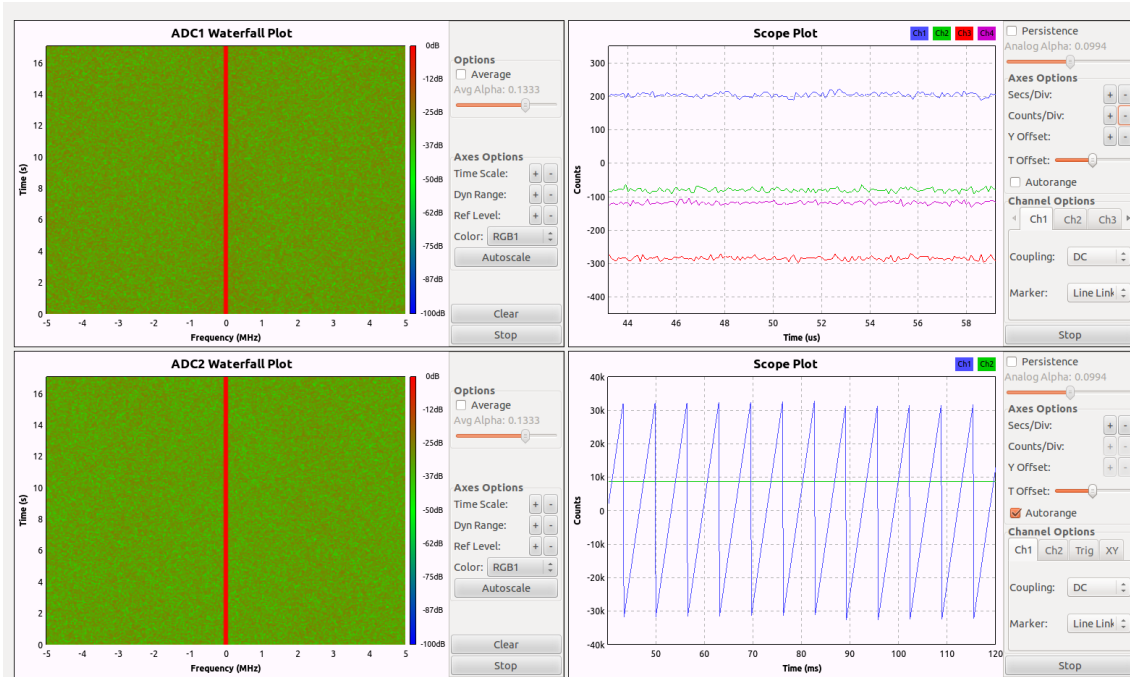


Figure 2.4. User interface window of running ADC grabber.

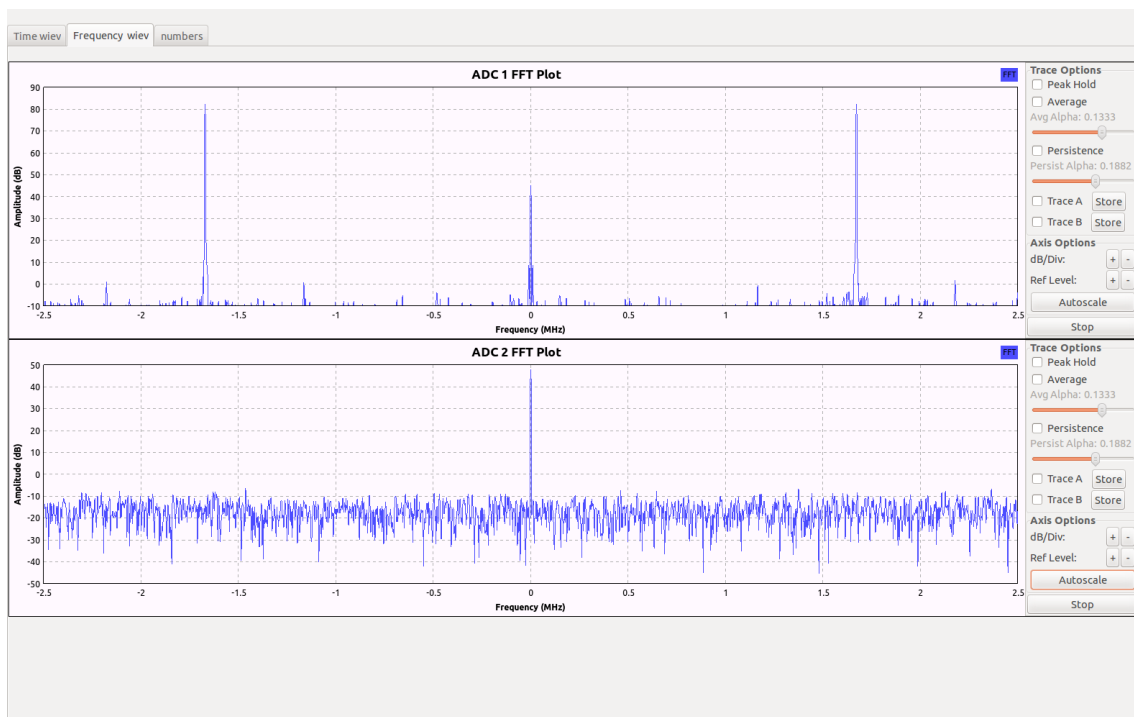
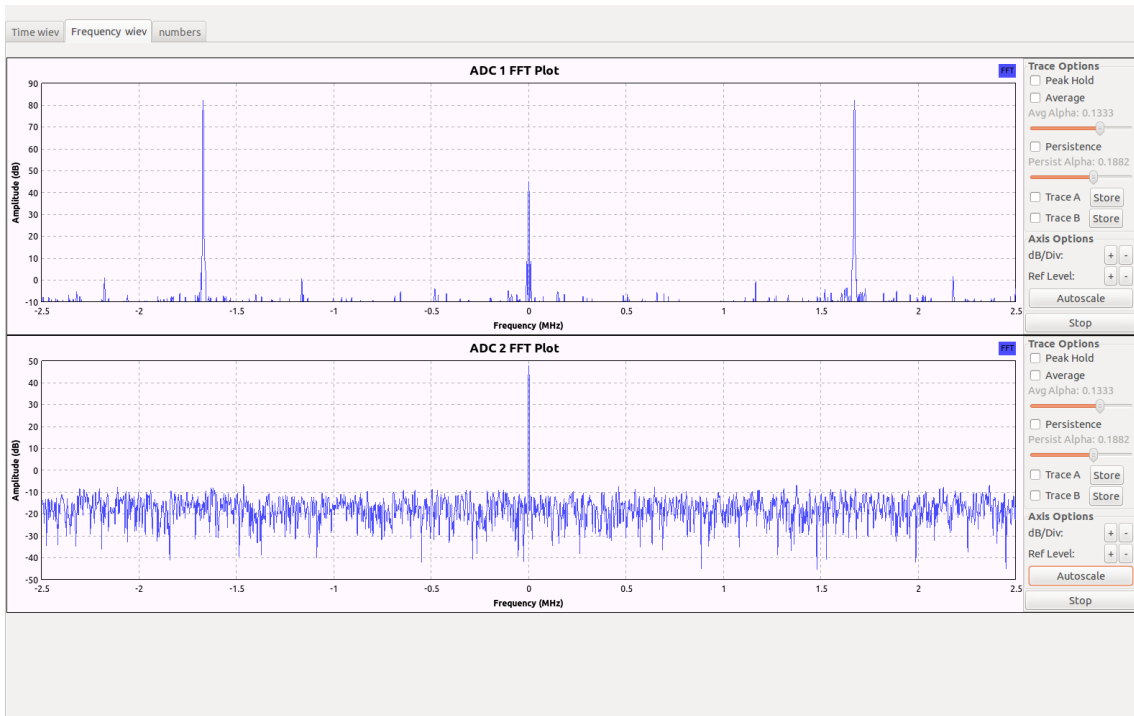


Figure 2.5. Sine signal from ADC1 module with LTC21190 and LT6600-5 devices.





**Figure 2.6.** Sine signal from ADC1 module with LTC21190 and LT6600-5 devices.

# Chapter 3

## Proposed final system

Construction of final system which should be used for real radioastronomy observations will be described. This chapter is mainly theoretical analysis of systems which should be used for data handling. Realisation of these ideas are planned for future development after full evaluation and testing of actual functional example design.

### 3.1 Custom design of FPGA board

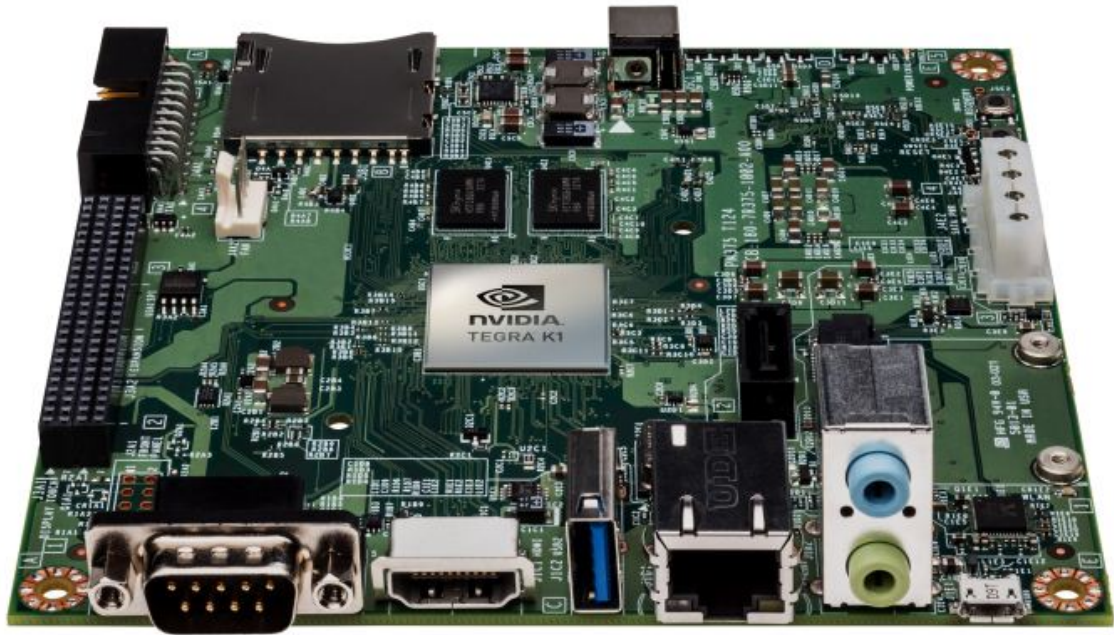
In beginning of the project custom design of FPGA interface board was supposed. This FPGA board should include PCI express interface and should have lower price than functional example construction. This board should have MLAB compatible design which is backward compatible with existing or improved design of ADC modules. For connection of this board an another adapter board with PCIe host interface was supposed. Thunderbolt technology standard was supposed for use in this PC to PCIe -> FPGA module. Thunderbolt chips are currently available on the market for reasonable prices. But specification for these devices are accessible for licensed users only and Intel has mass market oriented licensing policy, which makes this technology inaccessible for low quantity product design. In consequence of this external PCI Express cabling and expansion slots should be better solution.

But this systems and cables are still very expensive. For example (<http://www.opalkelly.com/products/x>) has price tag 995 USD at time of writing this thesis. Therefore better approach must be found.

### 3.2 Parralella board computer

### 3.3 GPU based computational system

A new GPU development board NVIDIA K1 has been released in recent time it is shown on image 3.1. This board are intended for use in computer vision, robotics, medicine, security, and automotive. This board has ideal parameters for signal processing for this relatively low price 192 USD. But it is currently in pre-order release stage (in April 2014).



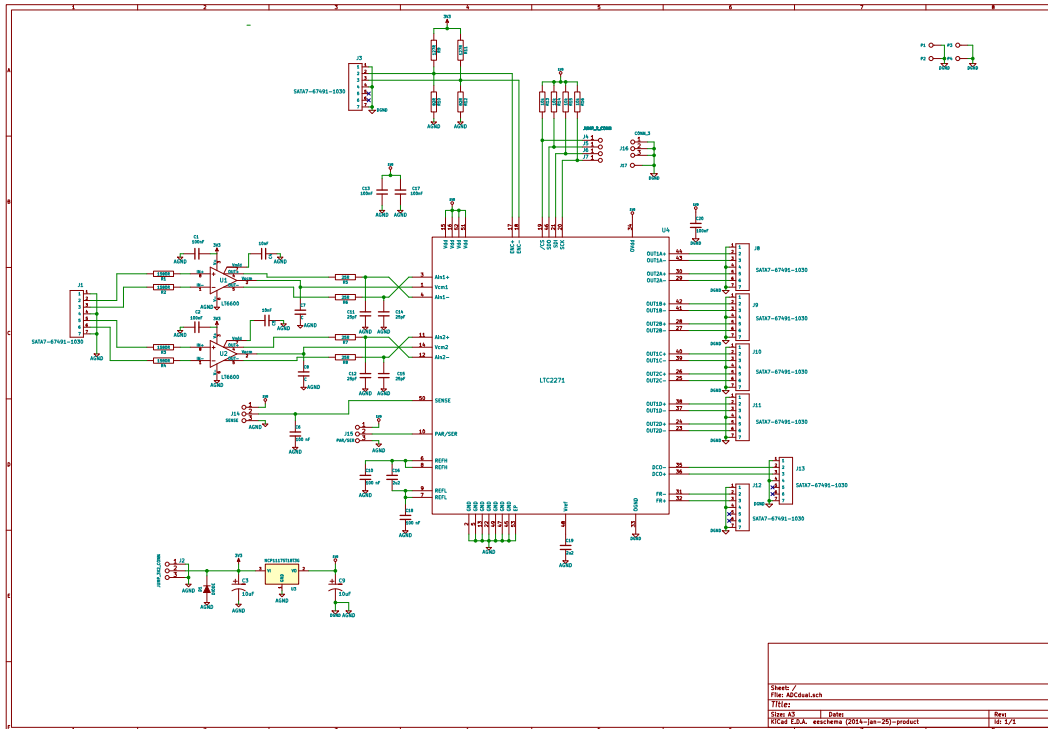
[img-NVIDIA-K1]

**Figure 3.1.** The NVIDIA Jetson TK1 Development Kit <https://developer.nvidia.com/jetson-tk1>.



# Appendix A

## Circuit diagram of ADCdual01A module





## Appendix **B**

### Circuit diagram of FMC2DIFF module

FMC\_connector

FMC.sch

SATA\_connectors

SATA.sch

miniSAS\_connectors

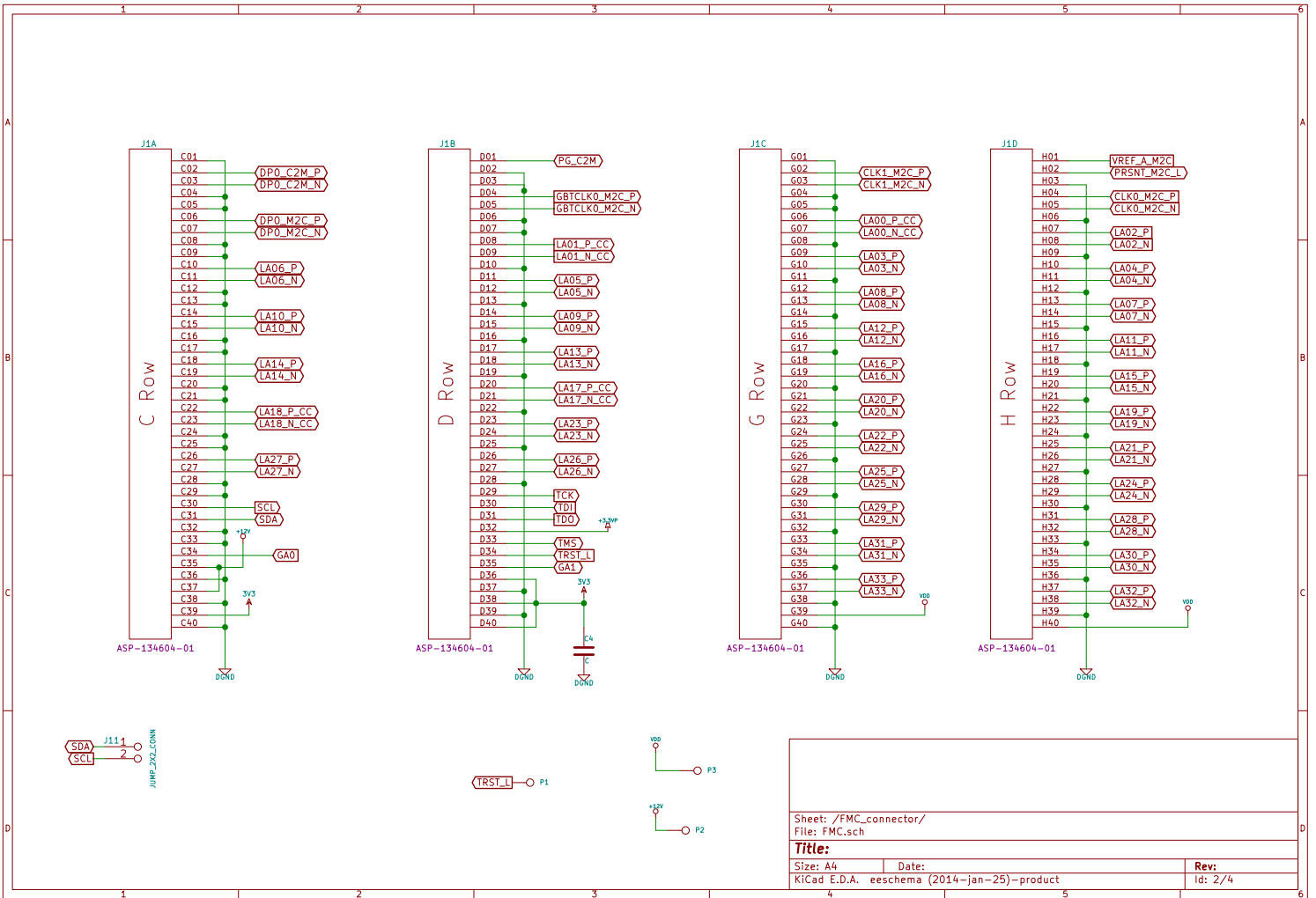
miniSAS.sch

Sheet: /  
File: FMC2DIFF.sch

**Title:**

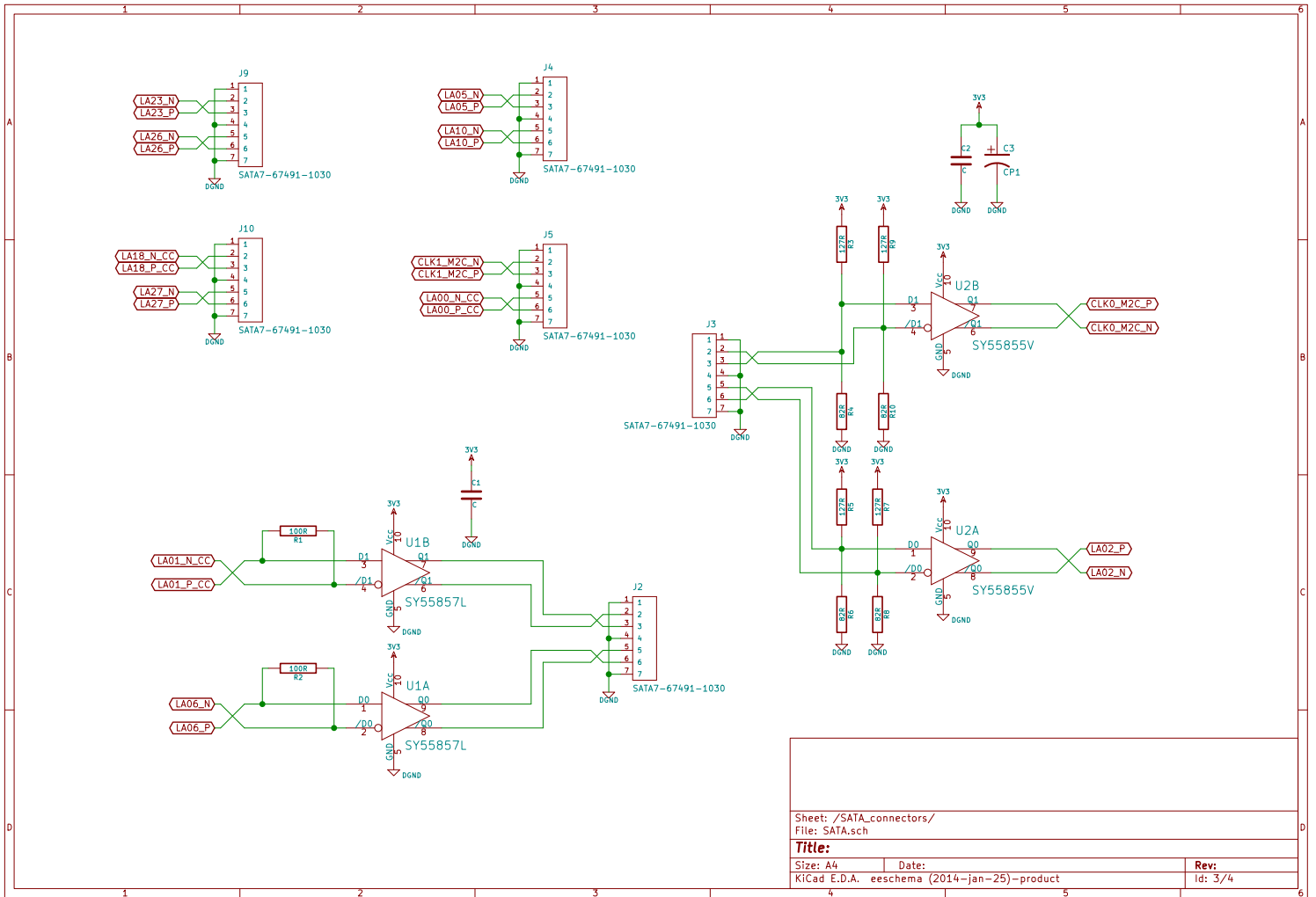
Size: A4 Date:  
KiCad E.D.A. eeschema (2014-jan-25)-product

Rev:  
Id: 1/4



Sheet: /FMC_connector/ File: FMC.sch		Title:	
Size: A4	Date:	Rev:	
KICad E.D.A. eeschema (2014-jan-25)-product		Id: 2/4	

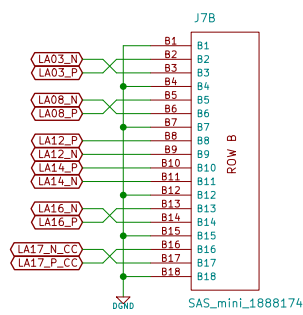
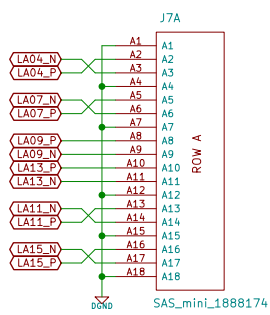
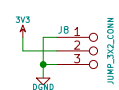
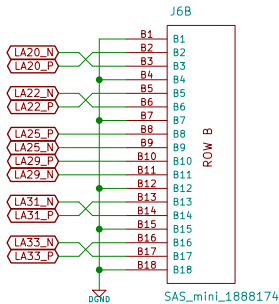
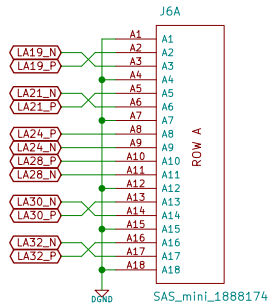




Sheet: /SATA\_connectors/  
 File: SATA.sch

**Title:**

Size: A4	Date:	Rev:
KiCad E.D.A.	eesschema (2014-jan-25)-product	Id: 3/4



Sheet: /miniSAS_connectors/ File: miniSAS.sch		
<b>Title:</b>		
Size: A4	Date:	Rev:
KiCad E.D.A.	eeschema (2014-jan-25)-product	Id: 4/4