Master's thesis

**Czech
Technical
University
in Prague**

F3

**Faculty of Electrical Engineering
Department of Measurement**

Fast multi-channel data acquisition system for radio-astronomy receiver

Jakub Kákona
Aircraft and Space Systems

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

Fakulta elektrotechnická
Katedra měření

Akademický rok **2013-2014**

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student: **Bc. Jakub Kákona**

Studijní program: **Kybernetika a robotika**
Obor: **Letecké a kosmické systémy**

Název tématu česky: **Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač**

Název tématu anglicky: **Fast multi-channel data acquisition system for radio-astronomy receiver**

Pokyny pro vypracování:

Proveďte rešerši a analyzujte stávající řešení vhodná pro danou aplikaci.

Navrhněte A/D modul pro digitalizaci radioastronomických dat založených na příjmu odražených pozemních signálů, ke konstrukci použijte dostupné ADC obvody. Jako datový koncentrátor pro přenos dat do PC využijte FPGA. Navrhněte připojení ADC modulů k FPGA a specifikujte požadavky na funkcionalitu implementovanou v FPGA. Výsledný VHDL design bude poskytnut.

Parametry: vzorkovací frekvence 1 MHz, možnost připojení 1 až 8 přijímačů (každý dva analogové kanály), rozlišení alespoň 12 bitů.

Návrh koncipujte škálovatelný, HW nechť sestává ze společné části a částí pro každý přijímač. Zkonstruujte funkční vzor zařízení. Využijte vývojovou desku ML605 s FPGA Virtex 6.

Převodník otestujte alespoň s jedním přijímačem a demonstrujte záznam dat a jejich zpracování.

Na základě otestování prototypu navrhněte (bez realizace) vlastní desku s FPGA a podpůrnými moduly.

Seznam odborné literatury:

[1] Vedral, J., Fischer, J.: Elektronické obvody pro měřicí techniku. Vydavatelství ČVUT, Praha 2004, ISBN 80-01-02966-2

[2] Richards, M.A., Scheer, J. A., Holm, W. A.: Principles of modern radar. Sci Tech Publishing, 2010, ISBN 978-1891121-52-4

Vedoucí diplomové práce: Ing. Martin Matoušek, Ph.D. (K13133)

Datum zadání diplomové práce: 14. ledna 2014

Platnost zadání do[1]: 31. srpna 2015

L.S.

Prof. Ing. Vladimír Haasz, CSc.
vedoucí katedry

Prof. Ing. Pavel Ripka, CSc.
děkan

V Praze dne 14. 1. 2014

[1] Platnost zadání je omezena na dobu tří následujících semestrů.

Acknowledgement / Declaration

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.

V Praze dne 12. 5. 2014

....

Abstrakt / Abstract

Dnešní radioastronomická pozorování jsou kvůli rušení a potřebě získat velké úhlové rozlišení realizována jako víceanténní přijímací systémy. Takto konstruovaná zařízení mají ale značné nároky na kvalitu zpracování signálu z více kanálů. K práci mě motivovala moje amatérská radioastronomická aktivita při sledování meteorů.

Diplomová práce se zabývá možnou realizací digitalizační části přijímače radioastronomických signálů. Popsaná realizace je optimalizována na vysoký dynamický rozsah vstupních signálů a dobrou fázovou stabilitu, což jsou nejvýznamnější parametry pro použití ve víceanténních systémech. Návrh i konstrukce jsou koncipovány jako open-source hardwarové řešení, které má zatím jedinečné parametry v oblasti přístrojů určených pro amatérskou i profesionální radioastronomii.

V diplomové práci jsem navrhl a realizoval zkušební verzi zařízení. Experimentoval jsem s ním. Ze zkušeností vyplývají doporučení pro opakovanou realizaci přijímačů, kterou chceme v amatérské síti pro sledování meteorů mnohonásobně zopakovat.

Klíčová slova: Radioastronomie, digitalizace signálu, A/D konverze

Překlad titulu: Rychlý vícekanálový systém sběru dat pro radioastronomický přijímač

Due to the ubiquitous presence of interference and a need for a large angular resolution, the current radioastronomical observations are carried out using multi-antenae receiver systems. Construction of such devices places great demands upon the quality of signal processing. A source of inspiration for my diploma thesis has been my own amateur radioastronomical activity in the field of meteor observations. The thesis deals with a possible realization of a digitalization unit for a radioastronomical signal receiver. The implementation described in the thesis is optimized for a high dynamic range and good phase stability, both being the most important parameters for its application in the multi-antenae systems. Design and the instrument implementation have been created as open-source hardware solutions, so far having unique characteristics among the devices used in amateur or professional radioastronomy. I have devised and implemented a trial version and made further experiments with it. A resulting recommendations for repeated implementations of the receivers, that we are planing to use in the amateur meteor observing networks, are based on these experiences.

Keywords: ADC interface, radioastronomy, signal digitalisation

Contents /

Tables / Figures

Chapter 1
Introduction

1.1 Current radioastronomy problems

From a radioastronomer's point of view, it is important that radioastronomy focuses its interest primarily on natural signals originating in the surrounding universe. It does not pay much attention to the man-made signals created by our civilisation.

However, it is due to these artificial signals, that the current radioastronomy faces a disturbance issue. The issue arises from the fact, that there are so many terrestrial transmitters currently active. All of them are sources of a dense signal mixture which can cause trouble not only to radioastronomers.

As a consequence, there already exists an effort to control the radiofrequency spectrum. As result of attempts to control the radiofrequency spectrum, the frequency allocation table was created [1]. The radio-frequency allocation table contains special bands allocated to radioastronomy use. However, for many reasons these bands are not clean enough to be used in radioastronomy observations directly. As a result, we cannot work in the same way as did the radioastronomers in the very beginnings of radioastronomy do. Many experiments, namely Cosmic microwave background detection or pulsar detection, cannot be realised nowadays in their original forms with satisfactory results.

Supporting evidence of such an effect is RadioJOVE project. NASA engineers who originally created the RadioJOVE project had a great idea. The RadioJOVE project brought an opportunity for creating a publicly available, cheap radioastronomy receiver. However, they used an old-fashioned construction design which, on one hand, can operate in unoccupied harsh environments like deserts, but on the other hand it simply did not meet the criteria that would make it possible to be used in modern civilisation, as we know it in Europe [2]. The source of its dysfunction is a presence of strong radiofrequency interferences. These interferences are orders of magnitude stronger than Jupiter decametric emissions, whose detection was the main aim of the RadioJOVE project. From what we have already seen in the light pollution mitigation pursuit, there is only a small chance to improve the situation in radiofrequency spectrum radically.

The only way to overcome this problem is to search for new methods of radioastronomy observations, new methods which allows us to work without completely clear radiofrequency bands and which allow us to see the surrounding universe even despite the existence of man-made radiofrequency interference mixture. One solution is to use already known natural radio frequency signals parameters. Natural signals usually have different signal properties than local interference. Natural objects do not have problems with transmission in bandwidths of tens of megahertz in sub 100 MHz bands. These objects are usually far away and the same signal could be received at almost half of the Earth globe without any significant differences. On the other hand, it is obvious that signals with such parameters have some drawbacks, namely in the reception power. The reception power of radioastronomical object is $1 \cdot 10^9$ smaller than signal power received from a typical broadband radio transmitter.

From the above mentioned facts concerning the natural radio signals we can conclude that modern requirements imposed on a radioastronomy receiver are completely different from the requirements existing back in the history. Radioastronomy is no longer limited by an access to electronic components, today it is rather limited by the everywhere presence of electronic.

▪ 1.2 Radio astronomy receiver

At the beginnings of radioastronomy, the receivers were constructed as simple stations with a single antenna or a multiple antenna array with fixed phasing. This approach was used because of the existing limits of electronic components and technologies. The main challenges of those times were problems of noise number and low sensitivity, both present due to the poor characteristics of active electronic components such as transistors and vacuum tubes.

Most of the present-day operating radioastronomy equipment has been constructed in a similar manner. It was produced usually shortly after the WWII or during the Cold War as a part of the military technology.

We have an access today to components with much higher quality, repeatability and a lower price as compared to the components accessible to previous generation of radioastronomers. That is why we can develop a better radioastronomical equipment, powerful enough to make new astronomical discoveries possible.[1])

We have the capacities necessary to develop a receiver which will have a wide bandwidth, a high third-order intercept point and preferably an option for phase and frequency locking to other receivers located at another radioastronomical site at the Earth. Currently there exist several receivers with the above-mentioned parameters, for example USRP2, USRP B210 or HackRF, which are commercially available. However all of them lack scalability and have higher prices unaffordable to our amateur radioastronomy network. Scalability and redundancy that are the main requirements of noise reduction algorithms which motivated this diploma project.

New radio astronomy systems such LOFAR are explicit examples of the scalability and redundancy approach. LOFAR has a completely different and novel structure developed to solve the problems of radioastronomy signal reception. It uses exclusively multi-antenna arrays and mathematical algorithms for signal handling. Radio signals recorded by LOFAR can be used in multiple ways: radio images can be computed (if sufficient cover of u/v plane is achieved), the radiation intensity can be measured, the spectrum can be analysed for velocity measurement, etc.

▪ 1.3 Required receiver parameters

The novel approach of the receiver construction described above goes hand-in-hand with new requirements on receiver parameters as well. No additional attempts to improve the signal-to-noise ratio on single antenna have been performed currently. There are however other parameters requested nowadays.

▪ 1.3.1 Sensitivity and noise number

Sensitivity and noise number are parameters that are tied together. However, the requirement for multi-antenna and multi-receiver arrays forces to keep the price of

---

[1]) Most of astronomy-related discoveries in the last fifty years came from radioastronomy.

receiver at the minimal value. This implies that the sensitivity and noise number have to be at least so good in the detection (signal / noise > 1) of an observed object, that it would be detected on the majority of receivers connected to an observation network.

■ 1.3.2 Dynamic range

The dynamic range represents a huge problem of current radioastronomical receivers. This parameter is enforced by humans present everywhere and creating electromagnetic inference (EMI) radiation on radio frequency (RF) band. The modern radioastronomy receiver must not be saturated by these high levels of signals but still needs to have enough sensitivity to see faint signals from natural sources. The dynamic range is limited either by the construction of the analog circuitry in the receiver or by the digitization unit. The maximal theoretical dynamic range of analog-to-digital converter (ADC) could be estimated from ADC bit depth using a following formula (1)

$$D.R. \, [dB] = 20 \cdot \log(2^n) \tag{1}$$

The formula (1) provides values shown in Table 1.1 below.

ADC Bits	Dynamic range [dB]
8	48
10	60
12	72
14	84
16	96
24	144

Table 1.1. Standard bit depths of ADC and its theoretical dynamic range.

If we look at the actual spectrum occupancy in Europe (measured in the power spectral density), we see that the signal dynamic range in spectra easily reaches more than 80 dB above natural noise levels [3]. If we do not want to deal with the receiver saturation or the poor sensitivity, we need a receiver and digitization unit which has a comparable dynamical range with received signals. This implies the use of 14 bit ADC at least without any spare of range. However, the 16 bit range should be optimal as we have spare range for the strongest RF signals. Two bytes sample range has in addition a good efficiency in use standard power of 2 data types length. We selected the 16 bit digital range as the optimal one for our design.

■ 1.3.3 Bandwidth

Historically, the bandwidth parameter in radioastronomical receivers used to be within the kilohertz range. Such a narrow bandwidth was acceptable because observations were processed directly by listening or by a paper chart intensity recorder. The chart recorder integrated the energy of a signal over a defined narrow bandwidth which was suitable for detecting the intensity variance of a microwave background. No wide-band transmitters existed in that era (except for TV transmitters) and tuning to other neighbouring frequency was easy as they were mostly vacant. Parallel observations from several places were unnecessary as well because the electromagnetic conditions were nearly same at all locations.

1.4 State of the art in receivers digitization units

Only a few digitization systems dedicated to radioastronomy exist currently. Today's systems use either a custom design of the whole receiver or they are constructed from commercially available components. Open-source principle attempts are very rare in the radioastronomy field.

1.4.1 Custom digitization system

Custom designs usually use non-recurring engineering for the development of a specific solution for an observation project. Consequently, such instruments are very costly if the developed instrument is not reproduced many times. A typical example of the instrument developed and manufactured in a single piece with enormous funding requirements was the Arecibo ALFA.

Another example, this time a custom-designed receiver and digitization unit design but duplicated many times is LOFAR system developed by Astron in the Netherlands [4] LOFAR is the innovative radioastronomy system which uses a phased antenna array approach in an enormous scale. Thousands (around $2 \cdot 10^4$) of antennas are manufactured an deployed in the field. The centrer of LOFAR system is situated in the Netherlands and peripheral antennas and a connection network are extended to other European countries.

Figure 1.1. One LOFAR LBA antenna element.

LOFAR project must use a low cost hardware due to the system scale. A special construction techniques were employed to keep the overall project budget at acceptable levels (specially designed polystyrene supporting blocks for High Band Antenna (HBA) for example). Many of used components are manufactured in a mass scale for other than scientific use. LBA antennas masts are made from a standard Polyvinyl chloride (PVC) plastic waste pipes. LOFAR uses low cost direct sampling receiver. The entire project was designed by the Netherlands Institute for Radio Astronomy, which produces many similarly sophisticated devices [5].

1.4.2 Modular digitization systems

Due to cost restrictions in science and astronomy instruments development, a reuse of engineering work is preferable. There is one example of a modular digitization and data processing system. The system Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) has been in development at the University of Berkeley [6] since around 2005. CASPER designers an engineers noticed a remarkable lack of such a hardware in radioastronomy science. Their ideas are summarised in the paper [7]. Unfortunately they use a proprietary connector standard and technology. They developed a modular system based purely on Tyco Z-DOK+ connectors family. CASPER data processing board with Z-DOK connectors is shown in Figure 1.2. Z-DOK connectors have a relatively high pricing (around 40 USD) [8]. Z-DOK connectors are a high quality differential pairs connectors. However, the price of these connectors is comparable with the price of one ADC channel in our design described in this diploma thesis.
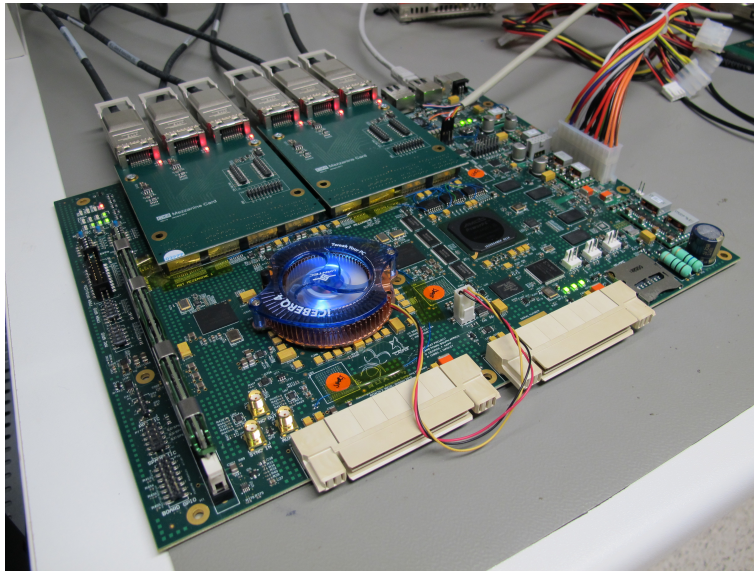
Figure 1.2. CASPER project ROACH-2 data processing board. White Z-DOK connectors for daughter ADC Boards can be easily seen in the front of the board.

In the contrary to professional astronomers, who use proprietary digitization units, amateur radioastronomers have been using multichannel sound cards [9] or self designed digitalisation units. Devices constructed by amateurs are usually non reproducible [10]. It is evident that the current radioastronomy lacks a proper hardware which could be used by both communities, professionals and amateurs. The optimal solution in such a situation should be the open-source hardware. We follow this path in this diploma project.

Chapter 2
Trial version of the receiver, design and implementation

The whole design of radioastronomy receiver digitalization unit is constructed to be used in a wide range of applications and tasks related to digitalization of signal from radioastronomy receivers. A good illustrating problem for its use is a signal digitalisation from multiple antenna arrays.

2.1 Required parameters

We require the following technical parameters, to supersede existing digitalization units solutions. Primarily, we need wide a dynamical range and high IP3. The receiver must accept wide dynamic signals because a typical radioastronomical signal has a form of a weak signal covered by a strong man-made noise or other undesired noises as lighting, Sun emissions etc.

Summary of other additional required parameters follows

- Dynamical range better than 80 dB, see section ?? for explanation
- Phase stability between channels
- Low noise (all types)
- Sampling jitter better than 100 metres
- Support for any number of receivers in the range of 1 to 8

Now we analyze several of the parameters in detail.

2.2 Sampling frequency

Sampling frequency is not limited by the technical constrains in the trial version. This parameter is especially limited by the sampling frequencies of analog-to-digital conversion chips available on the market and interface bandwidth. Combination of the required parameters – dynamic range requiring at least 16bit and a minimum sampling frequency of 1 MSPS leads to the need of high end ADC chips which does not support such low sampling frequencies at all. Their minimum sampling frequency is 5 MSPS.

We calculated a minimum data bandwidth data rate for eight receivers, 2 bytes per sample and 5 MSPS as $8 \cdot 2 \cdot 5 \cdot 10^6 = 80$ MB/s. Such data rate is at the limit of the actual writing speed of classical HDD and it is almost double the real bandwidth of USB 2.0 interface. As a result of these facts we must use faster interface. Faster interface is especially needed in cases where we require faster sampling rates than ADC's minimal 5 MSPS sample rate. The most perspective interface for use in our type of application is USB 3.0 or PCI Express interface. However, USB 3.0 is a relatively new technology without good development tools currently available. We have used PCI Express interface as the simplest and the most reliable solution.
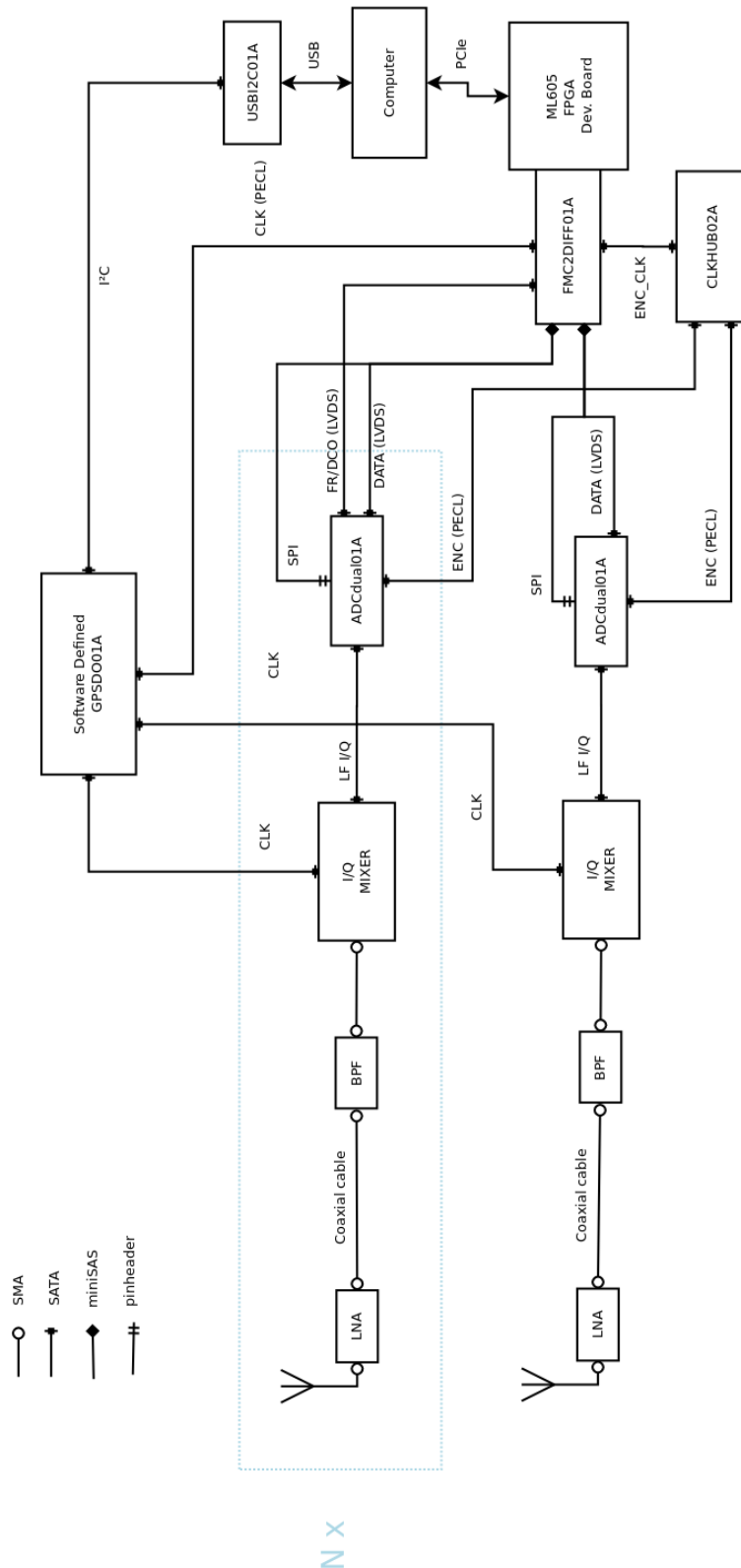
Figure 2.1. Expected realisation of signal digitalisation unit.

2.3 System scalability

For analogue channels' scalability, special parameters of ADC modules are required. Ideally, there should be a separate output for each analogue channel in ADC module.

ADC module must also have separate outputs for frames and data output clocks. These parameters allow for conduction at relatively low digital data rates. As a result, the digital signal can be conducted even through long wires. Modular concept allows a separation from central logical unit which supports optimization of number analogue channels.

Clock and data signals will be then handled distinctively in our modular scalable design. Selected ADC chips are guaranteed to have defined clock skew between the sampling and data output clocks. This allows taking data and frame clocks from the first ADC module only. The rest of the data and frame clocks from other ADC modules can be measured for diagnostic purposes (failure detection, jitter measurement etc.), but these redundant signals are not used for data sampling. If more robustness is required in the final application, DCO and FR signals may be collected from other modules and routed through an voting logic which will correct possible signal defects.

This system concept allows for scalability, that is technically limited by a number of differential signals on host side and its computational power. There is another advantage of scalable data acquisition system – an economic one. Observatories or end users can make a choice of how much money are they willing to spent on radioastronomy receiver system. This freedom of choice is especially useful for science sites without previous experience in radioastronomy observations.

■ 2.3.1 Differential signalling

The above mentioned concept of scalable design requires relatively long circuit traces between ADC and digital unit which captures the data and performs the computations. The long distance between the digital processing unit and the analog-to-digital conversion unit has an advantage in noise retention typically produced by digital circuits. Those digital circuits, such as FPGA , Ethernet or other flip-flops blocks and circuit traces, usually work at high frequencies and emit wide-band noise with relatively low power. In such cases any increase in a distance between the noise source and analog signal source increase S/N significantly. However, at the same time, a long distance brings problems with the digital signal transmission between ADC and computational unit. But this obstacle should be resolved more easily in free-space than on board routing. The high-quality differential signalling shielded cables should be used, such as massively produced and cheap SATA cables. This technology has two advantages over PCB signal routing. First, it can use twisted pair of wires for leak inductance suppression in signal path and second, the twisted pair may additionally be shielded by uninterrupted metal foil.

■ 2.3.2 Phase matching

For multiple antenna radioastronomy projects, system phase stability is a mandatory condition. It allows a precise, high resolution imaging of objects, increases signal to noise ratios in several observation methods and allows the use of advanced algorithms for signal processing.

High phase stability in our scalable design is achieved through centralized frequency generation and distribution with multi-output LVPECL hubs (CLKHUB02A), that have equiphased outputs for multiple devices. LVPECL logic is used on every system critical clock signal distribution hub. LVPECL logic has an advantage over LVDS in signal integrity robustness. LVPECL uses higher logical levels and higher signalling currents. Power consumption of LVPECL logic is nearly constant over the operating frequency range due to the use of bipolar transistors. This minimizes voltage glitches

which are typical for CMOS logic. One drawback of its parameters is a high power consumption of LVPECL logic which easily reaches tens of milliamperes per device.

This design ensures that all system devices have access to the defined phase and known frequency.

2.4 System description

This section deals with the description of the trial version based on Xilinx ML605 development board 2.6. The board had been used in a previous project and has not been used since then, but the FPGA parameters are more than sufficient of what we need for fast data acquisition system.

2.4.1 Frequency synthesis

We have used a centralized topology as a basis for frequency synthesis. One precise high-frequency and low-jitter digital oscillator has been used [11], while other working frequencies have been derived from it by the division of its signal. This central oscillator has a software defined GPS disciplined control loop for frequency stabilization.[1]) We have used new methods of software frequency monitoring and compensation in order to meet modern requirements on radioastronomy equipment which need precise frequency and phase stability over a wide baseline scales for effective radioastronomy imaging.

The GPSDO device consists of Si570 chip with LVPECL output. Phase jitter of GPSDO is determined mainly by Si570 phase noise. Parameters of the Si570 are summarized in the following table 2.1 (source [12]).

The GPSDO design, that is included in data acquisition system, has special feature – it generates time marks for a precise time-stamping of the received signal. Timestamps are created by disabling the local oscillator's outputs, connected to SDRX01B receivers, for 100 us. As result, a rectangular click in the ADC input signal is created which appears as a horizontal line in spectrogram. Timestamps should be seen in image 3.7 (above and below the meteor reflection).

Time-marking should be improved in future by digitalization of GPS signal received by antenna on observational station. Following that, the GPS signal can be directly sampled by a dedicated receiver and one separate ADC module. Datafile then consists of samples from channels of radio-astronomy receivers along with the GPS signal containing precise time information.

| | Phase Noise [dBc/Hz] | |
Offset Frequency	F_{out} 156.25 MHz	F_{out} 622.08 MHz
100 [Hz]	–105	–97
1 [kHz]	–122	–107
10 [kHz]	–128	–116
100 [kHz]	–135	–121
1 [MHz]	–144	–134
10 [MHz]	–147	–146
100 [MHz]	n/a	–148

Table 2.1. Phase noise of the used Silicon Laboratories Si570 chip. Offset frequency is measured from carrier frequency. Values shown in the table are given for two different carrier frequencies.

---

[1]) SDGPSDO design has been developed in parallel to this diploma thesis as a related project, but it is not explicitly required by the thesis itself and thus it is described in a separate document

9

Every ADC module will be directly connected to CLKHUB02A module which takes sampling clock signal delivered by FPGA from the main local oscillator. This signal should use high quality differential signalling cable – we should use SATA cable for this purpose. FPGA may slightly affect the clock signal quality by adding a noise, but it has a negligible effect on the application where developed system will be used.

◼ 2.4.2 Signal cable connectors

Several widely used and commercially easily accessible differential connectors were considered to be use in our design.

- HDMI
- SATA
- DisplayPort
- SAS/miniSAS

At the end, MiniSAS connector was chosen as the best option to be used in connecting together multiple ADC modules. A transition between SATA and miniSAS is achieved by SAS to SATA adapter cable which is commonly used in servers to connect SAS controller to multiple SATA hard disc in RAID systems and thus is commercially easily available. It is compatible with existing SATA cabling systems and aggregates multiple SATA cables to a single connector. It also has SPI configuration lines which can be seen in the following picture 2.2 as standard pinheader connector. The main drawback of miniSAS PCB connectors lies in the fact, that they are manufactured in SMT versions only. SMT design may eventually decrease the durability of the connector even if outer metal housing of connector is designed to be mounted using a standard through-hole mounting method.
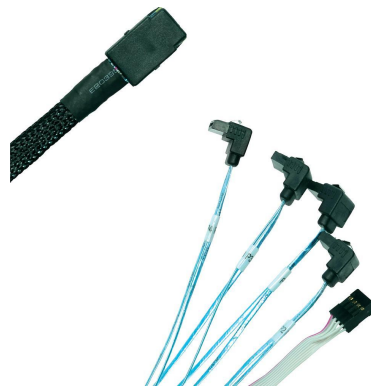
Figure 2.2. An example of miniSAS cable similar to used.

◼ 2.4.3 Signal integrity requirements

We use ADC devices that have DATA clock frequency eight times higher than sampling frequency in a single line output mode, implying a 40 MHz output bit rate. This implies a $1/4 \cdot 10^7 = 25$ ns time length of data bit, which is equivalent to 7.5m light path in free space. If we use copper PCB with FR4 substrate layer or coaxial/twinax cable, we could obtain velocity factor of 0.66 at worst condition. Then the light path for the same bit rate t_s will be 4.95 m. Although we do not have any cables in the system with comparable lengths, the worst data bit skew described by data sheets of the used components is $0.3 \cdot t_s$, which is 1.485 m. Therefore the length matching is not critical in our current design operating on lowest sampling speed. Length matching may become

critical in future versions with higher sampling rates, where the cable length must be matched. However SATA cabling technology is already prepared for that case and matched SATA cables are a standard merchandise.

2.4.4   ADC modules design
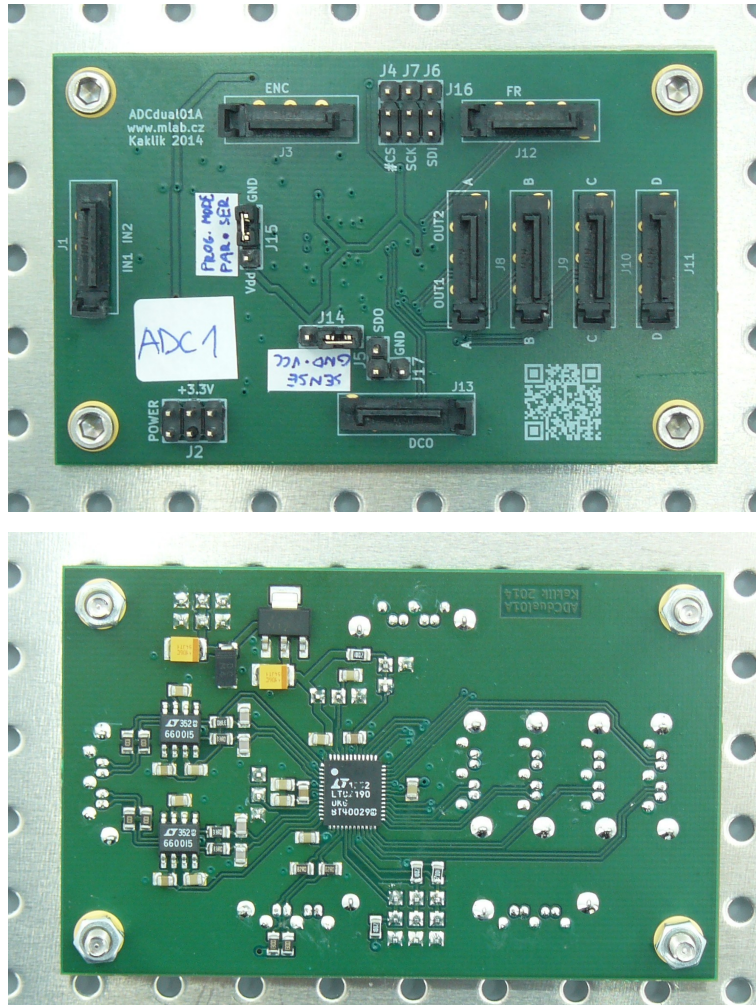
Figure 2.3. Realised PCB of ADCdual01A modules. Differential pairs routings are clearly visible.

2.4.5   ADC selection

There exist several standard ADC signalling formats currently used in communication with FPGA.

- DDR LVDS
- JEDEC 204B
- JESD204A
- Paralel LVDS
- Serdes
- serial LVDS

As a result of our need to use the smallest number of cables possible, the choice fell on the serial LVDS format. Small number of differential pairs is an important parameter

11

determining the construction complexity and reliability[13]. No many currently existing ADC devices have this kind of digital interface. An ultrasound AFE device chips seem to be ideal for this purpose – the chip has integrated both front-end amplifiers and filters. It has a drawback though - it is incapable of handling differential input signal and has a relatively low dynamic range (as it consists only of 12bit ADC) and has many single ended ADC channels. Consequently, the scaling is possible only by a factor of 4 receivers (making 8 analogue single ended channels).

If we add a requirement of separate output for every analogue channel and a 16bit depth we find that there are only a few 2-Channel simultaneous sampling ADCs currently existing which meet these criteria. We have summarized those ADCs in the following table 2.2

ADC Type	LTC2271	LTC2190	LTC2191	LTC2192	LTC2193	LTC2194	LTC2195
SNR [dB]	84.1	77	77	77	76.8	76.8	76.8
SFDR [dB]	99	90	90	90	90	90	90
S/H Bandwidth [MHz]	200				550		
Sampling rate [MSPS]	20	25	40	65	80	105	125
Configuration				SPI			
Package			52-Lead (7mm × 8mm) QFN				

Table 2.2. The summary of the currently available ADC types and theirs characteristics.

All parts in this category are compatible with one board layout. The main differences lay in the sampling frequency and signal to noise ratio, with the slowest having a maximum sampling frequency of 20 MHz. However, all of them have a minimal sampling frequency of 5 MSPS and all are configurable over a serial interface (SPI). SPI seems to be a standard interface used in high-end ADC chips made by the largest manufacturers (Analog Devices, Linear technology, Texas instruments, Maxim integrated..). We have selected two slowest types for our evaluation design. Following that, a PCB for this part have been designed. We have decided that ADCdual01A modules will have a standard MLAB construction layout with four mounting holes in corners aligned in defined raster of 400 mils.

Data serial data outputs of ADC modules should be connected directly by LVDS signalling levels conducted by SATA cables to FPGAs for the basic primary signal processing. The ADC chips used in the modules have a selectable bit width of data output bus and thus the output SATA connectors have signals arranged to contain a single bit from every ADC channel. This creates a signal concept enabling a selection of proper bus bit-width according to the sampling rate (higher bus bit-width downgrades signalling speed and vice versa.)

In order to connect the above mentioned signalling layout, miniSAS to multiple SATA cable should be used as described in section 2.4.2.

A KiCAD design suite had been chosen for PCB layout. However, the version, despite having integrated CERN Push & Shove routing capability, is slightly unstable as it sometimes crushes due to an exception during routing. On the basis of these stability issues, the design had to be saved quite often. On the other hand, compared to commercially available solutions, such as MentorGraphics PADS or Cadence Orcad, the Open-source KiCAD provides an acceptable option and it easily surpasses a widely used Eagle software.

As a part of work on the thesis, new PCB footprints for FMC, SATA, ADCs a and miniSAS connectors have been designed and were committed to KiCAD github library repository. They are now publicly available on the official KiCAD repository at GitHub.

ADCdual01A module has several digital data output formats. Difference between these modes lays in the number of differential pairs used.

- 1-lane mode
- 2-lane mode
- 4-lane mode

All of the above-mentioned modes are supported by the module design. For the discussed data acquisition system, the 1-lane mode was selected. 1-lane mode allows a minimal number of differential pairs between ADCdual01A and FPGA. Digital signalling scheme used in 1-lane mode is shown in the following image 2.4.
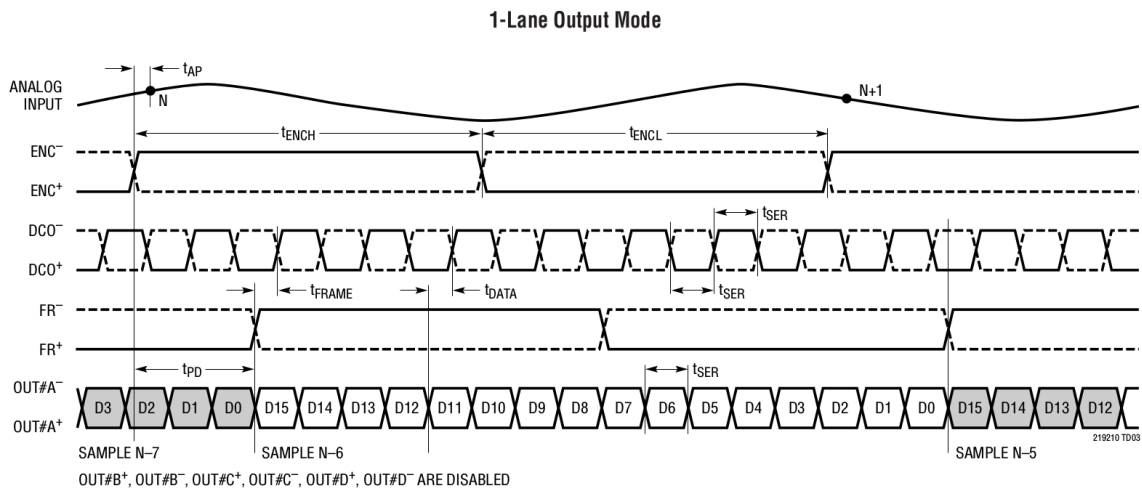
1-Lane Output Mode

Figure 2.4. Digital signalling schema for 1-line ADC digital output mode.

ADCdual01A parameters can be set either by jumper setup (referred to as a parallel programming in the device's data sheet) or by SPI interface. SPI interface has been chosen for our system, because of the parallel programming's lack of options (test pattern output setup for example).

Complete schematic diagram of ADCdual01A module board is included in the appendix.

■ 2.4.6 ADC modules interface

Both of the ADCdual01A modules were connected to FPGA ML605 board trough FMC2DIFF01A adapter board. The design of this adapter expects the presence of FMC LPC connector on host side and the board is, at the same time, not compatible with MLAB. It is, on the other hand, designed to meet the VITA 57 standard specifications for boards which support region 1 and region 3. VITA 57 regions are explained in the picture 2.7. This industry standard guarantees the compatibility with other FPGA boards that have FMC LPC connectors for Mezzanine Card. Schematic diagram of designed adapter board is included in the appendix.

The primary purpose of the PCB is to enable the connection of ADC modules located outside the PC case with ML605 development board. (In PC box analog circuits cannot be realized without the use of massive RFI mitigation techniques). Differential signalling connectors should be used for conducting digital signal over relatively long cables. The signal integrity sensitive links (clocks) are equipped with output driver and translator to LVPECL logic for better signal transmission quality.
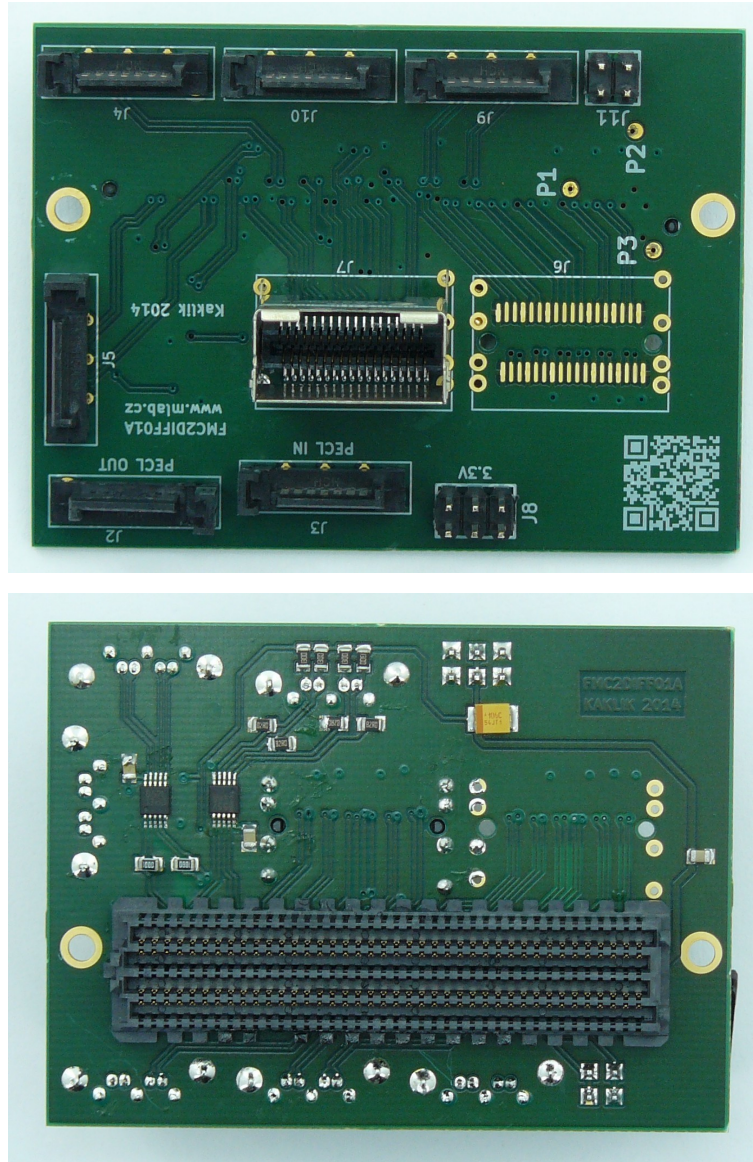
Figure 2.5. Realised PCB of FMC2DIFF01A module.

LVPECL level signal connectors on FMC2DIFF01A board are dedicated to transmit the clock signals. We have selected the SY55855V and SY55857L dual translators. Dual configuration in useful due to fact, that SATA cable contains two differential pairs.

The SY55855V is a fully differential, CML/PECL/LVPECL-to-LVDS translator. It achieves LVDS signalling up to 1.5Gbps, depending on the distance and the characteristics of the media and noise coupling sources. LVDS is intended to drive 50 Ω impedance transmission line media such as PCB traces, backplanes, or cables. SY55855V inputs can be terminated with a single resistor between the true and the complement pins of a given input [14].

The SY55857L is a fully differential, high-speed dual translator optimized to accept any logic standard from single-ended TTL/CMOS to differential LVDS, HSTL, or CML and translate it to LVPECL. Translation is guaranteed for speeds up to 2.5Gbps (2.5GHz toggle frequency). The SY55857L does not internally terminate its inputs, as different interfacing standards have different termination requirements[15].

Inputs of both used chips are terminated accordingly to used logic. The LVDS input is terminated differentially by 100 Ω resistor between positive and negative inputs. PECL input is terminated by Thevenin resistor network. Thevenin termination method was selected as optimal one, due to the absence of a proper power voltage (1,3 V) for direct termination by 50 Ω resistors. Termination on FPGA side is realized directly by settings the proper digital logic type on input pins.
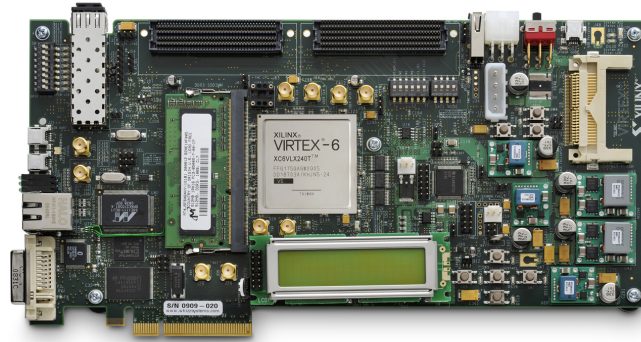
Figure 2.6. FPGA ML605 development board.
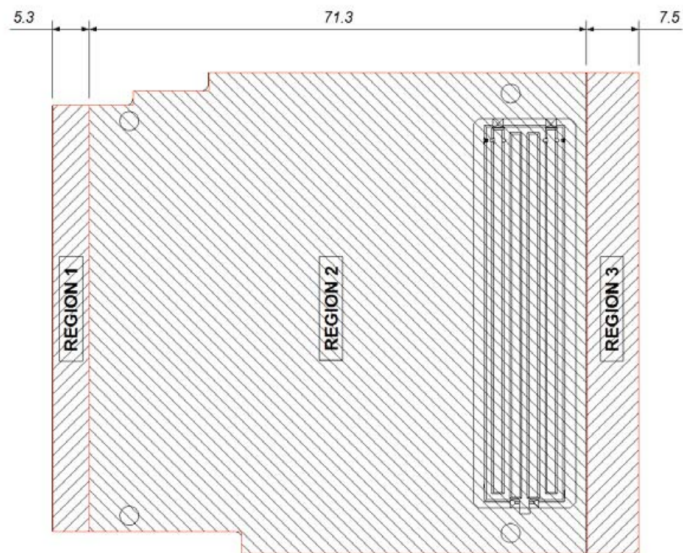
Figure 2.7. Definition of VITA57 regions.

Three differential logic input/output, one PECL input and one PECL output SATA connectors and two miniSAS connectors are populated on this board. This set of connectors allows a connection of any number of ADC modules within the range of 1 to 8. ADC data outputs should be connected to the miniSAS connectors, while other supporting signals should be routed directly to SATA connectors on adapter.

Lengths of differential pairs routed on PCB of the module are not matched between the pairs. Length variation of differential pairs is not critical in our design according to facts discussed in paragraph 2.4.4. Nevertheless, signals within differential pairs themselves are matched for length. Internal signal trace length matching of differential pairs is mandatory in order to minimize jitter and avoid a dynamic logic hazard conditions on digital signals, that represents the worst scenario. Thus the clocks' signals are routed in the most precise way on all designed boards.

Signal configuration used in our trial design is described in the following tables 2.3, 2.4 and 2.5.

miniSAS	SATA pair	FMC signal	Used as
P0	1	LA03	not used
P0	2	LA04	not used
P1	1	LA08	not used
P1	2	LA07	not used
P2	1	LA16	ADC1 CH1 (LTC2190)
P2	2	LA11	ADC1 CH2 (LTC2190)
P3	1	LA17	ADC2 CH1 (LTC2271)
P3	2	LA15	ADC2 CH2 (LTC2271)

Table 2.3. miniSAS (FMC2DIFF01A J7) signal connections between modules.

SPI connection J7	FMC signal	Connected to
SAS-AUX1	LA14_N	SPI DOUT
SAS-AUX2	LA14_P	SPI CLK
SAS-AUX3	LA12_N	CE ADC1
SAS-AUX4	LA12_P	CE ADC2
SAS-AUX5	LA13_N	soldered to GND
SAS-AUX6	LA13_P	not used
SAS-AUX7	LA09_N	not used
SAS-AUX8	LA09_P	soldered to GND

Table 2.4. SPI system interconnections

SPI interface is used in an unusual way in this design. SPI Data outputs from ADCs are not connected anywhere and read back is not possible, thus the configuration written to registers in ADC module cannot be validated. We have not observed any problems with this system, but it may be a possible source of failures.

Signal	FMC signal	FMC2DIFF01A	ADCdual01A
DCO	CLK1_M2C	J5-1	J13-1
FR	LA18_CC	J10-1	J12-1
ENC	LA01_CC	J2-1(PECL OUT)	J3-1
SDGPSDO01A LO	CLK0_M2C	J3-1 (PECL IN)	N/A

Table 2.5. Clock system interconnections

■ 2.4.7 FPGA function

Several tasks in separate FPGA blocks are performed by FPGA. In the first block the FPGA prepares a sampling clock for ADCdual01A modules by dividing the signal from

the main local oscillator. This task represents a separate block in FPGA and runs asynchronously to other logical circuits. Second block is a SPI configuration module, which sends configuration words to ADC modules and it is activated by opening of Xillybus interface file. Third block represents the main module, which resolves ADC - PC communication itself and it communicates via PCIe, collect data from ADC hardware and creates data packet 2.6. Last block is activated after the ADC is configured via SPI.

Communication over PCIe is managed by proprietary IP Core and Xillybus driver, which transfers data from FPGA registers to host PC. Data appear in a system device file named `/dev/xillybus_data2_r` on the host computer. Binary data which appear in this file after its opening are shown in the table below 2.6.

160bit packet								
Data name	FRAME	ADC1 CH1		ADC1 CH2		ADC2 CH1		ADC2 CH2
Data type	uint32	int16	int16	int16	int16	int16	int16	int16	int16
Content	saw signal	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}	$t1$	t_{1+1}

Table 2.6. System device `/dev/xillybus_data2_r` data format

Data packet block which is carried on PCI Express isa described in the table 2.6. The data packet consist of several 32bit words. The first word contains FRAME number and it is filled with saw signal for now, with incremental step taking place every data packet transmission. The following data words contain samples from ADCs' first and second channel. Samples from every channel are transmitted in pairs of two samples. Number of ADC channels is expandable according to the number of physically connected channels. An CRC word may possibly be added in the future to the end of the transmission packet for data integrity validation.

FRAME word at the beginning of data packet, now filled with incrementing and overflowing saw signal, is used to ensure that no data samples ale lost during the data transfers from FPGA. FRAME signal may be used in the future for pairing the ADC samples' data packet with another data packet. This new additional data packet should carry meta-data information about the sample time jitter, current accuracy of the local oscillator frequency etc.

Detailed description of the currently implemented FPGA functions can be found in a separate paper [16]. HDL source codes for FPGA at a state in which it was used are included on the enclosed CD. More recent development versions are publicly available from MLAB sources repository. Detailed description of currently implemented FPGA functions can be found in separate paper [16]. HDL source codes for FPGA at state which was used are included on enclosed CD. Future development versions are publicly available from MLAB sources repository [17].

■ 2.4.8 Data reading and recording

In order to read the data stream from the ADC drive, we use Gnuradio software. Gnuradio suite consists of gnuradio-companion package which is a graphical tool for creating signal-flow graphs and generating Python flow-graph source code. This tool has been used to create a basic RAW data grabber to record and interactively view waterfall plots using the data streams output from ADC modules.

The interactive grabber-viewer user interface shows live oscilloscope-like time-value display for all data channels and live time-frequency scrolling display (a waterfall view)
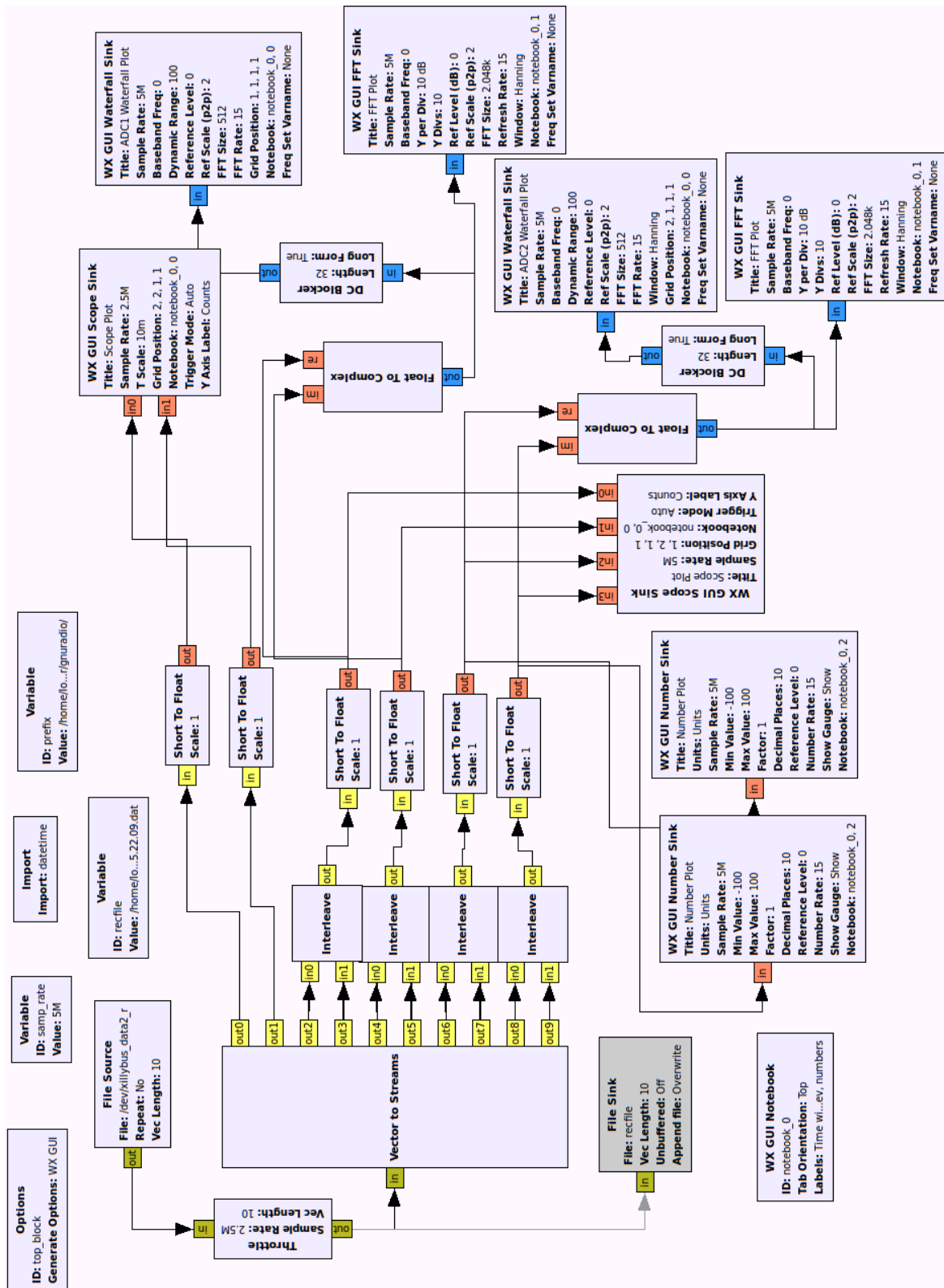
Figure 2.8. The ADC recorder flow graph created in gnuradio-companion.

for displaying the frequency components of the grabbed signal. Signal is grabbed to file with exactly the same format, as described in the table 2.6.
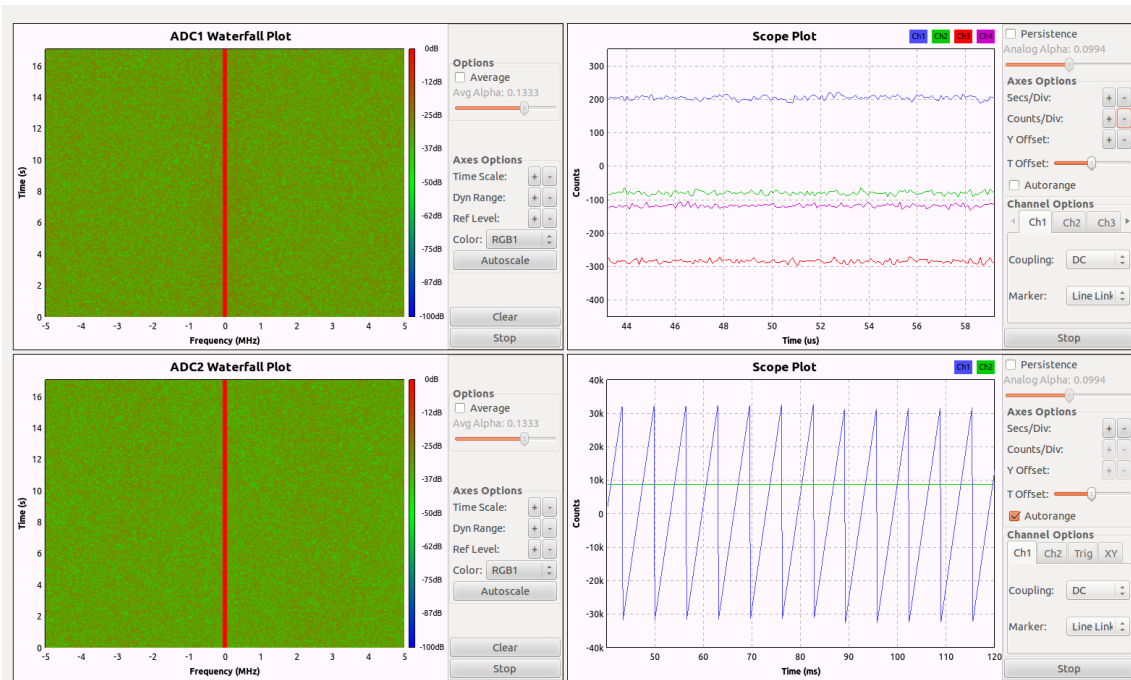
18

Figure 2.9. User interface window of a running ADC grabber.

19

Chapter 3
Achieved parameters

The trial version construction was tested for proper handling of sampling rates in the range of 5 MSPS to 15 MSPS, but it should work above this limit. System works on i7 8 cores computer with Ubuntu 12.04 LTS operating system. Data recording of input signal is impossible above the sampling rates around 7 MSPS due to bottleneck at HDD speed limits, but it should be resolved by the use of SSD disk drive. However, such design has not been tested in our setup.

3.1 Measured parameters

Two prototypes of ADC modules were assembled and tested. The first prototype, labeled ADC1, has LTC2190 ADC chip populated with LT6600-5 front-end operational amplifier. It also has a 1kOhm resistors populated on inputs which give it an ability of an internal attenuation of the input signal. The value of this attenuation A is calculated by the following formula (1)

$$A = \frac{806 \cdot R_1}{R_1 + R_2} \tag{1}$$

Where the letters stand for the following:

- A - Gain of an input amplifier.
- R_1 - Output impedance of signal source (usually 50 Ohm).
- R_2 - Value of serial resistors at operational amplifier inputs.

We have $R_2 = 1000\Omega$ and $R_1 = 50\Omega$ which imply that $A = 0.815$. That value of A was further confirmed by the measurement. In our measurement setup we have H1012 Ethernet transformer connected to inputs of ADC. We have used this transformer for signal symetrization from BNC connector at Agilent 33220A signal generator. Circuit diagram of the used transformer circuit is shown in picture 3.1 and circuit realization in photograph 3.4.

The signal generator Agilent 33220A which we used, does not have optimal parameters for this type of dynamic range measurement. Signal distortion and spurious levels are only -70 dBc according to Agilent datasheet [18]. We have managed to measure an ADC saturation voltage of 705.7 mV (generator output) with this setup, mostly due to an impedance mismatch and uncalibrated measurement setup, with 1V ADC range selected by sense pin. This is a relatively large error, but the main result of our measurement, seen as a FFT plot shown in image 3.2, confirms >80 dB dynamic range at ADC module input.

Similar test was performed at ADC2 module. For ADC2 we have to use formula with a different constant (1). The ADC2 module has LT6600-2.5 amplifiers populated on it with a gain equal to $A = 2.457$ and uses the same R_2 resistors. We measured saturation voltage of 380 mV (generator output) at channel 1 on this ADC. It is well within the parameter tolerances of the used setup.
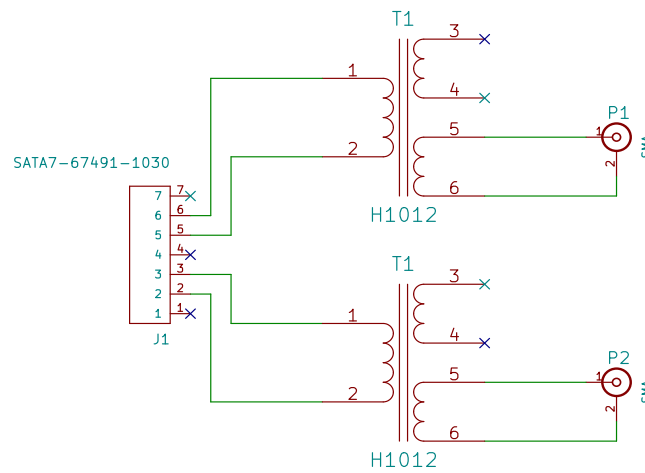
Figure 3.1. Simplified balun transformer circuit diagram.
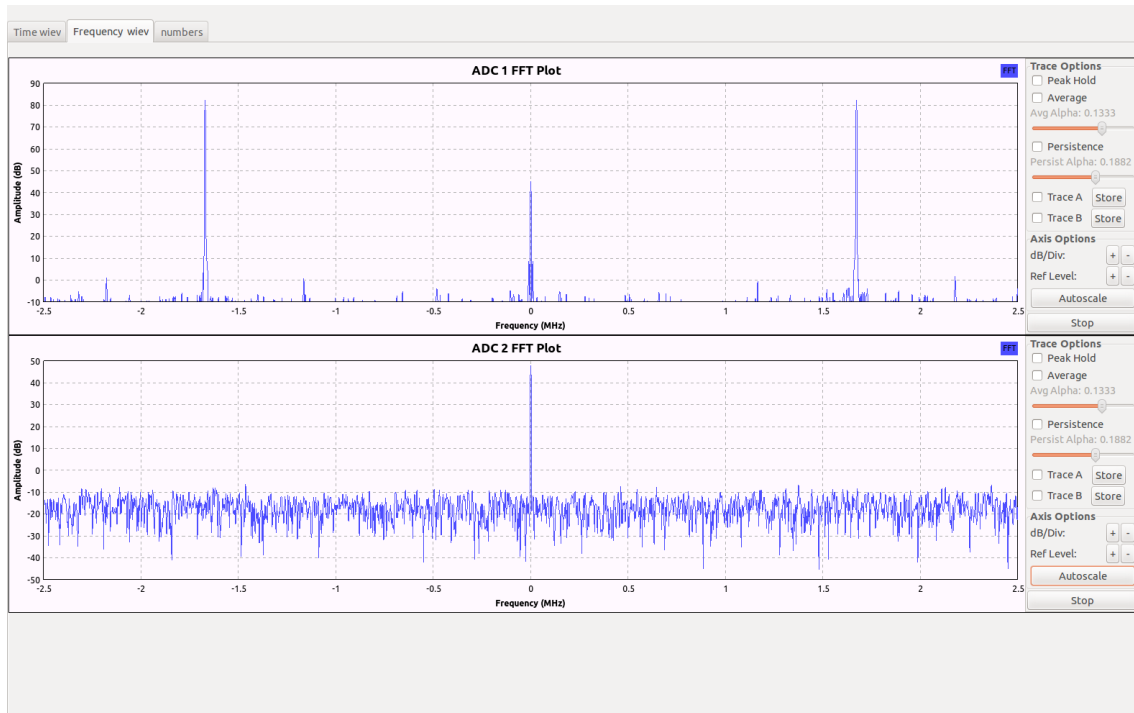
Figure 3.2. Sine signal sampled by ADC1 module with LTC2190 and LT6600-5 devices.

$$A = \frac{1580 \cdot R_1}{R_1 + R_2} \tag{2}$$

Where the letters stand for the following:

- A - Gain of an input amplifier.
- R_1 - Output impedance of signal source (usually 50 Ohm).
- R_2 - Value of serial resistors at operational amplifier inputs.
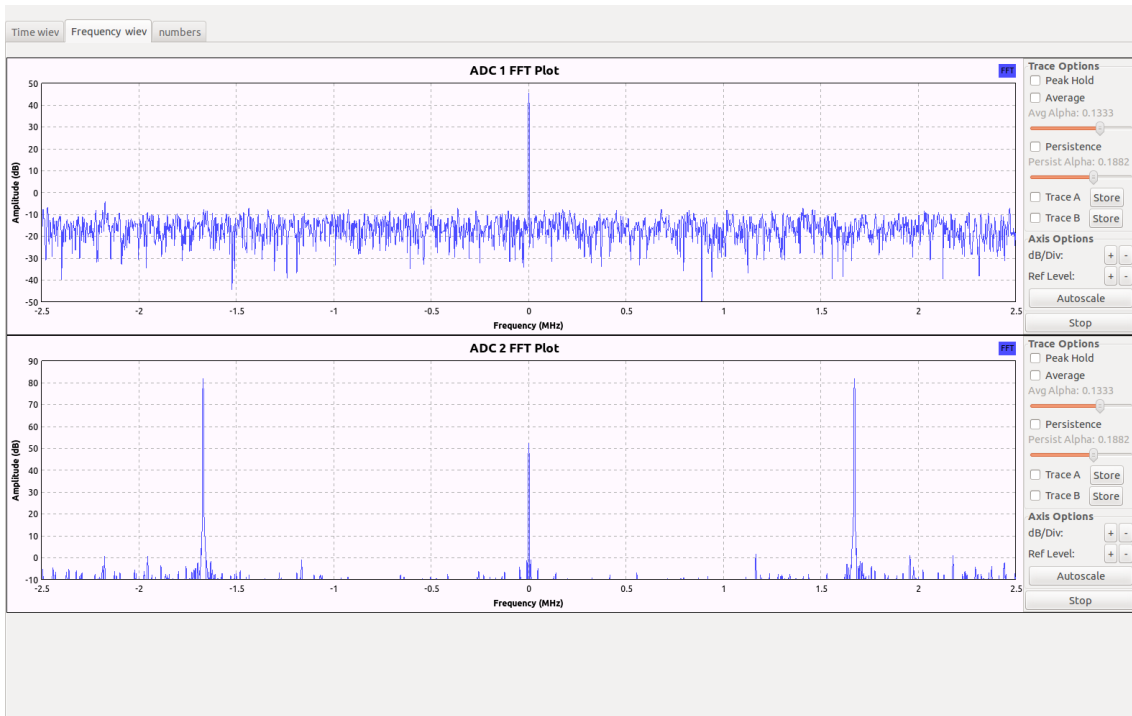
Figure 3.3. Sine signal sampled by ADC2 module with LTC2271 and LT6600-2.5 devices.
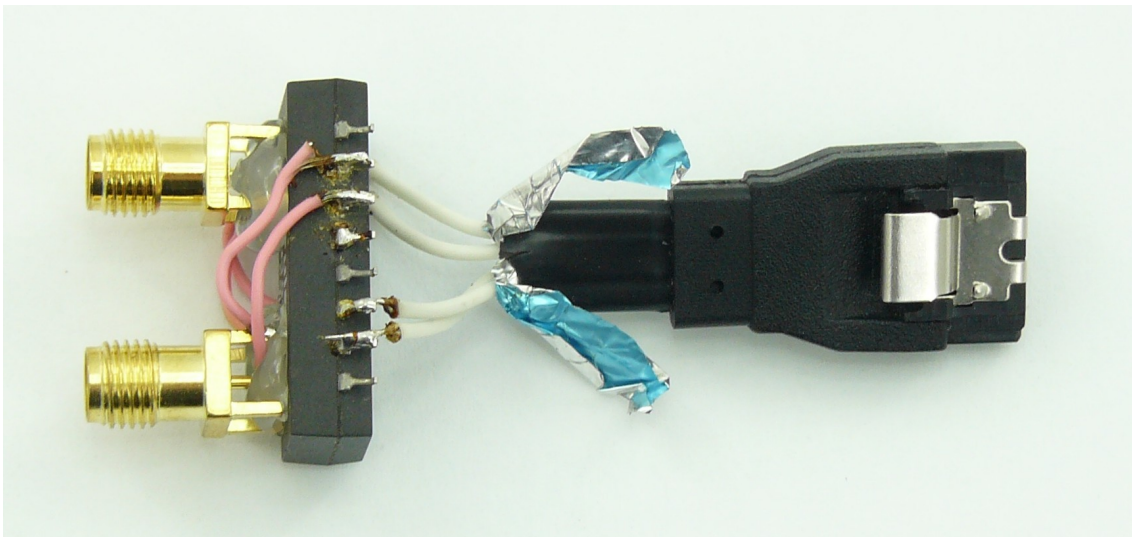
Figure 3.4. Balun transformer circuit used for ADC parameters measurement. It is constructed from H1012 transformer salvaged from an old Ethernet card.

Computed FFT spectra for measured signal are shown in the images 3.3 and 3.2. Both images confirm that ADCdual01A modules have input dynamical range of at least 80 dB.

▌ **3.2 Example of usage**

At current state the constructed radioastronomy digitization unit paired with SDRX01B receiver module could be used in several experiments. We describe overall ideas of these experiments and show preliminary results in cases where we obtain the data.

■ 3.2.1 Simple polarimeter station

If we use two antennas with different linear polarization (Crossed Yagi antennas for example), we should determine polarization state of received signal. Such kind of measurement is useful if we need an additional information about reflection to distinguish between targets. This configuration needs more complicated antenna configuration and we had no experience with this type of observation, so we have not implemented this experiment.

■ 3.2.2 Basic interferometric station

Interferometry station was chosen to serve as the most basic experimental setup. We connected the new data acquisition system to two SDRX01B receivers. Block schematics of the setup used is shown in the image 3.5. Two ground-plane antennae were used and mounted outside the balcony at CTU building at location 50° 4' 36.102" N, 14° 25' 4.170" E. Antennae were equipped with LNA01A amplifiers. All coaxial cables had the same length of 5 meters. Antennae were isolated by common mode ferrite bead mounted on cable to minimise the signal coupling between antennas. Evaluation system consisted of SDGPSDO local oscillator subsystem used to tune the local oscillator frequency.

Despite of the schematic diagram proposed at beginning of system description 2.1. We have used two separate oscillators – one oscillator drives ENC signal to ADCs still through FPGA based divider and the other one drives it to SDRX01B mixer. The reason for this modification was an attempt to simplify the frequency tuning during the experiment. A single oscillator may be used only with a proper setting of FPGA divider and this divider may be modified only by recompilation of FPGA code and loading/flashing a new FPGA schema. Due to fact that the FPGA is connected to PCI express and kernel drivers with hardware must be reinitialized, reboot of PC is required every time a FPGA scheme is changed. Instead of this complicated procedure, we set the FPGA divider to a constant division factor of 30 and used another district oscillator for ADCdual01 sampling modules and for SDRX01B receiver. We have used ACOUNT02A MLAB instrument for frequency checking of correct setup on both local oscillators.

For the simplest demonstration of phase difference between antennae, we have analysed part of the signal by complex conjugate multiplication between channels. Results of this analysis can be seen in the following picture 3.6. Points of the selected part of the signal create a clear vector, which illustrates the presence of the constant phase difference determined by RF source direction.

■ 3.2.3 Simple passive Doppler radar

If we use an existing transmitter with known carrier frequency and proper antenna, we can detect flying object as signals surrounding the transmitter carrier frequency. We planned this experiment with the same station configuration as was described in section 2.1. The ISS as object and GRAVES radar transmitter were selected as adequate testing objects (We know ISS reflections from previous experiments). This experiment could be realised by previously described interferometer station, but unfortunately we missed the suitable orbit pass due to technical lacks with station configuration.

■ 3.2.4 Meteor detection station
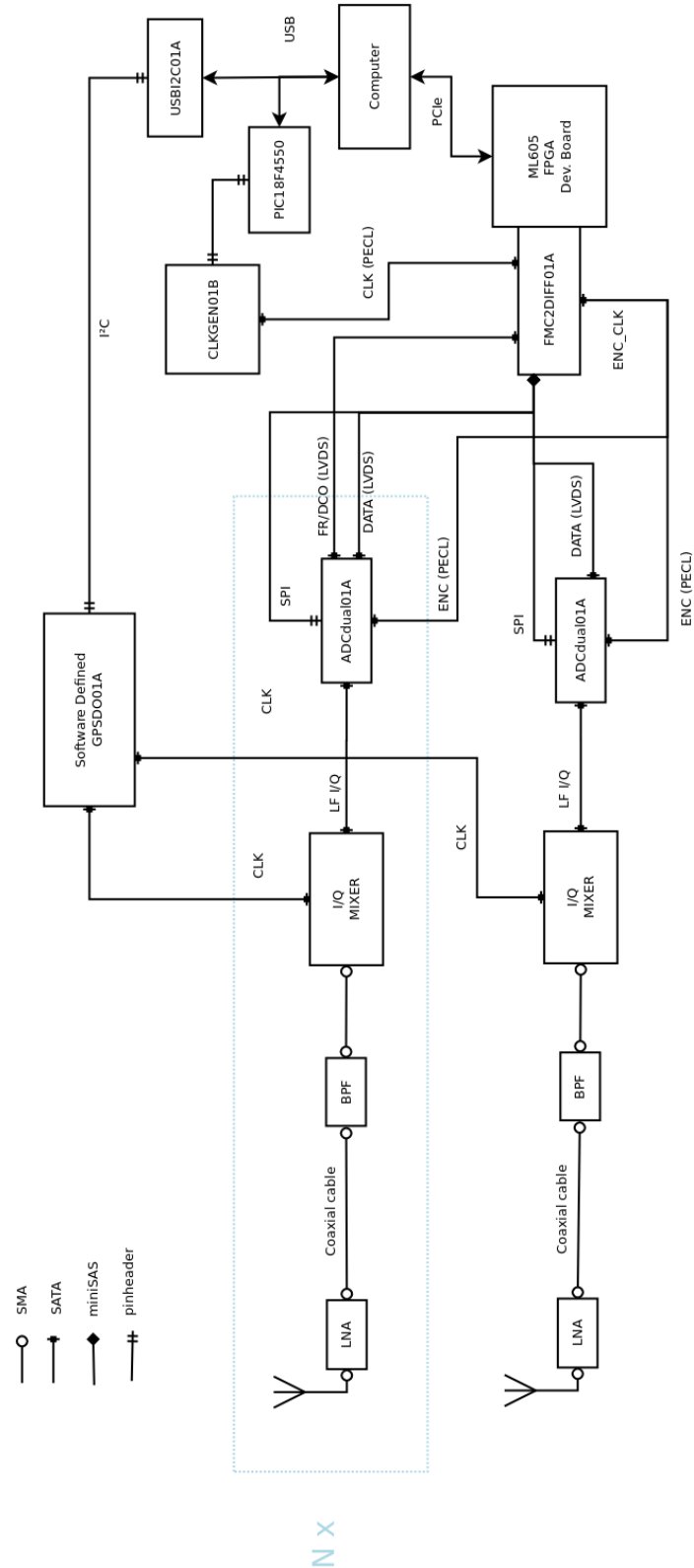
Figure 3.5. Complete receiver block schematic of dual antenna interferometric station.

The same observational station configuration should be used for meteor detection system [19]. We used the GRAVES radar as suitable signal source and monitored its carrier frequency. GRAVES radar is located in France therefore we could not see its
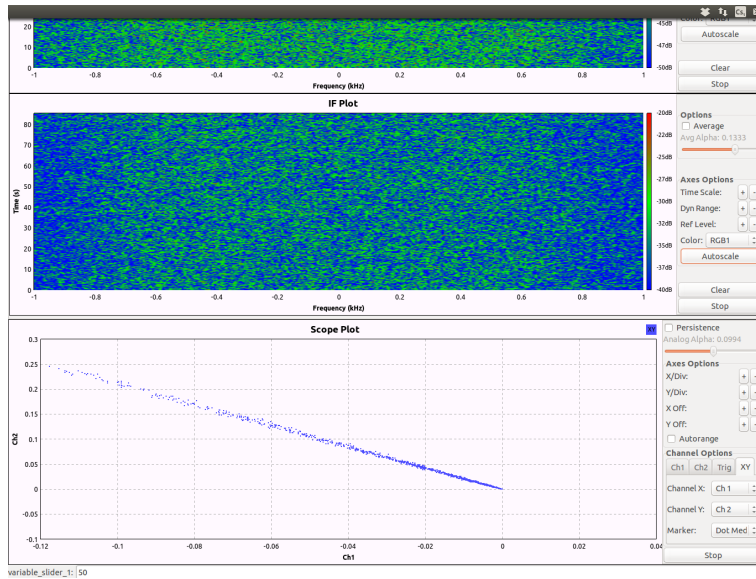
Figure 3.6. Demonstration of phase difference between antennae.

direct carrier signal, but meteors reflect it signal and as consequence we could easily detect meteor presence as reflection appearance. One meteor detected by this method is shown in picture 3.7.
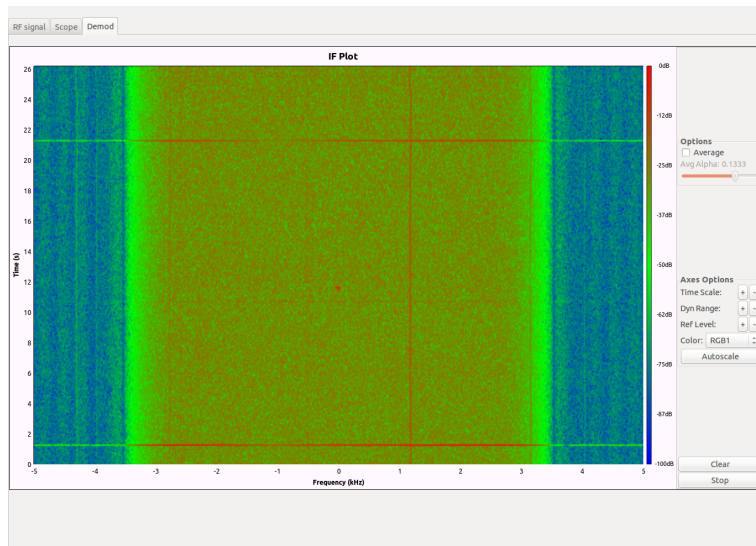
Figure 3.7. Meteor reflection (the red spot in centre of image) received by an evaluation design.

25

Chapter 4
Proposition of the final system

The construction of the final system, that is supposed to be employed for real radioastronomy observations will be described in this chapter. It is mainly a theoretical analysis of the data handling systems. Realization of the described ideas might be possible as a part of our future development after we fully evaluate and test the current trial design.

The system requires proper handling of huge amounts of data and either huge and fast storage capacity is needed to store the captured signal data, or enormous computational power is required for online data processing and filtering. Several hardware approaches currently exist and are in use for data processing problem handling. Either powerful multi gigahertz CPUs, GPUs, FPGAs, or specially constructed ASICs are used for this task.

4.1 Custom design of FPGA board

In the beginning of the project, a custom design of FPGA interface board had been considered. This FPGA board should include PCI express interface and should sell at lower price than the trial design. It should be compatible with MLAB internal standards which are further backward compatible with the existing or improved design of ADC modules. For a connection of FPGA board to another adapter board with PCIe we expect a use of a PCIe host interface. Thunderbolt technology standard was expected to be used in this PC to PCIe module communication which further communicates with MLAB compatible FPGA module. Thunderbolt chips are currently available on the market for reasonable prices [20]. However, a problem lies in the accessibility to their specifications, as they are only available for licensed users and Intel has a mass market oriented licensing policy, that makes this technology inaccessible for low quantity production. As a consequence, an external PCI Express cabling and expansion slots should be considered as a better solution, if we need to preserve standard PC as a main computational platform.

However, these PCI express external systems and cables are still very expensive. Take Opal Kelly XEM6110 [21] as an example, with its price tag reaching 995 USD at time of writing the thesis. Therefore, a better solution probably needs to be found.

An interface problem will by probably resolved by other than Intel ix86 architecture. Many ARM computers have risen on market due to an increased demand of embedded technologies, which require high computation capacity, low power consumption and small size – especially smartphones. Many of those ARM based systems have interesting parameters of signal processing. These facts make Intel's ix86 architecture unattractive for future projects.

4.2 Parralella board computer

Parallella is a new product created by Adapteva, Inc. [22]. It represents a small supercomputer, that has been in development for almost two years with only testing

series of boards produced until now (first single-board computers with 16-core Epiphany chip were shipped in December 2013) [22]. The board has nearly ideal parameters for signal processing (as it provides around 50 GFLOPS of computational power). It is is equipped with Epiphany coprocessor which has 16 High Performance RISC CPU Cores, Zynq-7020 FPGA with Dual ARM® Cortex™-A9 MPCore™ and operating frequency of 866 MHz, 1GB RAM, 85K Logic Cells, 10/100/1000 Ethernet and OpenCL support [23]. In addition to this, the board consumes only 3 Watts of power if both Zynq and Epiphany cores are running simultaneously.

The main disadvantage of Parralella board is its unknown lead time and an absence of SATA interface or other interface suitable for data storage connection. Fast data storage interface would be useful and would allow bulk processing of captured data. Following that, the results of data processing may be sent over the Ethernet interface to data storage server.
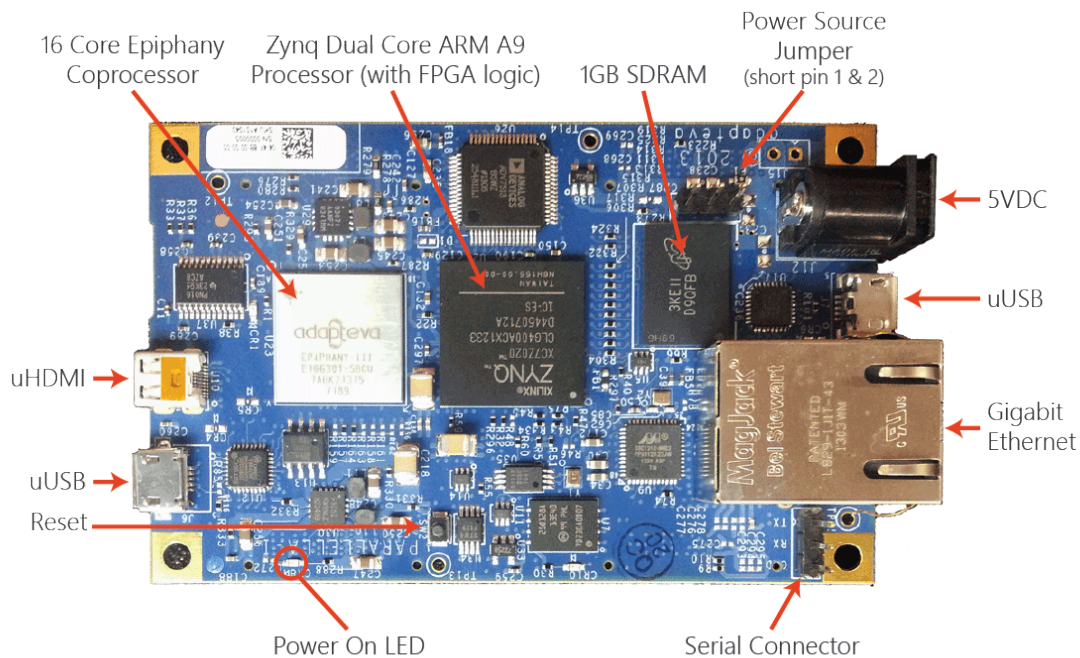
Figure 4.1. Top view on Parallella-16 board [23].

If Parallella board will be used as a radioastronomy data interface, there would be a demand for new ADC interface module. The interface module will use four PEC connectors mounted on the bottom of the Parallella board. This daughter module should have MLAB compatible design and should preferably be constructed in the form of separable modules for every Parallella's PEC connector.

4.3　GPU based computational system

A new GPU development board NVIDIA K1, shown in the following picture 4.2, has recently been released. These boards are intended to be used in fields including computer vision, robotics, medicine, security or automotive industry. They have good parameters for signal processing for a relatively low price of 192 USD. Unfortunately, they are currently only in pre-order release stage (in April 2014).
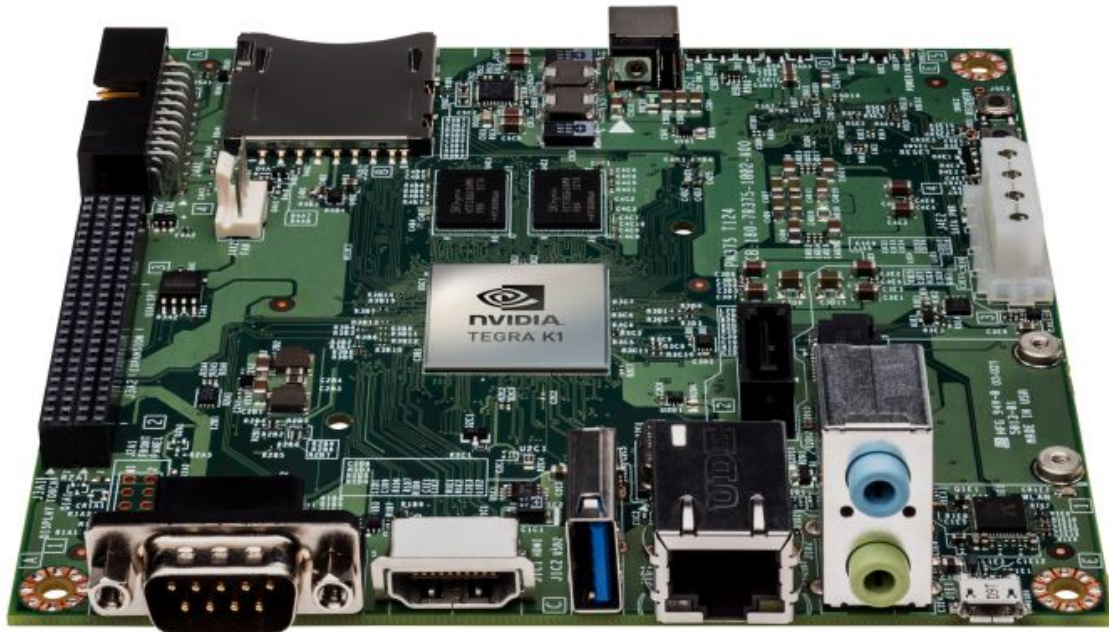
Figure 4.2. The NVIDIA Jetson TK1 Development Kit [24].

NVIDIA board differs from other boards in its category by a presence of PCI Experess connector. If we decide to use this development board in our radio astronomy digitalisation system, the PCI express should be used for FPGA connection. A new FPGA board with PCI Express direct PCB connector

4.4 Other ARM based computation systems

Other embedded ARM based computers, for example ODROID-XU, lack a suitable high speed interface. Their highest speed interface is USB 3.0 which has currently unsettled development support and needs commercial software tools for evaluation and testing.

From the summary analysis mentioned above, the Parrallella board seems to be a best candidate for computational board in radioastronomy data acquisition system, as it is optimised for high data flow processing. On one hand, Parrallella does not have much memory to cache the processing data but on the other hand it has wide bandwidth data channels instead. Other boards might provide much more computational power – 300 GFLOPS in case of NVIDIA K1, but they are optimised for heavy computational tasks on limited amount of data which represents a typical problem in computer graphics. However, in our application we do not need such extreme computation power at data acquisition system level. As a result we should presumably wait until Parallella becomes widely available. Following that, a new ADCdual interface board should be designed and prepared to be used in new scalable radio astronomy data acquisition system. In the meantime, before suitable computing hardware become accessible, the required applications and algorithms should be optimised using the proposed trial version with FPGA development board on standard PC host computer (having a PCI Express interface to development board).

Chapter 5
Conclusion

A special design of scalable data-acquisition system was proposed. This system has unique parameters compared to the state of the art radioastronomy signal processing hardware. Offering a 16bit resolution and comparable dynamical range is more than other similar constructions could offer. We demonstrated system functionality on the most basic interferometric station. Further validation of reached parameters would be necessary. Following that, the final design will eventually become a part of MLAB Advanced Radio Astronomy System[25].

All requirements demanded by the thesis specification have been reached or exceed. The required minimal sampling frequency of 1 MHz has been exceeded five times at least. Requested dynamical range specified by 12 bit have been exceeded at least by 8 dB in decibel scale. As by-pass product of digitalisation unit design the software defined GPS disciplined oscillator device has been developed. This device is currently in use on several radio meteor detection stations in Czech Republic. On other hand the proposed design is not still perfect and some minor imperfections should be corrected in future work.

5.1   Possible hardware improvements

The PCB design of the used modules might need more precise high-speed optimization of differential pairs. Improvement in high-speed routing allows a possible use of the fastest ADC from the Linear Technology devices family. The use of the faster ADCs even improves a range of possible usages. Minor ADC module imperfections, such as the unnecessary separation of FRAME and DCO signal to two connectors, should be mitigated. These two signals should be merged together to one SATA connector. With this modification we will be able to remove one redundant SATA cable between the analog to digital converter device and computational unit section.

5.2   Possible software improvements

In the future versions of the system hardware, the Xillybus IP core and driver interface should be swapped with an open-source alternative of PCIe interfacing module or PCIe might be completely avoided. In ADC configuration FPGA module, the SPI configuration data registers read back should be implemented.

Glossary

ADC – analog-to-digital converter
ALFA – Arecibo L-Band Feed Array
ATA – AT Attachment
CASPER – Collaboration for Astronomy Signal Processing and Electronics Research
CMOS – Complementary metal–oxide–semiconductor
DCO – Data Clock Output
EMI – Electromagnetic interference
FPGA – Field-programmable gate array
GPS – Global Positioning System
GPSDO – GPS disciplined oscillator
HBA – High Band Antenna
HDD – Hard disk drive
HDL – Hardware description language
IP3 – Third-order intercept point
ISS – International Space Station
LBA – Low Band Antenna
LOFAR – Low-Frequency Array
LVDS – Low-voltage differential signaling
LVPECL – Low Voltage Emitter-coupled logic
MSPS – Mega-Samples Per Second
NASA – National Aeronautics and Space Administration
PCB – printed circuit board
PCI Express – Peripheral Component Interconnect Express
PVC – Polyvinyl chloride
RF – Radio frequency
ROACH – Reconfigurable Open Architecture Computing Hardware (ROACH) board
SATA – Serial ATA
TV – Television
USB 2.0 – Universal Serial Bus version 2.0
USRP – Universal Software Radio Peripheral
WWII – Second World War

References

[1] UKARANet. Radio astronomy frequency allocations, May 2014.
http://www.ukaranet.org.uk/basics/frequency_allocation.htm.

[2] Kortánek Jiří. Radioteleskop jove, přijímač ruchů z jupiterových radiových bouří, bakalářská práce 000672041, September 2007.

[3] Microsoft. Microsoft spectrum observatory, 2012.
http://observatory.microsoftspectrum.com/.

[4] A. W. Gunst G. Heald J. P. McKean J. W. T. Hessels A. G. de Bruyn R. Nijboer J. Swinbank R. Fallows M. Brentjens A. Nelles R. Beck H. Falcke R. Fender J. Hörandel L. V. E. Koopmans G. Mann G. Miley H. Röttgering B. W. Stappers R. A. M. J. Wijers S. Zaroubi M. van den Akker A. Alexov J. Anderson K. Anderson A. van Ardenne M. Arts A. Asgekar I. M. Avruch F. Batejat L. Bähren M. E. Bell M. R. Bell I. van Bemmel P. Bennema M. J. Bentum G. Bernardi P. Best L. B■rzan A. Bonafede A.-J. Boonstra R. Braun J. Bregman F. Breitling R. H. van de Brink J. Broderick P. C. Broekema W. N. Brouw M. Brüggen H. R. Butcher W. van Cappellen B. Ciardi T. Coenen J. Conway A. Coolen A. Corstanje S. Damstra O. Davies A. T. Deller R.-J. Dettmar G. van Diepen K. Dijkstra P. Donker A. Doorduin J. Dromer M. Drost A. van Duin J. Eislöffel J. van Enst C. Ferrari W. Frieswijk H. Gankema M. A. Garrett F. de Gasperin M. Gerbers E. de Geus J.-M. Griemeier T. Grit P. Gruppen J. P. Hamaker T. Hassall M. Hoeft H. Holties A. Horneffer A. van der Horst A. van Houwelingen A. Huijgen M. Iacobelli H. Intema N. Jackson V. Jelic A. de Jong E. Juette D. Kant A. Karastergiou A. Koers H. Kollen V. I. Kondratiev E. Kooistra Y. Koopman A. Koster M. Kuniyoshi M. Kramer G. Kuper P. Lambropoulos C. Law J. van Leeuwen J. Lemaitre M. Loose P. Maat G. Macario S. Markoff J. Masters D. McKay-Bukowski H. Meijering H. Meulman M. Mevius E. Middelberg R. Millenaar J. C. A. Miller-Jones R. N. Mohan J. D. Mol J. Morawietz R. Morganti D. D. Mulcahy E. Mulder H. Munk L. Nieuwenhuis R. van Nieuwpoort J. E. Noordam M. Norden A. Noutsos A. R. Offringa H. Olofsson A. Omar E. Orrú R. Overeem H. Paas M. Pandey-Pommier V. N. Pandey R. Pizzo A. Polatidis D. Rafferty S. Rawlings W. Reich J.-P. de Reijer J. Reitsma A. Renting P. Riemers E. Rol J. W. Romein J. Roosjen M. Ruiter A. Scaife K. van der Schaaf B. Scheers P. Schellart A. Schoenmakers G. Schoonderbeek M. Serylak A. Shulevski J. Sluman O. Smirnov C. Sobey H. Spreeuw M. Steinmetz C. G. M. Sterks H.-J. Stiepel K. Stuurwold M. Tagger Y. Tang C. Tasse I. Thomas S. Thoudam M. C. Toribio B. van der Tol O. Usov M. van Veelen A.-J. van der Veen S. ter Veen J. P. W. Verbiest R. Vermeulen N. Vermaas C. Vocks C. Vogt M. de Vos E. van der Wal R. van Weeren H. Weggemans P. Weltevrede S. White S. J. Wijnholds T. Wilhelmsson O. Wucknitz S. Yatawatta P. Zarka A. Zensus J. van Zwieten M. P. van Haarlem, M. W. Wise. *LOFAR: The LOw-Frequency ARray*, May 2013.
http://arxiv.org/abs/1305.3550.

[5] Astron. Design and development, May 2014.
http://www.astron.nl/other/desp/competences_DesApp.htm.

[6] Univeristy of California Berkeley. Center for astronomy signal processing and electronics research, May 2014.
https://casper.berkeley.edu/.

[7] Univeristy of California Berkeley. A new approach to radioastronomy signal processing, May 2014.
https://casper.berkeley.edu/papers/200509URSI.pdf.

[8] Digikey. 6367550-5-nd, May 2014.
http://www.digikey.com/product-detail/en/6367550-5/6367550-5-ND/2259130.

[9] Fringe Dwellers. Simple interferometer, May 2004.
http://fringes.org/.

[10] Pieter-Tjerk de Boer. Pa3fwm's software defined radio page, April 2013.
http://wwwhome.cs.utwente.nl/~ptdeboer/ham/sdr/.

[11] M. Kakona J. Kakona. Software defined gps disciplined oscillator - gpsdo01a, January 2014.
http://wiki.mlab.cz/doku.php?id=en:gpsdo.

[12] Silicon Laboratories. *Si570 datasheet*, January 2014.
http://www.silabs.com/Support%20Documents/TechnicalDocs/si570.pdf.

[13] Robert LeBoeuf. Data converter serial lvds interface improves board routing, snaa110, January 2011.
http://www.ti.com/lit/wp/snaa110/snaa110.pdf.

[14] Inc Micrel. *SY55855V datasheet*, 2005.
http://www.micrel.com/_PDF/HBW/sy55855v.pdf.

[15] Inc Micrel. *SY55857L datasheet*, 2006.
http://www.micrel.com/_PDF/HBW/sy55857l.pdf.

[16] Ondřej Sychrovský. Connecting an fmc with attached a/d converters – middleware for an fpga board, ctu-cmp-2014-5, May 2014.

[17] MLAB. Softwarově definovaný přijímač mlab sdrx, May 2014.
svn://svn.mlab.cz/MLAB/Designs/HAM%20Constructions/SDRX02B.

[18] Inc. Agilent Technologies. *33220A Function / Arbitrary Waveform Generator, 20 MHz*, 2011.
http://www.home.agilent.com/agilent/redirector.jspx?action=obs&nid=536883183.3.00&lc=eng&cc=CZ&ckey=187648&pubno=5988-8544EN&ltype=LitStation&ctype=AGILENT_EDITORIAL&ml=eng.

[19] MLAB. Radio meteor detection station, May 2014.
http://wiki.mlab.cz/doku.php?id=cs:rmds02.

[20] Intel Mouser. Dsl2210, January 2014.
http://cz.mouser.com/search/Refine.aspx?Keyword=106790692&Ns=Pricing|0&FS=True&Ntk=P_MarCom.

[21] Opal Kelly. Opal kelly xem6110, January 2011.
http://www.opalkelly.com/products/xem6110/.

[22] Adapteva. Parallella - supercomputing for everyone, January 2014.
http://www.parallella.org/board/.

[23] Adapteva. Parallella-16, April 2014.
http://shop.adapteva.com/collections/featured-products/products/parallella-▉16.

[24] NVIDIA. The nvidia jetson tk1 development kit, April 2014.
https://developer.nvidia.com/jetson-tk1.

[25] Jakub Kákona MLAB. Pokročilá radioastronomická stanice aras01a, September 2013.

Appendix A
Circuit diagram of ADCdual01A module
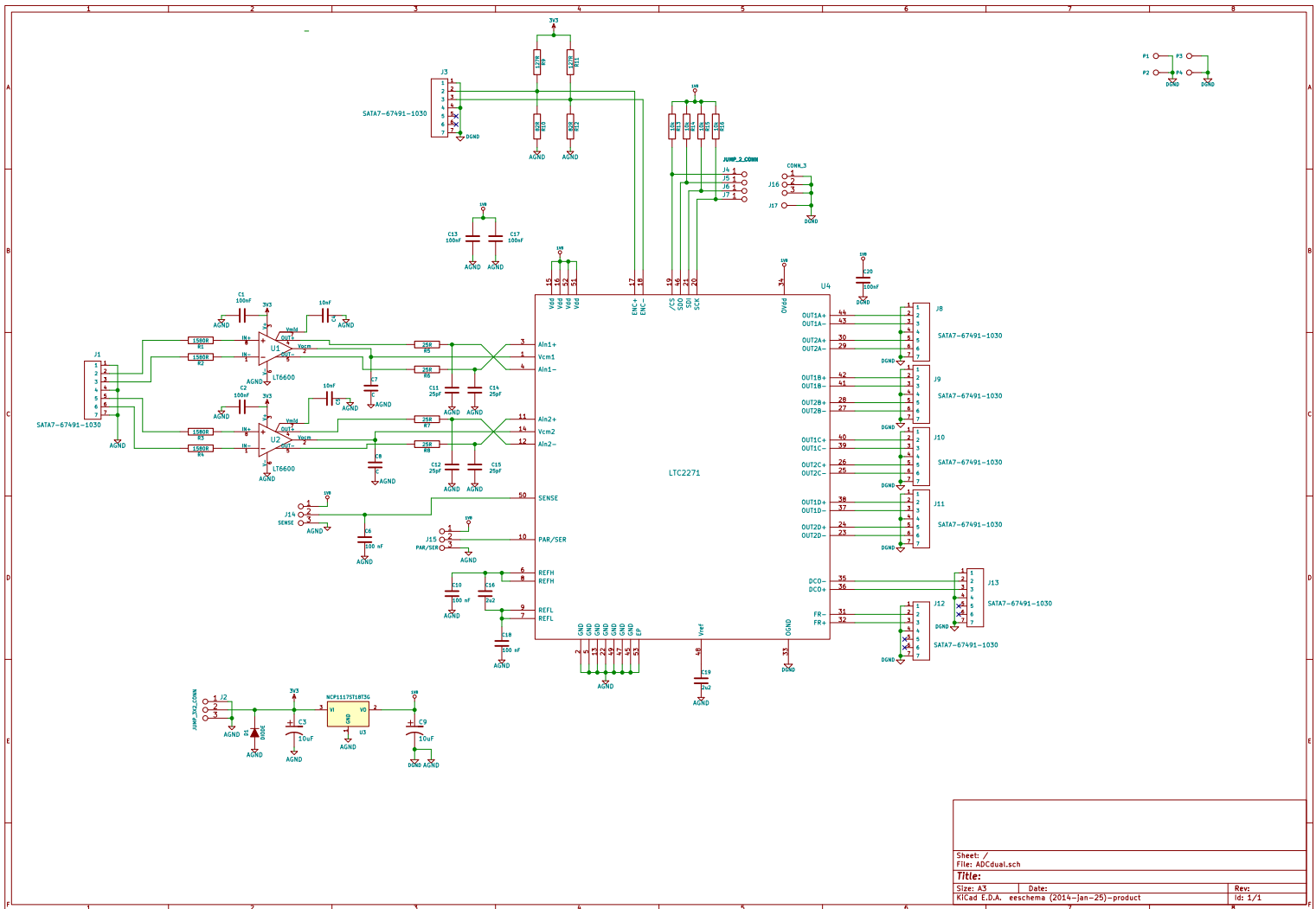
Appendix B
Circuit diagram of FMC2DIFF module

FMC_connector

FMC.sch

SATA_connectors

SATA.sch

miniSAS_connectors

miniSAS.sch

J1A — C Row — ASP-134604-01

C01, C02, C03, C04, C05, C06, C07, C08, C09, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40

DP0_C2M_P
DP0_C2M_N
DP0_M2C_P
DP0_M2C_N
LA06_P
LA06_N
LA10_P
LA10_N
LA14_P
LA14_N
LA18_P_CC
LA18_N_CC
LA27_P
LA27_N
SCL
SDA
+12V
GA0
3V3
DGND

J1B — D Row — ASP-134604-01

D01, D02, D03, D04, D05, D06, D07, D08, D09, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40

PG_C2M
GBTCLK0_M2C_P
GBTCLK0_M2C_N
LA01_P_CC
LA01_N_CC
LA05_P
LA05_N
LA09_P
LA09_N
LA13_P
LA13_N
LA17_P_CC
LA17_N_CC
LA23_P
LA23_N
LA26_P
LA26_N
TCK
TDI
TDO
+3.3VP
TMS
TRST_L
GA1
3V3
C4
C
DGND

J1C — G Row — ASP-134604-01

G01, G02, G03, G04, G05, G06, G07, G08, G09, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, G31, G32, G33, G34, G35, G36, G37, G38, G39, G40

CLK1_M2C_P
CLK1_M2C_N
LA00_P_CC
LA00_N_CC
LA03_P
LA03_N
LA08_P
LA08_N
LA12_P
LA12_N
LA16_P
LA16_N
LA20_P
LA20_N
LA22_P
LA22_N
LA25_P
LA25_N
LA29_P
LA29_N
LA31_P
LA31_N
LA33_P
LA33_N
VDD
DGND

J1D — H Row — ASP-134604-01

H01, H02, H03, H04, H05, H06, H07, H08, H09, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H25, H26, H27, H28, H29, H30, H31, H32, H33, H34, H35, H36, H37, H38, H39, H40

VREF_A_M2C
PRSNT_M2C_L
CLK0_M2C_P
CLK0_M2C_N
LA02_P
LA02_N
LA04_P
LA04_N
LA07_P
LA07_N
LA11_P
LA11_N
LA15_P
LA15_N
LA19_P
LA19_N
LA21_P
LA21_N
LA24_P
LA24_N
LA28_P
LA28_N
LA30_P
LA30_N
LA32_P
LA32_N
VDD

J111 — JUMP_2X2_CONN
SDA   1
SCL   2

TRST_L   P1
VDD   P3
+12V   P2

J9

LA23_N
LA23_P
LA26_N
LA26_P
1
2
3
4
5
6
7
DGND
SATA7-67491-1030

J4

LA05_N
LA05_P
LA10_N
LA10_P
1
2
3
4
5
6
7
DGND
SATA7-67491-1030

J10

LA18_N_CC
LA18_P_CC
LA27_N
LA27_P
1
2
3
4
5
6
7
DGND
SATA7-67491-1030

J5

CLK1_M2C_N
CLK1_M2C_P
LA00_N_CC
LA00_P_CC
1
2
3
4
5
6
7
DGND
SATA7-67491-1030

3V3
C2
C
C3
CP1
DGND
DGND

3V3
127R
R3
3V3
127R
R9

3V3
VCC
U2B
D1
/D1
SY55855V
Q1
Q1
GND
DGND

CLK0_M2C_P
CLK0_M2C_N

82R
R4
82R
R10
DGND
DGND

J3
1
2
3
4
5
6
7
DGND
SATA7-67491-1030

3V3
127R
R5
3V3
127R
R7

3V3
VCC
U2A
D0
/D0
SY55855V
Q0
Q0
GND
DGND

LA02_P
LA02_N

82R
R6
82R
R8
DGND
DGND

3V3
C1
C
DGND

3V3
100R
R1
LA01_N_CC
LA01_P_CC
VCC
U1B
D1
/D1
SY55857L
Q1
Q1
GND
DGND

3V3
100R
R2
LA06_N
LA06_P
VCC
U1A
D0
/D0
SY55857L
Q0
Q0
GND
DGND

J2
1
2
3
4
5
6
7
DGND
SATA7-67491-1030

Sheet: /SATA_connectors/
File: SATA.sch
Title:
Size: A4   Date:
KiCad E.D.A. eeschema (2014-jan-25)-product
Rev:
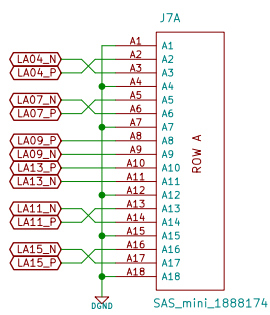Id: 3/4

J6A
A1 A1
A2 A2
A3 A3
A4 A4
A5 A5
A6 A6
A7 A7
A8 A8
A9 A9
A10 A10
A11 A11
A12 A12
A13 A13
A14 A14
A15 A15
A16 A16
A17 A17
A18 A18
ROW A
SAS_mini_1888174

LA19_N
LA19_P
LA21_N
LA21_P
LA24_P
LA24_N
LA28_P
LA28_N
LA30_N
LA30_P
LA32_N
LA32_P
DGND

J6B
B1 B1
B2 B2
B3 B3
B4 B4
B5 B5
B6 B6
B7 B7
B8 B8
B9 B9
B10 B10
B11 B11
B12 B12
B13 B13
B14 B14
B15 B15
B16 B16
B17 B17
B18 B18
ROW B
SAS_mini_1888174

LA20_N
LA20_P
LA22_N
LA22_P
LA25_P
LA25_N
LA29_P
LA29_N
LA31_N
LA31_P
LA33_N
LA33_P
DGND

3V3
J8 1
2
3
DGND
JUMP_2X2_CONN

J7A
A1 A1
A2 A2
A3 A3
A4 A4
A5 A5
A6 A6
A7 A7
A8 A8
A9 A9
A10 A10
A11 A11
A12 A12
A13 A13
A14 A14
A15 A15
A16 A16
A17 A17
A18 A18
ROW A
SAS_mini_1888174

LA04_N
LA04_P
LA07_N
LA07_P
LA09_P
LA09_N
LA13_P
LA13_N
LA11_N
LA11_P
LA15_N
LA15_P
DGND

J7B
B1 B1
B2 B2
B3 B3
B4 B4
B5 B5
B6 B6
B7 B7
B8 B8
B9 B9
B10 B10
B11 B11
B12 B12
B13 B13
B14 B14
B15 B15
B16 B16
B17 B17
B18 B18
ROW B
SAS_mini_1888174

LA03_N
LA03_P
LA08_N
LA08_P
LA12_P
LA12_N
LA14_P
LA14_N
LA16_N
LA16_P
LA17_N_CC
LA17_P_CC
DGND

Sheet: /miniSAS_connectors/
File: miniSAS.sch
Title:
Size: A4 | Date: | Rev:
KiCad E.D.A. eeschema (2014-jan-25)-product | Id: 4/4

Appendix C
Content of enclosed CD

- Thesis source code
- Measured data file from interferometric station
- Installation file of gnuradio in version used in work
- GRC flow-graphs
- Used datasheets
- Photographs from development and testing
- Source files for designed PCB modules.